



Mirabilis Design dramatically advances Electronics System Level Design by eliminating the six to nine months development effort required to create processor models for use in designing architectures.

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Mirabilis Design announces Processor Generator Toolkit; Rapid architecture model generator for designing multi-core and multi-processor systems

Sunnyvale, CA. — February 13th, 2006— Mirabilis Design Inc. of Sunnyvale, CA, a leading provider of system architecture design software for hard real-time electronics with embedded software, today announced the release of the first in a series of hardware and software model generators for the VisualSim Architect. The Processor Generator Toolkit enables users to generate detailed cycle-accurate simulation models of microprocessors, microcontrollers, DSP and application-specific processors in less than one day using only parameters. The toolkit enables processor architects to optimize the pipeline and instruction set, systems engineers to design new system platforms and software engineers to experiment with flows, thread distribution and scheduling long before an architecture commitment is made.

“Growth in system design has been slower than industry expectations. The long time taken to construct models is the primary cause of this situation,” according to Deepak Shankar, President of Mirabilis Design Inc. “Most models written in C or SystemC are over 10K lines of code, answer a specific question, and are virtually not reusable. The VisualSim Generators have reduced model development from months to days. Finally, the industry can achieve a good Return-on-Investment (ROI) for system-level design.”

The Processor Toolkit works by describing a processor using information from the vendor datasheet. This data is input into a wizard containing parameters, instruction table and pipeline stages. The resulting processor model is used to define complete systems with the Architecture Library components- RTOS, bus, switch, DRAM, DMA, controller and cache. Software instruction sequences and pseudo-code can be executed on this model for performance and power evaluations of multi-processor or multi-core systems.

Mirabilis Design has completed customer projects using this Toolkit. A PowerPC 7410 with AltiVec was created using this Generator. A multi-processor computer with local cache connected through a Rapid I/O and a Raceway serial interface to the memory sub-system was built around the generated block. Synthetic Aperture Radar (SAR) software was executed on this model to identify the real-time bottlenecks and then compared with the physical prototype. The processor generation, model development and analysis required less than 5 days effort. Additional projects include comparing dual ARM7 and single ARM 9 for an AES Rijndahl algorithm implementation.



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The generated processor model provides full visibility into the pipeline, execution units, instruction set, pre-fetch actions, data and instruction cache access, superscalar, out-of-order executions and interrupts service routines. Analyses include latency by transaction, route mapping, utilization by individual unit, stalls, flush time, context-switching, hit-miss ratio and throughput.

VisualSim Architect is a graphical, platform-independent design environment that accelerates performance analysis and architecture exploration. Designers construct models using pre-built parameterized construction components and use the automated statistics and run-time visualization for ad-hoc analysis. VisualSim has fully integrated SystemC and all mathematical capabilities of MatLab. In addition, there are co-simulation links to Verilog, VHDL, STK, Excel and MatLab and an open, timed-API for integrating simulators. VisualSim optimizes the initial concept through a series of modeling refinements and abstractions to allow the best architecture to become an executable specification.

Availability

VisualSim Processor Generator Toolkit is part of the Architecture Library and is currently available on Windows, Linux and UNIX. VisualSim Architect is a prerequisite for the Toolkit. Pricing for the Processor Generator Toolkit starts at \$5000 including parameter settings for PowerPC and ARM. Other processor parameters can be defined by the user or are available at no extra charge from Mirabilis Design.

About Us

Founded in 2003, and headquartered in Sunnyvale, CA, USA, Mirabilis Design is a leading provider of System-Level Architecture Exploration software for designing hard real-time electronics with embedded software. Mirabilis Design accelerates Concept to Specification by drastically reducing typical model development from months to days. Typical systems engineering efforts have been reduced by over 6X and overall project time by 25-30% using the VisualSim software package. The core product, VisualSim, is a modeling and simulation environment that provides the required simulation engines, modeling libraries, analysis tools and interfaces for conducting systems experimentation with the required level of accuracy. There are two variations of VisualSim: VisualSim Architect is used by designers to construct models and conduct ad-hoc analyses. VisualSim Explorer is Web Server software used to distribute specifications as executable simulation models embedded in documents accessed by just a web browser.

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