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design

Concept Exploration, Architecture Analysis, Functional Validation



Workshop A3: Accelerating AdvancedTCA Product Design Cycles

Goals of Session

- Create framework for architecture exploration
- Identify problems and applications addressed by this exploration
- Provide example to demonstrate the exploration
- Study impact of performance, functional & power analysis

Agenda

- Overview of Architecture Exploration
- Performance, Power and Functionality
- Case Study: Server Blade Design
- Benefits and risks
- Biography
- Q&A

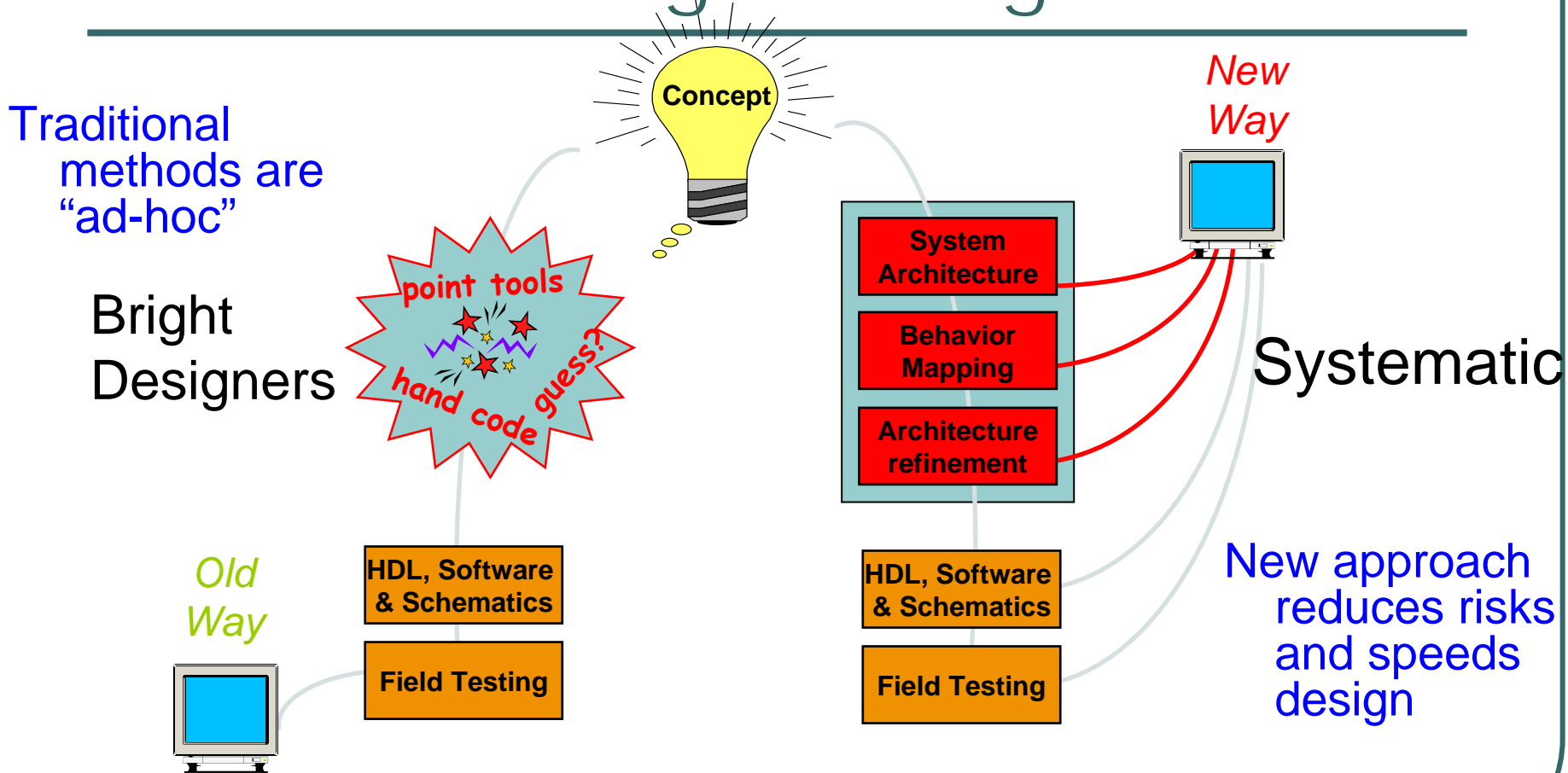
ATCA Design Challenges

- Design time is short
- Keep up with technology shifts
- Support growing application needs
- Software-base is exploding
- Create unique differentiation

***Without over-sizing,
How do you create the lowest cost, highest QOS and
minimal power consumption for largest Applications?***

From Concept to Prototype

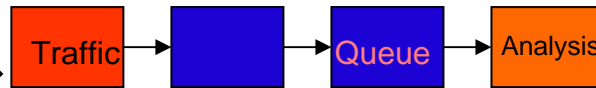
"Is this the Right Design?"



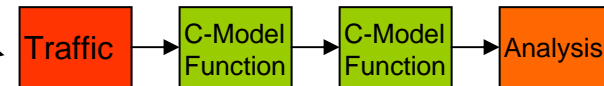
Errors in early architectural decisions cannot be revised with low-level optimization efforts

Engineering Design Flow

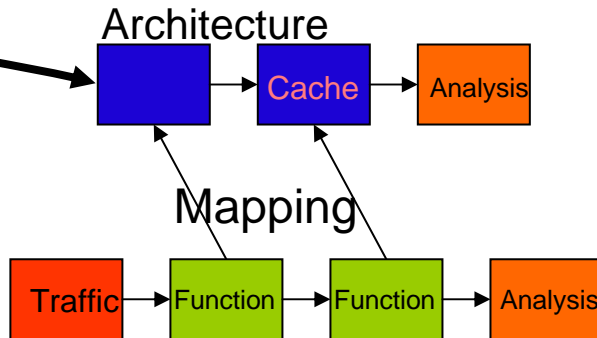
Step 1: Performance/Power
Transaction-Level



Step 1: Algorithm
Behavior/ Untimed



Step 2: Architecture/
Cycle-accurate



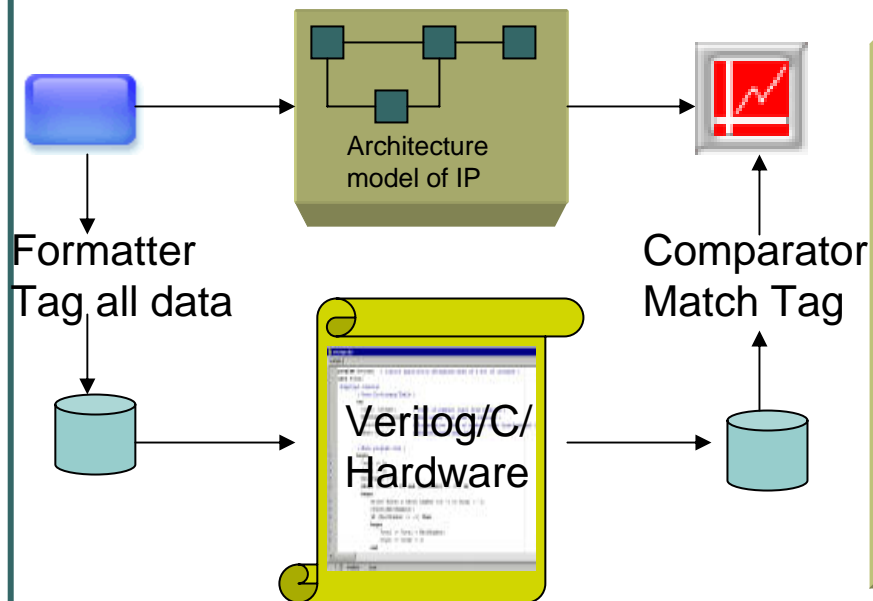
Behavior

Refine

Refine with
C-code

Is this the Right Design?

System Verification



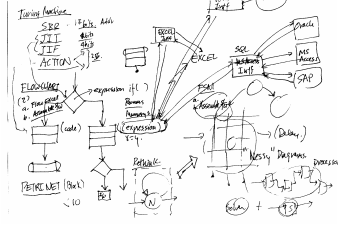
- Validate product not just HW/SW
 - Application relevant test vectors
- Match architecture timing
 - Within band range
- Verify software functionality
 - Task sequencing @ DSP/uP
 - Resource contention

Eliminate product failure by maximizing relevant verification

Performance, Power and Functional Exploration

Need to design a new phone
 -Must play MP3 files
 -Java games so, accelerator
 -Need a uP, DSP and FPGA

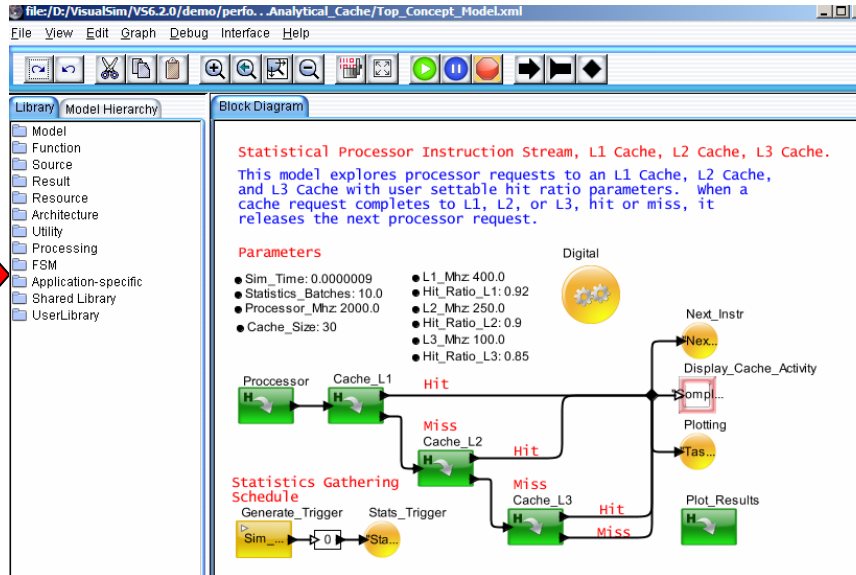
Customer Requirements



Discussion



Idea



Analysis Bottlenecks Throughput Capacity

Golden Reference Architecture Defn. Component Size Function mapping

Concept Engineering and Design Optimization

Server Blade Virtual Prototype

file:/D:/VisualSim/Test/VS3_0_1/demo/HAL/SAR/SAR_App7.xml

File View Edit System Graph Debug Interface Help

Library Model Hierarchy Block Diagram

High-Performance Blade Server
 Conduct architecture trade-off for implementing SAR application software on a multi-processor system

Parameters.

- Board_Name: "Board_1"
- Channel: "RapidIO"
- Switch_Speed: 1000.0

State_Plot_Block
 State_Plot_Block2

DE Simulator

Architecture Configuration.

C-Code Scheduling on the Processor(s).

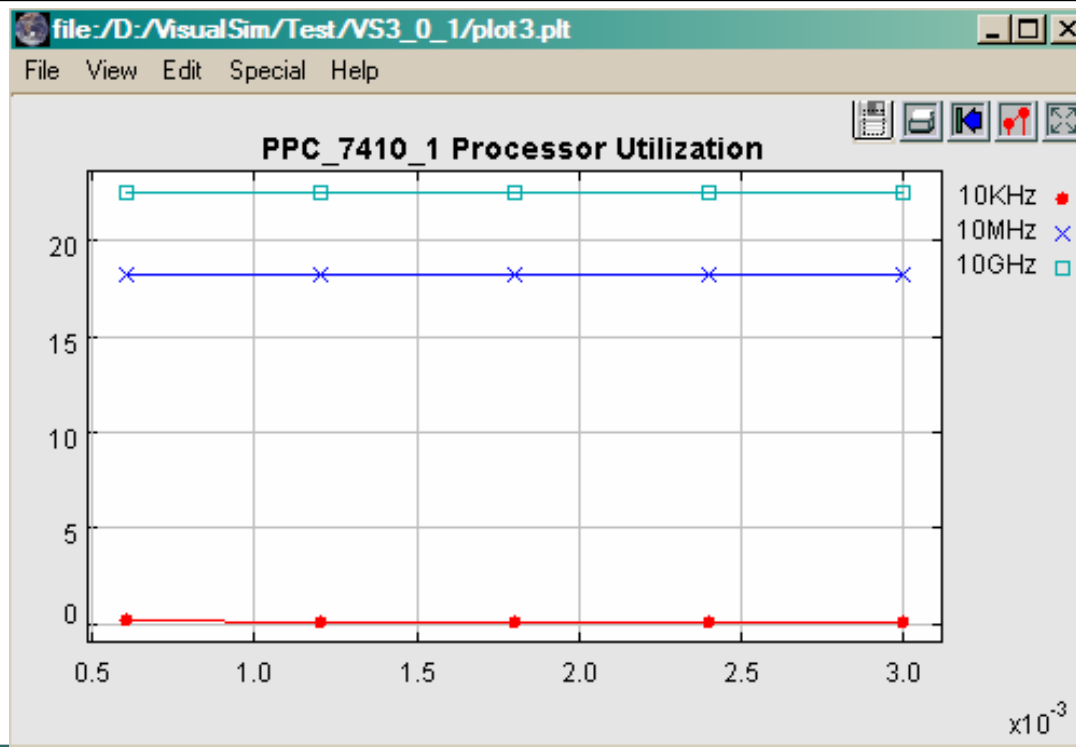
Architecture Setup, Utilization, Instruction_Set, State_Plot_Block, PPC_7410_1 Server, PPC_7410_2 Server, Backbone Switch, Memory1, Memory2, SDR, Chan., MUX, MUX2, A_D., A_D., Rap., Rac., Pro...

Command

ModelBuilder 3.0-beta (November 22, 2005)
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Analysis Output

Input Traffic Rates	10 KHz	10 MHz	10 GHz
PPC 7410 Stall	2.60%	59.03%	50.65%



When to Conduct System Simulation

- Performance, Power or Functionality is non-deterministic
- Refine or validate specification
- Start of the design cycle
- Changes to requirements
- Inconsistency of specification vs. Implementation

System Explorations

- Selecting the right platform
 - Processor-based, FPGA or SoC-centric designs
 - Trade-off power, performance and functionality
- Hardware-Software partitioning
 - Multiple Processors vs. Hardware Acceleration
- Identify capacity limitation or bottlenecks
 - Multiple DMA, Co-Processor and sizing peripherals
- Prototype full system operation
 - Traffic, FPGA, SoC, Processor/DSP and channels
- Diagnostics and verification
 - Reuse system model for verifying RTL, C and prototype
 - Select test points based on system response

Is this the “Right” design?

Guidelines for Top-Down Modeling

- Start top-down
- Create baseline model using a known reference
- Create empty Hierarchical block
- Add details to the Hierarchy
- Define traffic/workload and analysis
- Build models in steps and verify at each step
- Combine individual tested blocks to create full system

Guidelines for Modeling and Qualification

- Selecting right modeling approach
 - Which blocks and language for a particular exploration
 - Standardize naming conventions for ports, memory, parameters and blocks
 - Parameters, memory and interfaces definition to ensure block reuse
 - Interface definition to integrate 3rd party
 - Define transactors for integration of implementation models
 - Custom code format for reuse on all OS and new projects
- Guidelines for model qualification
 - Setup threshold for model acceptance- Utilization or Throughput levels
 - Establish attributes combinations for test sign-off
 - Define traffic and parameter randomization ranges

Guidelines for Analysis

- Performance
 - Latency, Utilization and Throughput
- Functional
 - Flow correctness
 - Impact of trigger signals and registers
 - Stateflow diagrams
- Meeting requirements or constraints
 - Match output at system, implementation and field testing
- Power Consumption and associated Thermal metrics
 - Determine tolerance and operating ranges
- System reliability
 - Randomize inputs to test reliability in different conditions

Presenter: Deepak Shankar

- Founder and CEO, Mirabilis Design Inc.
- Advanced degrees in Systems Engineering and Telecommunication
- Over 15 years experience in systems engineering of network systems
- Developed the first hardware-software co-design approaches to dramatically reduce telecom product risk
- Created programs to improve design efficiency by 30-75%

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