Mirabilis Design Memory Library enables both SoC and systems architects to design memory controllers, maximize memory efficiency for performance-critical applications and lower power consumption.

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Mirabilis Design announces the industry-first Electronic System-Level Memory Model library to accelerate the trade-off memory architectures

Highlights:

- Largest collection of Memory models to evaluate bandwidth, read and write latency, and power consumed for different user cases.
- Can be combined with the extensive VisualSim architecture library to assemble the full system or SoC.

Sunnyvale, CA. — February 1st, 2016— Mirabilis Design Inc. today announced the release of the VisualSim Memory modeling library. This library contains all current and prior versions of DDR, LPDDR, HBM, SRAM, JEDEC-complaint memory controller and a generic memory controller. System designers and architects use this library to develop new memory sub-systems, explore new standards and algorithms, and optimize the memory access for their target application. The solution has been used to conduct trade-off between different speed/variations of DRAM, performance vs. power, and memory bandwidth efficiency.

“Memory interface design and analysis is the biggest demand from our system-level customer base”, said Deepak Shankar, Founder of Mirabilis Design. “This library is a first of its kind and contains all the required models in one folder. Our customers are using these blocks to architect deterministic read/write latency and maximize battery life.”

VisualSim Memory can be used with VisualSim resource, behavior and cycle-accurate modeling libraries to construct models, simulate and analyze the complete system or SoC. This library is used to validate proposal, conduct trade-off decisions, timing, throughput, arbitration algorithm, power consumption analysis, and study systems behavior with different configuration (single vs. dual channels, clock speed variations, addressing schemes, and controller algorithms).

Features of VisualSim Memory Modeling Library:

- DRAM blocks available are DDR2, DDR3, DDR4, LPDDR2, LPDDR3, LPDDR4, and SRAM
- Storage blocks available are Flash and SSD
- New technology available are NVM, and HBM
- Memory controllers available are JEDEC-standard, Multi Port-Multi Channel, and generic.

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- Statistical and Cycle-Accurate Cache

- These memory controller and RAM blocks can be combined with the processor, RTOS, buses, interfaces, traffic generators and other architecture components to assemble the entire system.
- The modeled systems can be simulated for a variety of interface speeds, traffic rates, memory capacity, controller attributes, vendor-specific timing.

Availability:
VisualSim Memory Modeling Library is available now and pricing starts at $5,000 in United States. This library requires VisualSim Architect to construct models and simulate. The product is supported on Windows, Linux and Mac OS/X.

Interact with the application of the DDR3 blocks from the memory library at:
http://www.mirabilisdesign.com/new/software/demo/methodology/SW_I1D1_AXI_HWDRAM.html

Image of the library is provided at:
http://www.mirabilisdesign.com/Resources/Images/Memory_Controller.png

About VisualSim Architect:
VisualSim Architect is a system-level modeling, simulation, and analysis environment with a wide-ranging set of libraries and application templates that significantly improve model construction and analysis time. The environment enables designers to rapidly converge to a design which meets a diverse set of interdependent time- and power requirements. Additional information is available at: http://mirabilisdesign.com/new/visualsim/

About Mirabilis Design:
Mirabilis Design is a Silicon Valley company, providing software solutions to identify and eliminate risk in the product specification; accurately predict the human and time resources required to develop the product; and improve communication between diverse engineering teams. Additional information is available at: http://mirabilisdesign.com/new

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