Adding Software Development features into System-Level Design creates a higher quality product testing and validation platform

Editorial Contact
Anupurba Mukherjee
Product Marketing
Email:amukherjee@mirabilisdesign.com

Mirabilis Design Inc.
2010 El Camino Real, #1061
Santa Clara, CA 95050
Tel: 408-245-8992

Mirabilis Design integrates Fast Functional Processors into VisualSim Architect to close the software design, development and validation loop

Sunnyvale, CA. — January 27, 2020 — Mirabilis Design announces VisualSim VPS, a platform that combines VisualSim hardware model with Gem5 Instruction Set. This integration brings together the software execution capabilities of Gem5 with the validated semiconductor /embedded /network libraries in VisualSim. VisualSim VPS supports 32-bit and 64-bit architectures, multi-core, and out-of-order processors. Instruction Sets available are ARMv7, ARM v8, ARM SVE, RISC-V, x86, Power and CUDA GPU. All Instruction Sets in VPS come pre-loaded with Linux and a graphical debugger.

"Our customers can now map the software task graph onto a hardware platform, get the scheduled optimized and then immediately start the software development. This new approach saves months from the current methodology for software development. Based on our early customer experience, we have seen projects save almost 6 months and reduce costs by 15%."
-said Deepak Shankar, Founder of Mirabilis Design.

VisualSim VPS has been tested with Electronic Control Units, Infotainment systems, AI processors and hybrid prototyping of Radar systems. This innovation improves the quality of architecture exploration, enables accurate performance testing, integrates research and product development, simulate the entire system or semiconductor prior to development, and shift software development to systems engineering. Systems engineer can generate task graphs of the software and hardware engineers can map it to architecture models to experiment with integrated vs. distributed, multi-core vs. multi-processor, multi-thread vs. single-thread, and ARM vs. RISC-V. Software developers can replace parts of the task graph with the software running on the Instruction Set while hardware engineers can replace with physical prototypes, thus offering a flow from concept to debugging. Mirabilis Design has substantially reduced cost of software development, increased validation from concept to deployment, and created a collaborative platform for OEM, suppliers, and semiconductor vendors.

With VPS, the software behavior model can be replaced with the software executing on an OS that runs on the target processor platform. This provides greater validation of the architecture and allows the software developer to reuse the same early architecture model for software development.

To jumpstart the adoption of VPS, Mirabilis Design has created a number of templates- that bring together emulators, FPGA boards, AXI, Network-on-chip, cache coherency and a complete suite of

memory models. These templates can be used immediately in automotive, medical, IoT, industrial and space applications.

Availability

VisualSim VPS is shipping right now and is available on Ubuntu Linux 18.04 and 20.04 and centOS, Python 2.72, gcc 4.8 or clang 3.1 (or newer), and SWIG 2.0.4 or newer. VPS will work with VisualSim Architect 2030 and is provided as a free upgrade. VisualSim Architect is available on Windows, Linux and Mac OS. VPS does not require a separate license for the Instruction Set Simulators and can be distributed freely.

About Mirabilis Design

Mirabilis Design, a Silicon Valley company, designs cutting edge software solutions that identify and eliminate risks in product performance. Its flagship product, VisualSim Architect is a system-level modeling, simulation, and analysis environment that relies on libraries and application templates to vastly improve model construction and time required for analysis. The seamless design framework facilitates designers to work on a design together, cohesively, to meet an intermeshed time and power requirements. It is typically used for maximum results, early in the design stage, parallel to the development of the product's written specification. It precedes implementation stages - RTL, software code, or schematic – rendering greater design flexibility.

########

Trademarks