S2C and Mirabilis Design teamup to deliver a heterogeneous solution for SoC architecture exploration and verification

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Santa Clara, CA. — August 18, 2020 — S2C and Mirabilis Design today announced the collaboration and delivery of a hybrid SoC architecture exploration solution that reuses available RTL-based blocks to accelerate model construction and speed-up very complex simulations. The collaboration enables design projects that deploy model-based design methodology to further reduce the time and effort spent on creating complicated custom models of legacy designs.

As part of this collaboration, Mirabilis Design's VisualSim architecture exploration solution integrates S2C's FPGA-based Prodigy Logic System as a functional block. The seamless integration allows an FPGA prototype to act as a sub-model, and to provide accurate simulation responses, in system exploration.

"Electronic System-Level architecture exploration is an essential solution for SoC product trade-off and validation. The core technology of VisualSim solution has already lowered the modeling barrier. If a portion of the SoC is available in RTL, then the modelling effort can be further reduced by reuse." Said Deepak Shankar, Founder of Mirabilis Design. "Modeling custom blocks has traditionally been a challenge in creating a system-level model. The collaboration enables the RTL behavior to be easily integrated into the ESL model to create a virtual platform. The model can be simulated to gather metrics on response times, throughput, power consumption and correctness of data values. "

"Design the right product needs to come before design the product right. As today's SoC getting increasingly complex, we have observed a large increase of functional design errors related to specifications in recent years." Said Toshio Nakama, CEO of S2C. "The ability to accurately model

the system that comprises of design blocks in various level of abstractions is key to making sure designers are catching specification issues early in design cycles. We are excited to partner with Mirabilis to offer prototyping users a hybrid SoC architecture exploration methodology."

About **Mirabilis Design**

Mirabilis Design is a Silicon Valley software company providing Architecture Exploration solutions for the automotive, semiconductor and electronics industries. The architecture exploration solution enables teams across companies and time-zones to collaborate, visualize the product before development; validate and optimize the specification; and compute the business metrics such as cost, resource requirements and schedule. VisualSim Architect is a system-level modeling, simulation, and analysis environment that provides technology-accurate modeling libraries and application-specific templates to enable rapid model construction and maximize the scope of analysis. VisualSim enables design teams to generate timing, throughput, power and functional correctness measurement of the full system prior to Model-based System Engineering. For more information please visit www.mirabilisdesign.com.

About **S2C**

S2C, is a global leader of FPGA prototyping solutions for today's innovative SoC/ASIC designs. S2C has been successfully delivering rapid SoC prototyping solutions since 2003. With over 500 customers and more than 2,500 systems installed, our highly qualified engineering team and customer-centric sales team understands our users' SoC development needs. S2C has offices and sales representatives in the US, Europe, Israel, China, Korea, Japan, and Taiwan regions. For more information please visit www.s2cinc.com.

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