Supporting the RISC_V community with design tools

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Mirabilis Design creates the first RISC-V system-level architecture exploration solution

Santa Clara, CA. — May 20, 2020 — Mirabilis Design announced today the VisualSim RISC-V system modeling and simulation environment. With this release, VisualSim provides a complete RISC-V modeling package for developers of RISC-V IP, designers of RISC-V processors and systems engineers developing applications using RISC-V components. The package contains configurable RISC-V core, vendor-specific RISC-V processors, TileLink, DMA, peripherals, RTOS, memory modules and over 20 application templates in IoT, networking, wireless, consumer electronics, automotive and high-performance computing systems. The library components are compatible with the rest of the hardware, software, schedulers and network library from Mirabilis Design.

To introduce this RISC-V solution, Mirabilis Design is conducting a complementary RISC-V Webinar on May 27. Register at: https://www.mirabilisdesign.com/sign-up/

"We have seen demand for everything RISC-V but the feasibility of a final product is an unknown in most applications," says Deepak Shankar. "It is far cheaper to build a virtual prototype in VisualSim and experiment with it, than invest a year and $20 million."

The VisualSim system model provides the first clear view of your product using RISC-V. These models are constructed early in the design phase and far before development has started. This solution enables product designers to evaluate feasibility, eliminate risk and identify system bottlenecks of products using RISC-V. In the VisualSim environment, the user constructs a model of the product, add the traffic and sensor interfaces and defines the user-cases. This model is simulated with different parameter values and scenarios. The generated reports provides visibility into timing deadlines, power consumption, resource efficiency, deadlocks, buffer occupancy, data overflow, quality of service and functional correctness.

RISC-V library from Mirabilis Design contains all the building block required to assemble a product that incorporates a RISC-V, be it a semiconductor component or a supercomputer. The application templates accelerate the modeling effort and enables new modelers to quickly put together a system. The eco-system consists of common trace interfaces, task graph generators, pre-configured reports and a visualizer that pinpoints the exact system behavior. The models can be built as a combination of stochastic and timing-accuracy. All the library blocks combine timing, power and functionality, making it the first RISC-V package that allows for true trade-off studies.

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You can view the usage of the library from,
Solid State Device using RISC-V Processor:
http://www.mirabilisdesign.com/launchdemo/demo/system_architecture/SSD/SSD_RISC_V/
System-on-chip using RISC-V core:
https://www.mirabilisdesign.com/launchdemo/demo/HAL/RISC_V/RISCV_InOrder/

About VisualSim Architect
VisualSim RISC-V is available as a standard library option in VisualSim 2020. , the modeling
and simulation platform from the Mirabilis Design. This product is used extensively in
designing products ranging from processors to automobiles. VisualSim Architect is available on
Windows, Linux, and MAC OS.

About Mirabilis Design
Mirabilis Design, a Silicon Valley company, designs cutting edge software solutions that identify
and eliminate risks in product performance. Its flagship product, VisualSim Architect is a
system-level modeling, simulation, and analysis environment that relies on libraries and
application templates to vastly improve model construction and time required for analysis. The
seamless design framework facilitates designers to work on a design together, cohesively, to
meet an intermeshed time and power requirements. It is typically used for maximum results,
early in the design stage, parallel to the development of the product's written specification. It
precedes implementation stages - RTL, software code, or schematic – rendering greater design
flexibility.

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