Power Modeling

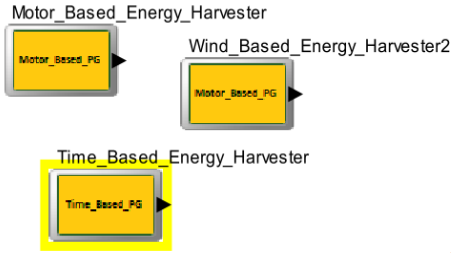
1 Power Generation

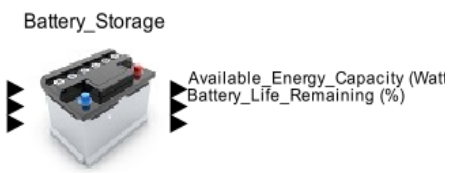
2 Power Storage

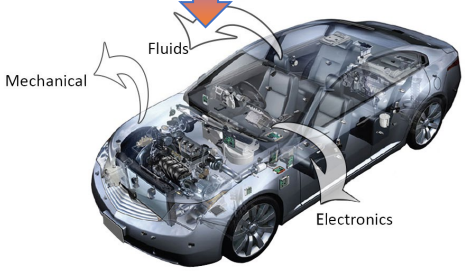
3 Power Consumption

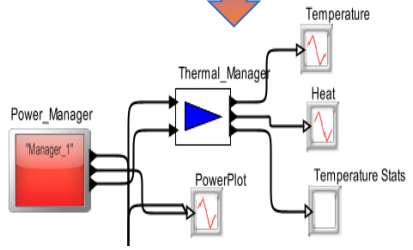
4 Power Management

5 Thermal Management









- 3 Types of Power Generators in VisualSim
- Power Profiles can be defined with constant or variable charge capacity (Watt-Hr)

- Instantaneous energy capacity
- Battery Life Remaining
- Total Battery Consumption
- Charge drop due to power surge
- Battery Low Warnings

- State based power consumption of both electronics (controller, SOC) and Mechanical parts (brakes, wheels)
- Average Power, Instantaneous Power and Cumulative Power report

- PowerStates can be defined using PowerTable or using a state change diagram

- Thermal Management based on average power and power state changes

6

Verification and Debugging

- Decide on power management algorithms based on power consumption
- Sizing of power generators
- Debugging power spikes
- Understanding power consumed by the software application
- Power Consumption overhead due Voltage and Frequency Transition time

7

Downstream Integration

- Generate UPF format with power domains and associated voltage levels
- Generate systemVerilog power testbench
- Generate powerState change VCD dump for debugging

Concept of VisualSim Power Technology

Incorporate hardware, software and network
- Power changes based on Workloads and use-cases

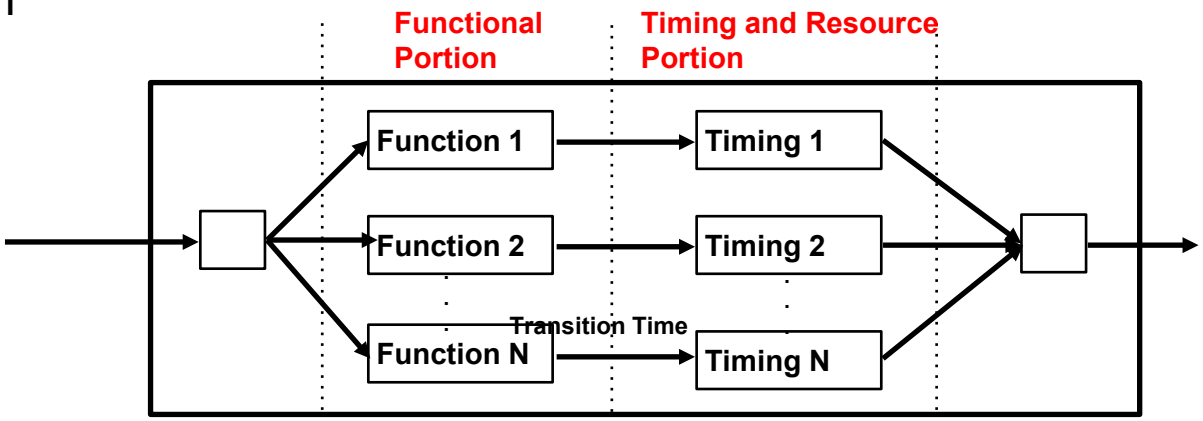
Power for each devices modeled as states at each clock cycle
- Task -based power, transitions and management logic

Hierarchical power management with each H block owning an individual Power Table
- Next-level Power Table cumulates all lower-level power devices

Looks at each of the entities in detail
- **Generation-** Multiple sources- wind, solar, motor, constant and custom
- **Storage**- Types of batteries
- **Consumption** at various rates by multiple devices with different clock speeds
- **Management** based on time and custom logic

Generate UPF power profile for downstream test and SystemVerilog Testbench for Power

Reports are average, instant, battery life, usage, comparison between input, available and consumed



Block Functional and Timing Diagram

Block Power Mode Diagram

Power is now an integral part of Architecture Exploration

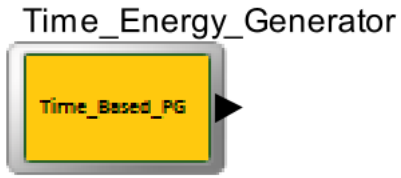
Power Generator

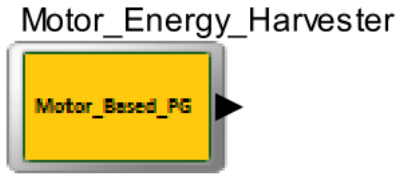
Time-Energy

- Constant Power Source
- File Based
- Time Based

Motor-Energy

- Motor Based Power Generation
- Wind Based Power Generation





Time-Energy Settings

UseTraceFile:	false /* boolean enables mode */
Trace_File_Name:	/* file name */
UseTimeBased:	false /* boolean enables mode */
Time_Based_Duration:	10.0E-03 /* time seconds */
Time_Based_Charge_Setup:	/* Time-Based Charge Profile */ ID StartWHR EndWHR Efficiency PercentTime ; 1 0.0 20.0 100.0 15.0 ; 2 20.0 20.0 100.0 50.0 ; 3 20.0 0.0 100.0 15.0 ; 4 0.0 0.0 100.0 20.0 ;
UseConstant:	true /* boolean enables mode */
ConstantChargeCapacity:	500.0 /* charge rate in Watt-Sec */
SimTime:	1.0

Using Trace file from existing system

Using Time-based

1. Duration is the period
2. Setup has % of time in the Period of each time
3. Charge can increase or reduce during the period
4. Efficiency is amount of charge converted

Constant output at the set rate

Motor-Energy Settings

Use_Wind_Turbine:	false
Wind_Turbine_Setup:	/* Wind_Turbine Charge Profile */ ID Duration Speed Efficiency ; 1 4.0 3.728 95.0 ; 2 4.0 4.970 97.0 ; 3 4.0 5.592 100.0 ; 4 4.0 6.213 100.0 ; 5 4.0 4.970 97.0 ; 6 4.0 4.319 95.0 ;
r:	1.0/*Rotor Radius in meter*/
row:	1.225/*air Density*/
k:	0.000133/*Constant*/
Cp:	0.40/*Maximum Power Coefficient*/
Use_Motor_Generator:	true
Motor_Charge_Setup:	/* Motor-Generator Charge Profile */ ID RPM Duration ChargeCapacityWHR Efficiency ; 1 0 10.0 0.0 100.0 ; 2 2500 10.0 55.0 100.0 ; 3 2500 10.0 55.0 100.0 ; 4 4000 10.0 105.0 100.0 ; 5 4500 10.0 110.0 100.0 ; 6 4000 10.0 105.0 100.0 ; 7 2500 10.0 55.0 100.0 ; 8 2500 10.0 55.0 100.0 ; 9 0 10.0 0.0 100.0 ;
SimTime:	1.0

Compute the Wind Power based on air speed and efficiency

Motor based on RPM

Power Storage - Battery

Used to capture

- Rate of consumption
- Impact of continuous charging
- Lifecycle loss due to power spikes and thermal shock
- (Experimental) Heat and Temperature

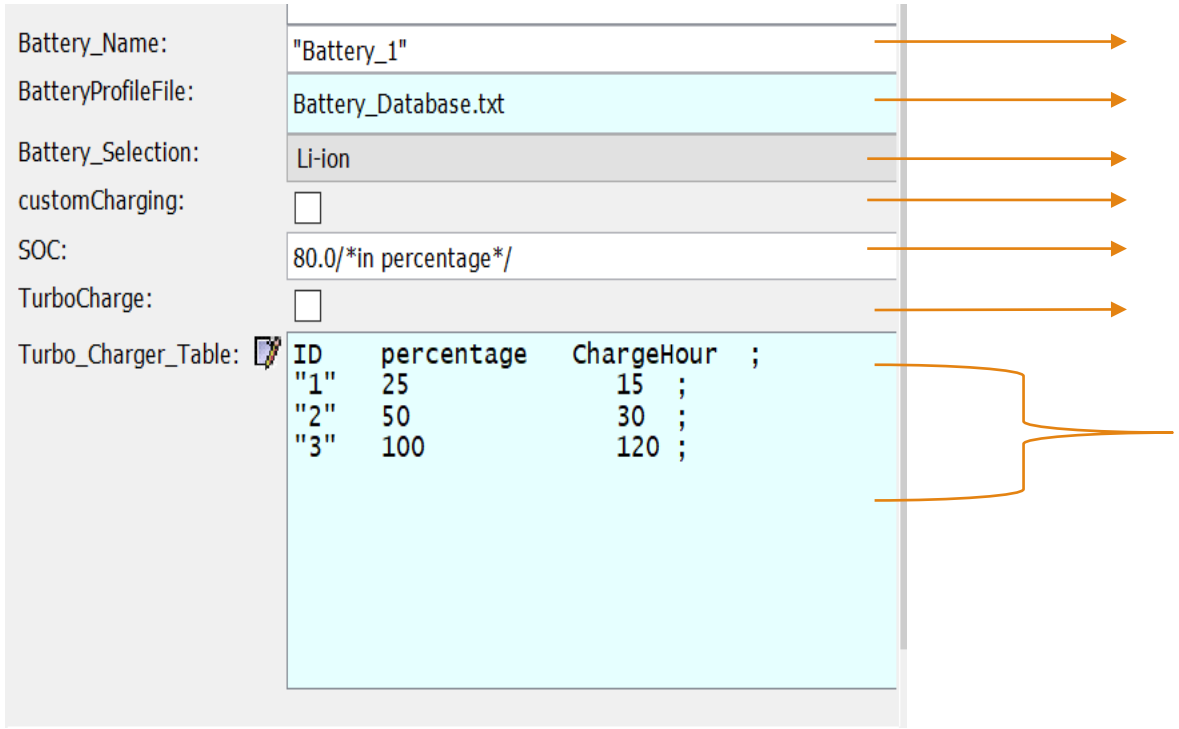
Types of batteries support

- Battery database support NiCd, Li-Ion, NiMh, LdAcid

Activities modeled

- Charging- SOC threshold, Turbo charge, all input charge
- Discharge- From the PowerTable
- Lifecycle, discharge

Battery Block - Parameters



Requires Unique name
Default database provided
Select battery type
Default charging is the value arrive. Click to Custom
State of Charge for charging to resume.
Enable Turbo charging

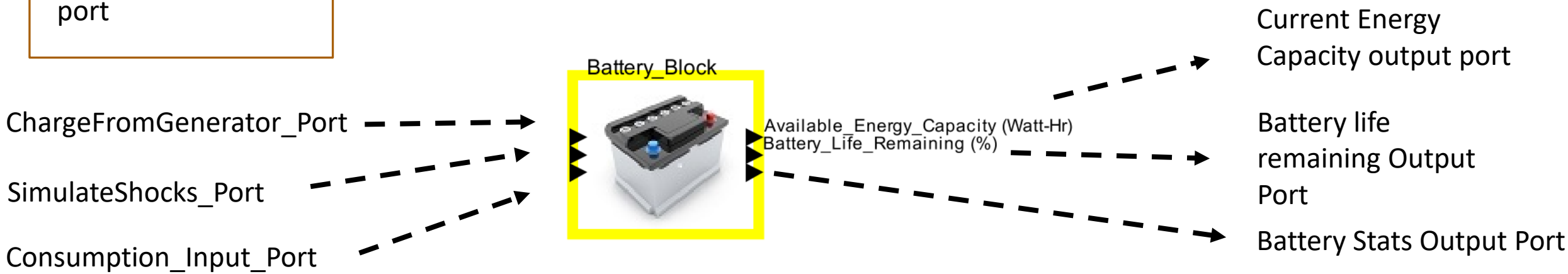
Time taken to get to each level of charge. Similar to phone battery chargers

Note:
Power generated when not charging is wasted.
User can add items to the database
Edit the instance to add the new battery types

Block Ports

Connect
1. Power Generator
2. Aging input in %
3. Power Table
Instantaneous power port

Connect Output Ports to TimeDataPlotter and TextDisplay



Power Management

Power Table

Edit parameters for PowerTable2

Block_Documentation:
```
This is the Excel spreadsheet import.  The power
information is maintained here.
```

Manager_Name: "Manager_1"

fileOrURL: Browse

Manager_Setup:
```
    Architecture_Block          Standby  Active  Wait     Idle         Down    Existing  OffState  OnState  t_OnOff      Mhz          Volts   ;
Streaming_Board_ARM_1             stdy     act      wat      idl        0.0            Standby   Standby   Active   1.0e-8    Processor_Speed_MHz     1.0     ;
Streaming_Board_ARM_2             stdy     act      wat      idl        0.0            Standby   Standby   Active   1.0e-8    Processor_Speed_MHz     1.0     ;
Streaming_Board_MOVE            25.0     100.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
Cache_I_Cache_ARM_1             50.0     150.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
Cache_D_Cache_ARM_1             50.0     150.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
Cache_I_Cache_ARM_2             50.0     150.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
Cache_D_Cache_ARM_2             50.0     150.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
Cache_L2                        50.0     150.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
Streaming_Board_HW_ACC          10.0     100.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
Streaming_Board_HW_ACC_Bus      50.0     150.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
Streaming_Board_RAM_Bus         50.0     150.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
Streaming_Board_ROM_Bus         50.0     150.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
Streaming_Board_Ext_SDRAM_Bus   50.0     150.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
Streaming_Board_Ext_FLASH_Bus   50.0     150.0    0.0      0.0        0.0            Standby   Standby   Active   1.0e-8    1000.0     1.0     ;
ACT_Standby_Ext_SDRAM           37.6     0.1      22.4     0.0        0.0    Standby   Standby   Active     Cycle_t       1200.0 1.0     ;  /* No Rd, Wr   */
ACT_Active_Ext_SDRAM            37.6     0.1      22.4       0.0      0.0    Standby   Standby   Active     Cycle_t       1200.0   1.0     ;  /* No Rd, Wr   */
ACTIVATE_Ext_SDRAM              0.01     38.4     0.0        0.0      0.0    Standby   Standby   Active     Cycle_t       1200.0   1.0     ;  /* No Rd, Wr   */
WTR_Power_Ext_SDRAM             0.0      216.2    0.0        0.0      0.0    Standby   Standby   Active     Cycle_t       1200.0   1.0     ;  /* Same as Wr */
Write_Power_Ext_SDRAM           0.0      216.2    0.0        0.0      0.0    Standby   Standby   Active     Cycle_t       1200.0   1.0     ;
Read_Power_Ext_SDRAM            0.0      392.2    0.0        0.0      0.0    Standby   Standby   Active     Cycle_t       1200.0   1.0     ;
RRD_Power_Ext_SDRAM             0.0      13.8     0.0        0.0      0.0    Standby   Standby   Active     Cycle_t       1200.0   1.0     ;
RFSH_Power_0_Ext_SDRAM          11.8     12.0     0.0        0.0      0.0    Standby   Standby   Active     Cycle_t       1200.0   1.0     ;  /* Standby no Rd/Wr, else Down */
RFSH_Power_15_Ext_SDRAM         11.8     12.0     0.0        0.0      0.0    Standby   Standby   Active     Cycle_t       1200.0   1.0     ;  /* Standby no Rd/Wr, else Down */
Streaming_Board_Ext_FLASH       150.0     350.0   0.0      0.0        0.0          Standby   Standby   Active    1.0e-8    1000.0     1.0     ;
Scheduler_EBU_Scheduler         75.0     250.0    0.0      0.0      0.0   Standby   Standby   Active    1.0e-8    1000.0     1.0     ;
Scheduler_LMU_Scheduler         75.0     250.0    0.0      0.0      0.0   Standby   Standby   Active    1.0e-8    1000.0     1.0     ;
STR_AXI_ARM_Rd_Data_Channel     70.0     300.0    0.0   0.0              0.0   Standby   Standby   Active     0.0           1000.0     1.0     ;
STR_AXI_ARM_Wr_Data_Channel     70.0     300.0    0.0   0.0              0.0       Standby   Standby   Active     0.0           1000.0     1.0     ;
```

Delay_to_Change_State:
```
/* Async_State_Change.  First row contains Column Names, expressions valid for entries except Device Name.

--------Device Name-------  ------------Time State--------- */
    Architecture_Block      State     Time_or_Express  Next ;
Scheduler_HW_Engine         Standby   1.0e-3           Idle ;
```

Expression_List:
```
/* First row contains Column Names.

---------Reference--------  --------------Expression------------ */
Name                                Value                ;
Cycle_t                     0                            ;
multi                       ((2.0e-19)*Processor_Speed_MHz*Processor_Speed_MHz*1.0e12)+ ((-6.0e-11)*Processor_Speed_MHz*1.0e6)+0.017 ; /*value in Watts*/
act                         multi*1.0e3                  ;/* since power table is set to be using in milli watts scale, multiplying with 1.0e3 to balance it*/
stdy                        0.1*act                      ;
wat                         0.95*act                     ;
idl                         0.02*act                     ;
```

Battery_Units: Milli_Watts

State_Plot_Enable: ☐

Power State Table Entry

- **Manager_Name**: Unique name for this Power Manager
- **Manager_Setup** parameter :
  - ✓ Architecture block : Lists the devices supported by power table. A device can be divided into multiple sub-components with a unique line for each (Example-DRAM)
  - ✓ Power States: (Minimum list; Additional states added per need)
    - Standby: Power consumption when device is idle
    - Active: Power consumption when device is processing a task
    - Wait: Power Consumption when device is waiting for a response
    - Idle: Power consumption during Off state of the device

Edit parameters for PowerTable2

Block_Documentation: This is the Excel spreadsheet import. The power information is maintained here.

Manager_Name: "Manager_1"

fileOrURL:

Manager_Setup:

```
/* Power_Table.  First row contains Column Names, expressions valid for entries except Device Name.

--------Device Name--------  ---------Power States---------      -----Operating States------  -----------State Transitions---------  --Speed--  --Exist-- */
    Architecture_Block          Standby   Active   Wait    Idle    Existing  OffState  OnState  t_OnOff      Mhz                    Volts   ;
Streaming_Board_ARM_1           stdy      act      wat     idl     Standby   Standby   Active   1.0e-8    Processor_Speed_MHz    1.0     ;
Streaming_Board_ARM_2           stdy      act      wat     idl     Standby   Standby   Active   1.0e-8    Processor_Speed_MHz    1.0     ;
Streaming_Board_MOVE            25.0      100.0    0.0     0.0     Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
Cache_I_Cache_ARM_1             50.0      150.0    0.0     0.0     Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
Cache_D_Cache_ARM_1             50.0      150.0    0.0     0.0     Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
Cache_I_Cache_ARM_2             50.0      150.0    0.0     0.0     Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
Cache_D_Cache_ARM_2             50.0      150.0    0.0     0.0     Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
Cache_L2                        50.0      150.0    0.0     0.0     Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
```

Transition Details

- ✓ Operating State:
  - Existing: Initial state of the device
  - OffState: Off state of the device
  - OnState: Active/ON state of the device
- ✓ State Transitions
  - t_OnOff: transition time delay from one state to another. Value can be modified dynamically
  - "t_OnOff can be used to specify the time it will take to reach the peak power level once the change of state has been made.

Edit parameters for PowerTable2

Block_Documentation:

```
This is the Excel spreadsheet import.  The power
information is maintained here.
```

Manager_Name: "Manager_1"

fileOrURL:

Manager_Setup:

```
/* Power_Table.  First row contains Column Names, expressions valid for entries except Device Name.

--------Device Name-------  ---------Power States------                ----Operating States----  ----------State Transitions---------  --Speed--  --Exist-- */
    Architecture_Block          Standby  Active  Wait     Idle        Existing  OffState  OnState  t_OnOff      Mhz                    Volts   ;
Streaming_Board_ARM_1           stdy     act     wat      idl         Standby   Standby   Active   1.0e-8    Processor_Speed_MHz    1.0     ;
Streaming_Board_ARM_2           stdy     act     wat      idl         Standby   Standby   Active   1.0e-8    Processor_Speed_MHz    1.0     ;
Streaming_Board_MOVE            25.0     100.0   0.0      0.0         Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
Cache_I_Cache_ARM_1             50.0     150.0   0.0      0.0         Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
Cache_D_Cache_ARM_1             50.0     150.0   0.0      0.0         Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
Cache_I_Cache_ARM_2             50.0     150.0   0.0      0.0         Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
Cache_D_Cache_ARM_2             50.0     150.0   0.0      0.0         Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
Cache_L2                        50.0     150.0   0.0      0.0         Standby   Standby   Active   1.0e-8    1000.0                 1.0     ;
```

Power Table Parameters

- ✓ Optional Parameters
  - Mhz: used for computation done in Expression List
  - Volts: used for computation done in Expression List
  - More variables can be added. The values can be dynamic

Edit parameters for PowerTable2

Block_Documentation:

```
This is the Excel spreadsheet import.  The power
information is maintained here.
```

Manager_Name: "Manager_1"

fileOrURL:

Manager_Setup:

```
/* Power_Table.  First row contains Column Names, expressions valid for entries except Device Name.

--------Device Name-------  ---------Power States------                -----Operating States------  ----------State Transitions---------  --Speed--  --Exist-- */
    Architecture_Block          Standby  Active  Wait     Idle          Existing  OffState  OnState  t_OnOff      Mhz                    Volts    ;
Streaming_Board_ARM_1           stdy     act      wat      idl          Standby   Standby   Active   1.0e-8    Processor_Speed_MHz    1.0      ;
Streaming_Board_ARM_2           stdy     act      wat      idl          Standby   Standby   Active   1.0e-8    Processor_Speed_MHz    1.0      ;
Streaming_Board_MOVE            25.0     100.0    0.0      0.0          Standby   Standby   Active   1.0e-8    1000.0                 1.0      ;
Cache_I_Cache_ARM_1             50.0     150.0    0.0      0.0          Standby   Standby   Active   1.0e-8    1000.0                 1.0      ;
Cache_D_Cache_ARM_1             50.0     150.0    0.0      0.0          Standby   Standby   Active   1.0e-8    1000.0                 1.0      ;
Cache_I_Cache_ARM_2             50.0     150.0    0.0      0.0          Standby   Standby   Active   1.0e-8    1000.0                 1.0      ;
Cache_D_Cache_ARM_2             50.0     150.0    0.0      0.0          Standby   Standby   Active   1.0e-8    1000.0                 1.0      ;
Cache_L2                        50.0     150.0    0.0      0.0          Standby   Standby   Active   1.0e-8    1000.0                 1.0      ;
```

Power Management & Dynamic Compute

- Delay_to_State_Change is the power control state machine that changes state if the device has been in a particular state for a time period. The format is

  "<Device_Name> <State> <Time_or_Expression> <Next_State>"

- Expression_List define expressions for State values and can be computed dynamically. The format is

  "<Name> <value or expression> ; “

Delay_to_Change_State:

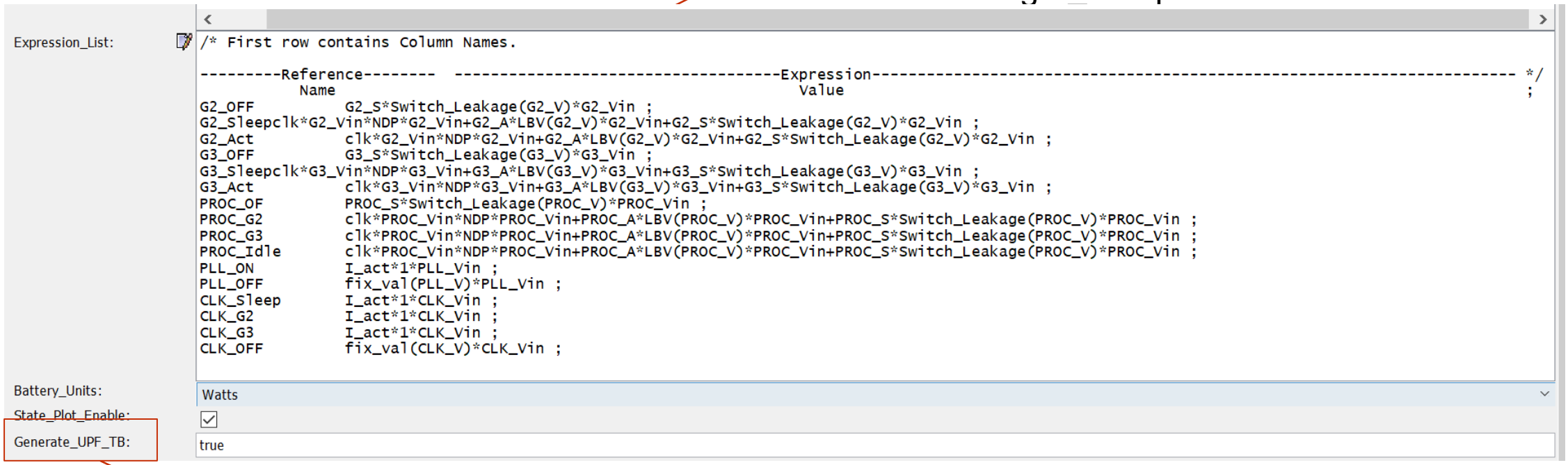
```
/* Async_State_Change.  First row contains Column Names, expressions valid for entries except Device Name.

--------Device Name-------  ------------Time State--------- */
    Architecture_Block      State     Time_or_Express  Next ;
Scheduler_HW_Engine         Standby   1.0e-3           Idle ;
```

Expression_List:

```
/* First row contains Column Names.

---------Reference--------  --------------Expression------------ */
Name                                Value                       ;
Cycle_t                     0                                   ;
multi                       0.227                               ;
act                         multi*1.0e3                         ;
stdy                        0.1*act                             ;
wat                         0.95*act                            ;
idl                         0.02*act                            ;
```

Power Table – Custom States and Other Options

User can define Power Equations or any other variables in the system and then use it in Manager_Setup



- Generates UPF File with Domains and Voltages Allotted based on Power Entry
- Generates System Verilog Behavioural description of PowerManager Block and System Verilog test bench based on the PowerState transitions in the model

- ❑ Custom states define dhere can be used in operating states
- ❑ Custom equations can be used in place of power number values, voltage, frequency

Configuring the Power Table

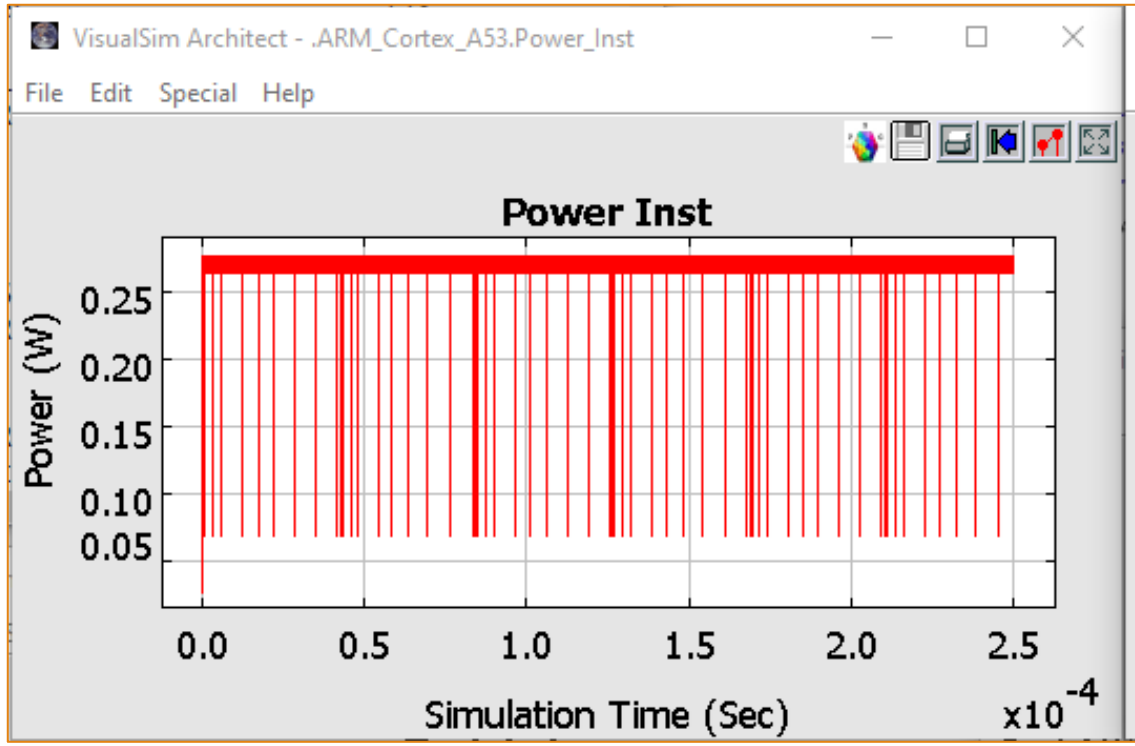
Minimum information

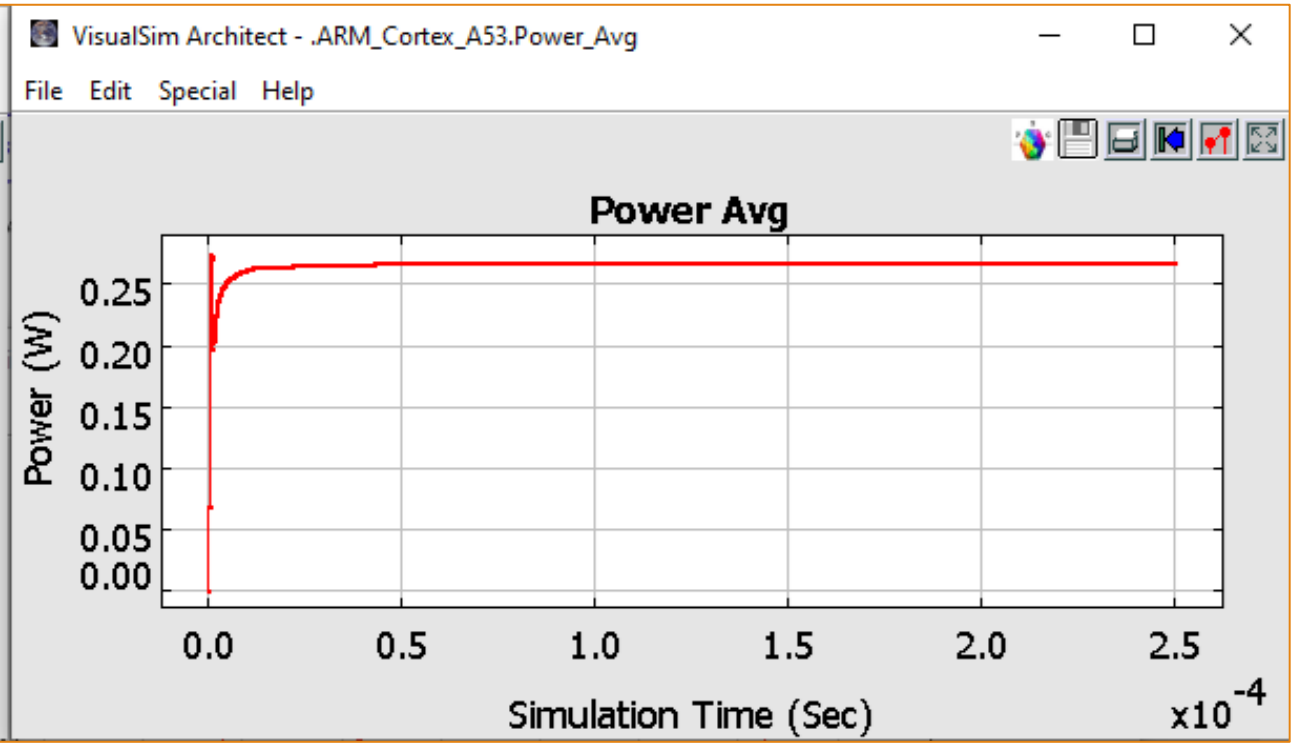
- List of states and associated power values
- Power values can be double or a complex expression that has variables

Each device

- Define power (in watts/mW/uW) for all the states (Active, Standby, Idle etc.)

VisualSim Power Plots





Detailed Power Stats

VisualSim Architect - .Power_Perf_example_A53_power_2.Stats.Power_Debug

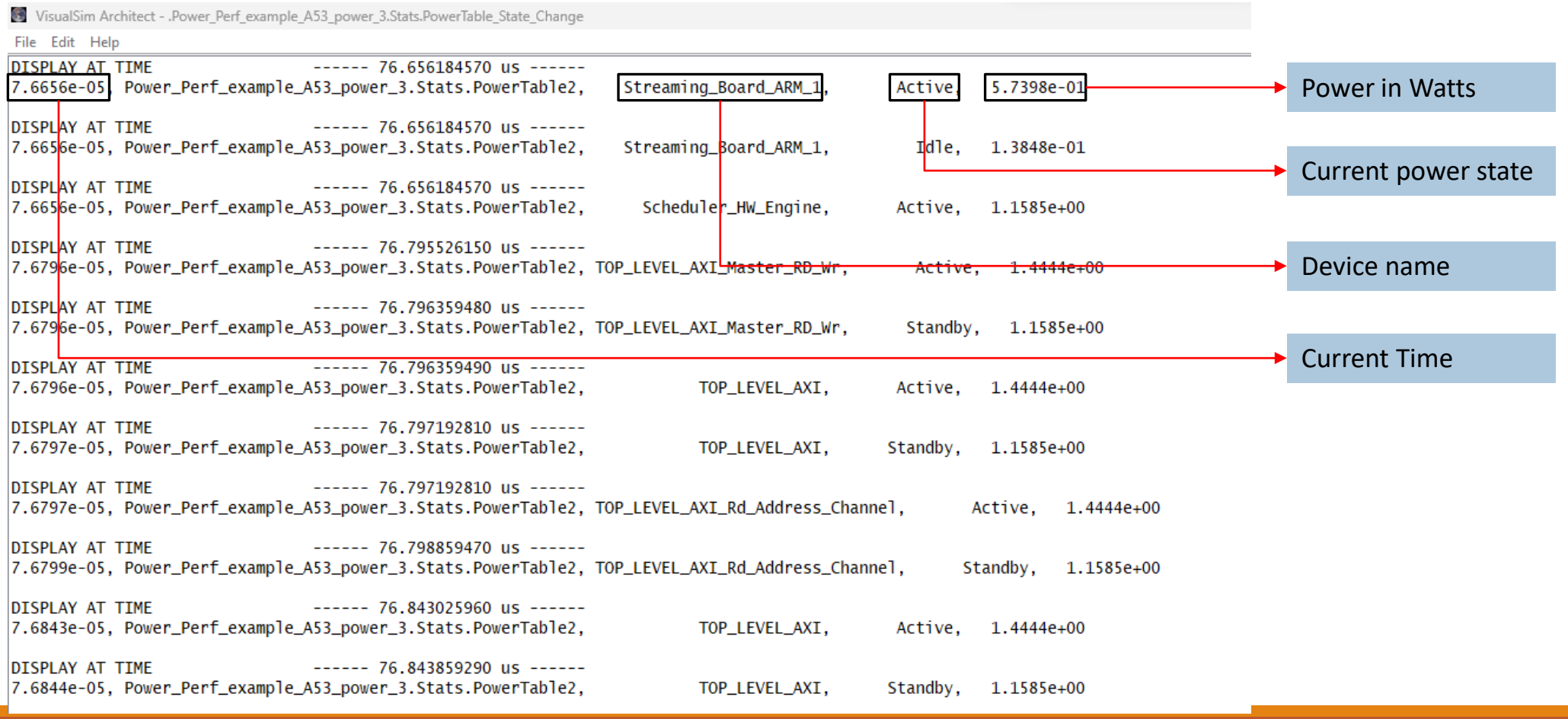
Device	Current	Average	Active	Standby	Wait	Idle
Scheduler_HW_Engine	0.75	0.2008084699088	1.02	0.75	0.375	0.0
Streaming_Board_ARM_1	0.4355	0.1444355104106	0.4355	0.038025	0.019015	0.0
Streaming_Board_Ext_SDRAM	0.06222	0.0901663640044	1.464	0.06222	0.03111	0.0
TOP_LEVEL_AXI	0.019065	0.0197685981321	0.305	0.019065	0.0095325	0.0
TOP_LEVEL_AXI_Master_RD_Wr	0.019065	0.0197686081975	0.305	0.019065	0.0095325	0.0
TOP_LEVEL_AXI_Rd_Address_Channel	0.019065	0.0197709597014	0.305	0.019065	0.0095325	0.0
TOP_LEVEL_AXI_Wr_Address_Channel	0.019065	0.0	0.305	0.019065	0.0095325	0.0
Total	1.32398	0.5138358997584				

PowerStats_Power_Perf_example_A

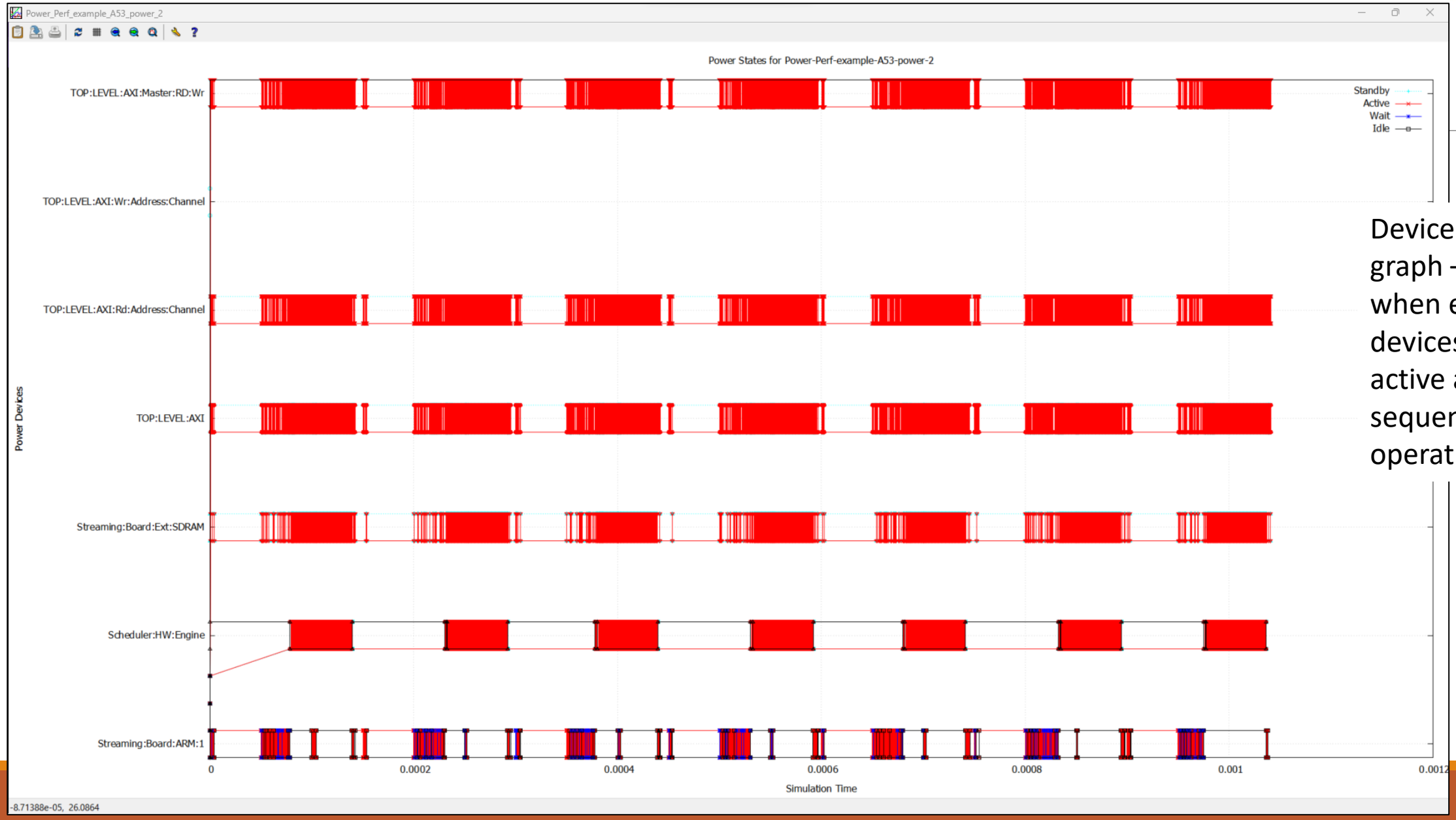
File Edit View

```
Power_Manager  (Power_Perf_example_A53_power_2.Stats.Manager_1)
Hier File Name (PowerStats_Power_Perf_example_A53_power_2_Stats_Manager_1_Hier.txt)

Device,                                 Cumulative,             Average
Streaming_Board_ARM_1,                  1.15234E-4,             0.05761
Scheduler_HW_Engine,                    3.93183E-4,             0.19659
Streaming_Board_Ext_SDRAM,              1.53386E-4,             0.07669
TOP_LEVEL_AXI,                          3.90109E-5,             0.01950
TOP_LEVEL_AXI_Rd_Address_Channel,       3.90109E-5,             0.01950
TOP_LEVEL_AXI_Master_RD_Wr,             3.90109E-5,             0.01950

TOTAL,                                  7.78837E-4,             0.38941
GrandTOTAL,                             7.78837E-4,             0.38941
```

Power State Transition Log – PowerTable 3rd port output



GNU Plot – Detailed power plot



Device activity graph – identify when each of the devices are active and their sequence of operation.

Power Management for Custom Blocks using Regex

Manager Setup for Custom Blocks

Manager_Setup:

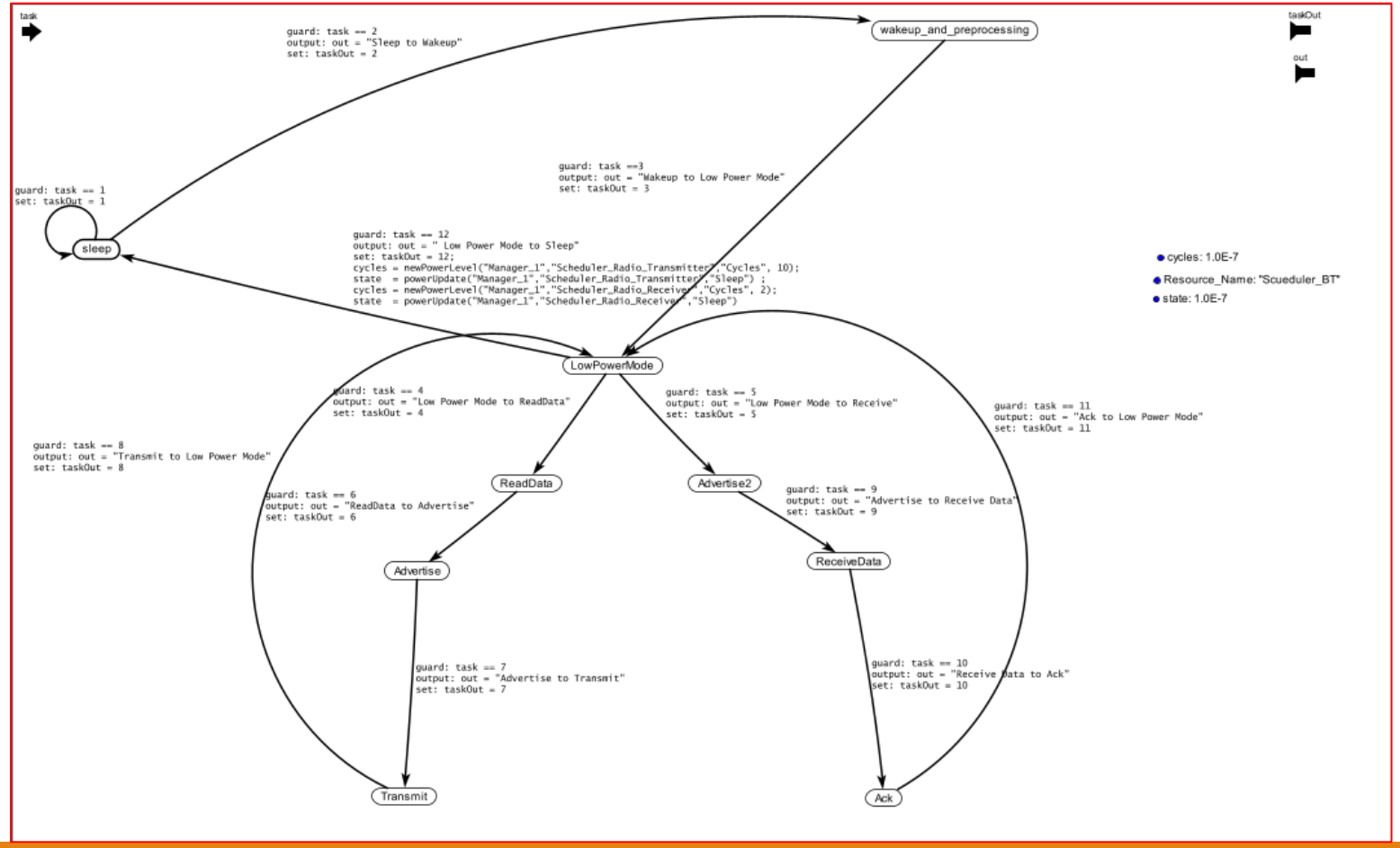
```
/* Power_Table.  First row contains Column Names, expressions valid for entries except Device Name.
                 where "Scheduler_" or "STR_" + BlockName; Processor, Bus, DRAM = Architecture_Name + "_" + BlockName
--------Device Name-------  ---------Power States------  -----Operating States------  --toActive--  --Speed--  --Exist-- */
Architecture_Block          Standby  Active  Wait  Idle  Existing  OffState  OnState    t_OnOff        Mhz        Volts    ;
UCIe_Link_Delay_1_to_TX           70.0     300.0   0.0   0.0   Standby   Standby   Active     Cycle_t       1000.0     1.0     ;
UCIe_Link_Delay_1_From_RX         70.0     300.0   0.0   0.0   Standby   Standby   Active     Cycle_t       1000.0     1.0     ;
```

Regex Used :

```
stateChange("Manager_1",UCIe_Switch_Name+"_Link_Delay_"+Port_Number+"_to_TX","Existing","Active")
WAIT(Link_Setup_Delay_Per_Transfer)
WAIT(Link_Delay_First_Transfer)
stateChange("Manager_1",UCIe_Switch_Name+"_Link_Delay_"+Port_Number+"_to_TX","Existing","Standby")
```

Defining Power States using State Diagram

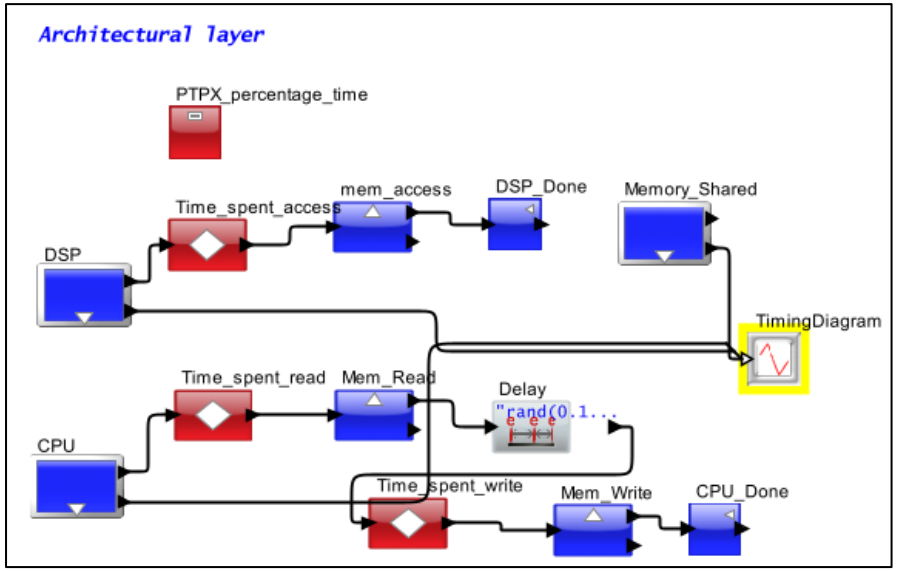
Control System Design – state machines

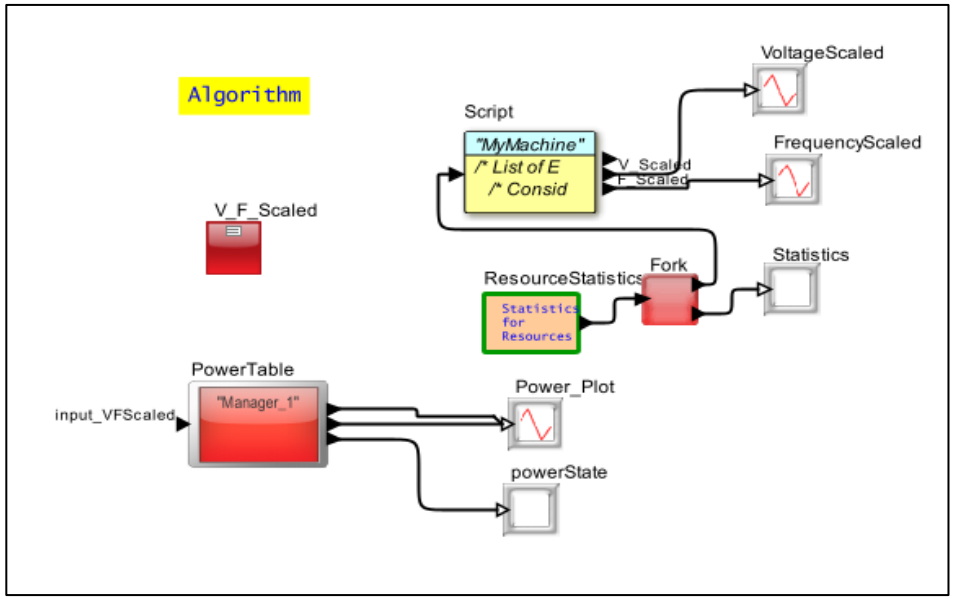


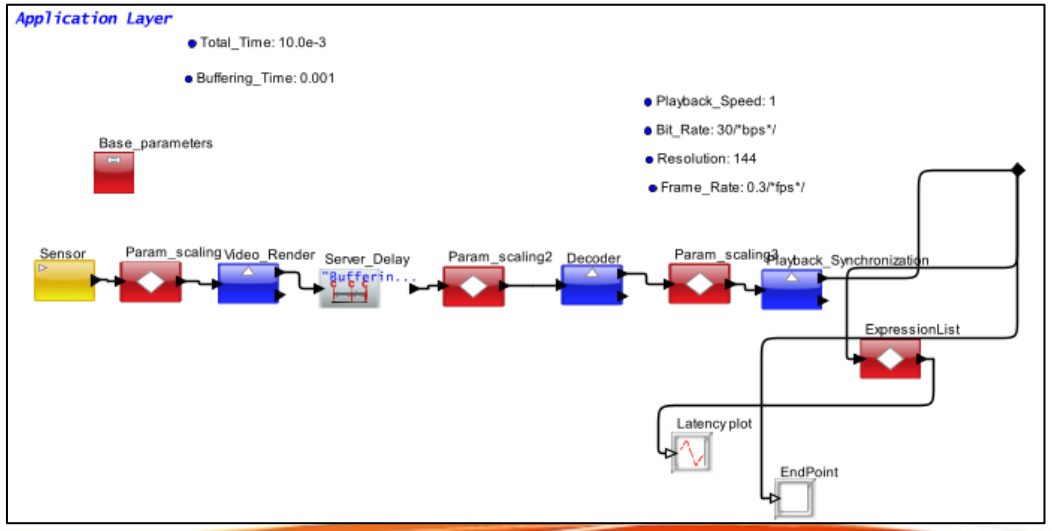
Bluetooth module in IoT Demo model

Dynamic Power Analysis

Dynamic Power Analysis







Architectural Layer -> 2 Cores and a shared memory

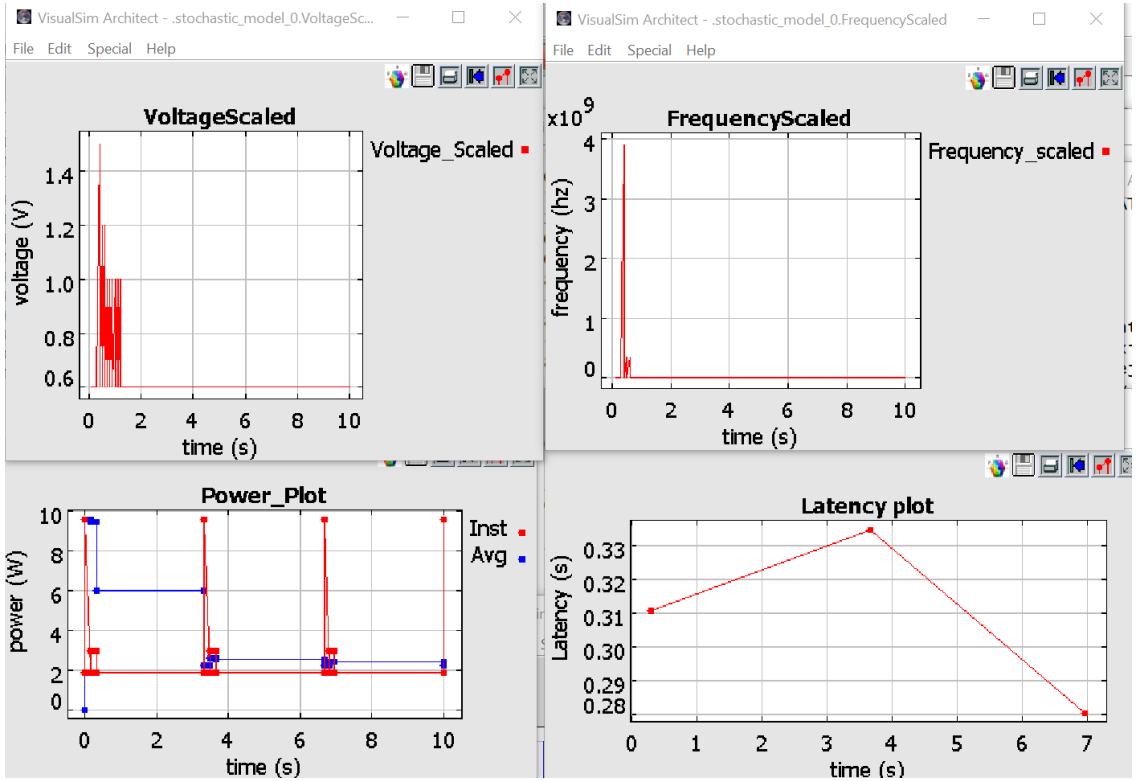
Model location: Attached

Algorithm → Script is used to track Utilization_Mean and throttle Voltage and Frequency based on that

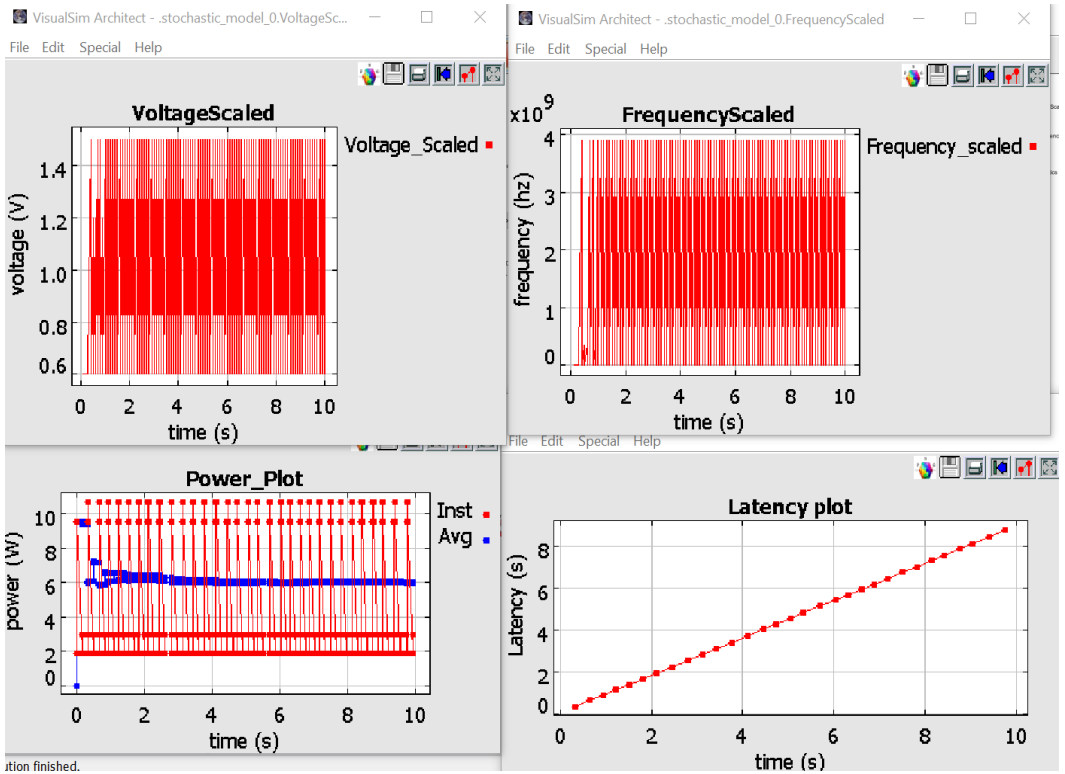
Application Layer -> Each Task takes certain percentage time on the Resource, determined by PTPX input data

Results

Frequency and Voltage Scaling Up/down based on Core Utilization



Frame_Rate = 0.3fps



Frame_Rate = 30fps

Cumulative Power Report

VisualSim Architect - file:/C:/VisualSim/VisualSim2410_64/V. . ._stochastic_model_0_Manager_1_Hier.txt

File Edit Help

Power_Manager (stochastic_model_0.Manager_1)
Hier File Name (PowerStats_stochastic_model_0_Manager_1_Hier.txt)

Device,	Cumulative,	Average
Scheduler_CPU,	10.01141,	1.00114
Scheduler_DSP,	6.16701,	0.61670
Scheduler_Memory,	6.16172,	0.61617
TOTAL,	22.34015,	2.23401
GrandTOTAL,	22.34015,	2.23401

Frame_Rate = 0.3fps

Power_Manager (stochastic_model_0.Manager_1)
Hier File Name (PowerStats_stochastic_model_0_Manager_1_Hier.txt)

Device,	Cumulative,	Average
Scheduler_CPU,	47.22800,	4.72280
Scheduler_DSP,	6.21912,	0.62191
Scheduler_Memory,	6.47172,	0.64717
TOTAL,	59.91885,	5.99188
GrandTOTAL,	59.91885,	5.99188

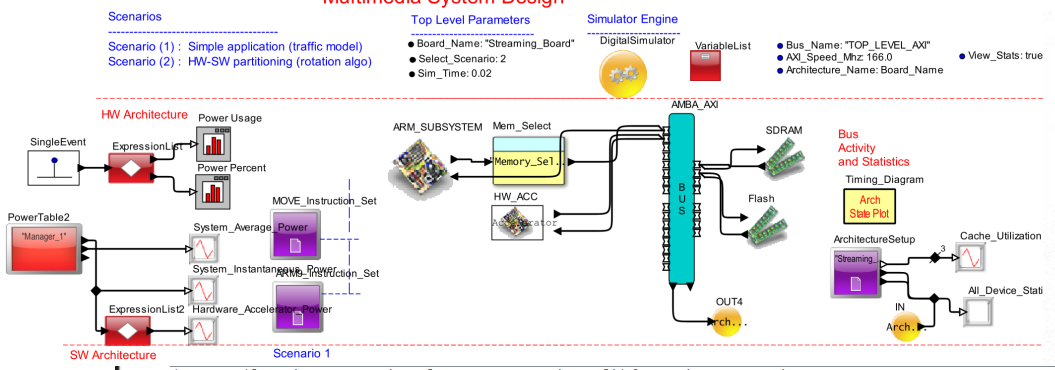
Frame_Rate = 30fps

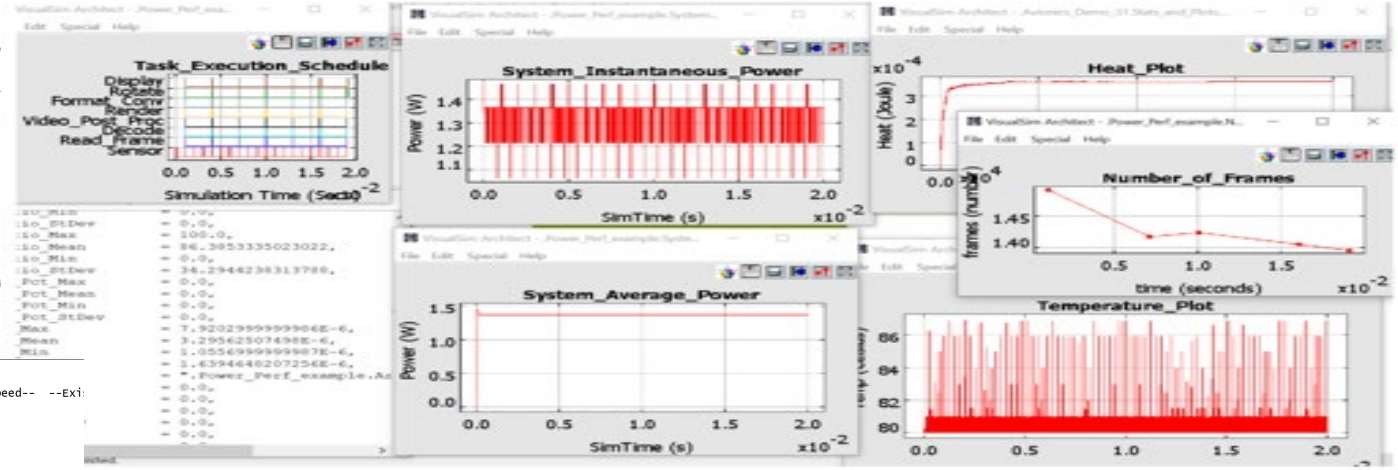
Results and Downstream Integration

Power Modeling

MIRABILIS

Observe the Power, Performance and Thermal Impact

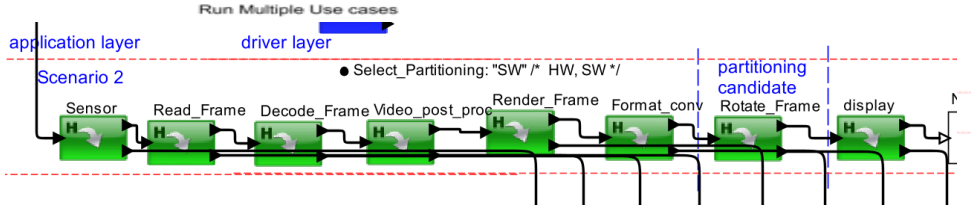





```
/* Power_Table.  First row contains Column Names, expressions valid for entries except Device Name.

--------Device Name-------  ---------Power States------  -----Operating States------  ----------State Transitions---------  --Speed--  --Exi
    Architecture_Block           Standby  Active  Wait     Idle  Existing  OffState  OnState  t_OnOff      Mhz       Volts    ;
Streaming_Board_ARM              75.0     200.0    100.0    100.0  Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Streaming_Board_MOVE             25.0     100.0    0.0      0.0    Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Streaming_Board_Cache            50.0     150.0    0.0      0.0    Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Streaming_Board_HW_ACC           10.0     100.0    0.0      0.0    Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Streaming_Board_HW_ACC_Bus       50.0     150.0    0.0      0.0    Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Streaming_Board_AHB_Bus          50.0     150.0    0.0      0.0    Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Streaming_Board_RAM_Bus          50.0     150.0    0.0      0.0    Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Streaming_Board_ROM_Bus          50.0     150.0    0.0      0.0    Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Streaming_Board_Ext_SDRAM_Bus    50.0     150.0    0.0      0.0    Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Streaming_Board_Ext_FLASH_Bus    50.0     150.0    0.0      0.0    Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Streaming_Board_Ext_SDRAM       150.0     350.0    0.0      0.0     Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Streaming_Board_Ext_FLASH       150.0     350.0    0.0      0.0    Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Scheduler_EBU_Scheduler          75.0     250.0    0.0      0.0     Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
Scheduler_LMU_Scheduler          75.0     250.0    0.0      0.0    Standby   Standby   Active   1.0e-8     1000.0     1.0     ;
STR_AXI_ARM_Rd_Data_Channel      70.0     300.0    0.0    0.0    Standby   Standby   Active     0.0          1000.0     1.0     ;
STR_AXI_ARM_Wr_Data_Channel      70.0     300.0    0.0    0.0    Standby   Standby   Active     0.0          1000.0     1.0     ;
AXI_ARM                          70.0     300.0    0.0    0.0    Standby   Standby   Active     0.0          1000.0     1.0     ;
AXI_ARM_Rd_Address_Channel       70.0     300.0    0.0    0.0    Standby   Standby   Active     0.0          1000.0     1.0     ;
AXI_ARM_Wr_Address_Channel       70.0     300.0    0.0    0.0    Standby   Standby   Active     0.0          1000.0     1.0     ;
STR_TOP_LEVEL_AXI_Rd_Data_Channel    70.0     300.0    0.0    0.0    Standby   Standby   Active     0.0          1000.0     1.0     ;
STR_TOP_LEVEL_AXI_Wr_Data_Channel    70.0     300.0    0.0    0.0    Standby   Standby   Active     0.0          1000.0     1.0     ;
TOP_LEVEL_AXI                    70.0     300.0    0.0    0.0    Standby   Standby   Active     0.0          1000.0     1.0     ;
/* Async_State_Change.  First row contains Column Names, expressions valid for entries except Device Name.
```

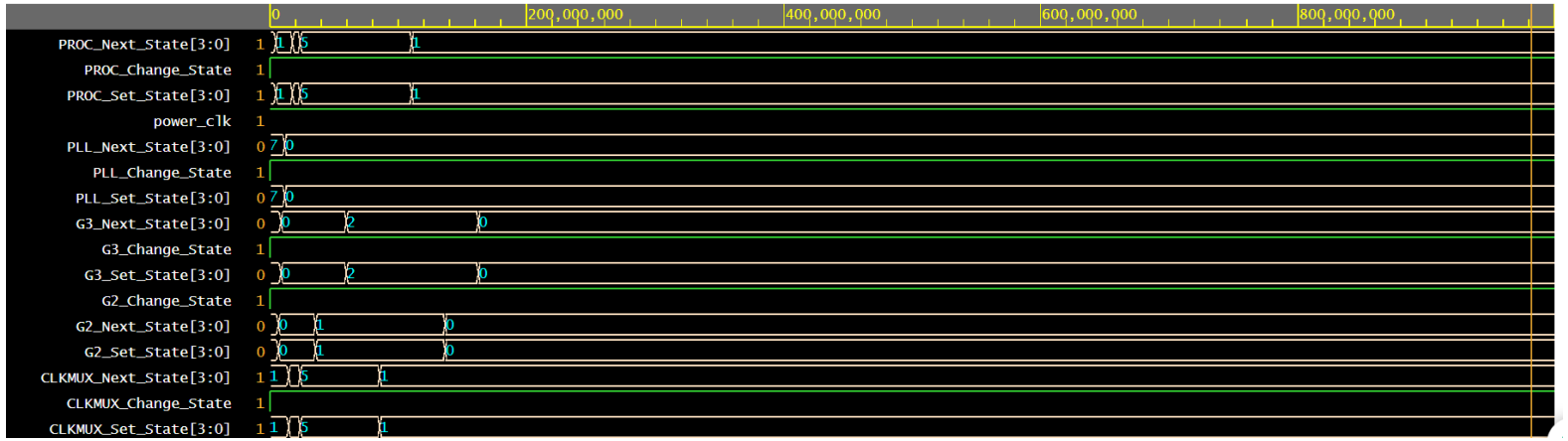
Vary the parameters

- Hardware partition for a specific task
- Change BUS speed
- Change cache-hit ratio




```
create_power_domain -name PD_PROC -elements {PROC}
create_power_domain -name PD_G2 -elements {G2}
create_power_domain -name PD_G3 -elements {G3}

#creating supply ports
# Use Architecture_Block name. Eg: VDD_ARM
create_supply_port -port VDD_PROC
creatw_supply_port -port VSS_PROC


#creating supply net for PROC

create_supply_net PWR -domain PD_PROC
create_supply_net GND -domain PD_PROC

#connecting supply port to supply net
connect_supply_net PWR -ports {VDD_PROC}
connect_supply_net GND -ports {VSS_PROC}

#reusing the nets for other blocks since "Volts" is same
create_supply_net PWR -reuse -domain PD_PLL
create_supply_net GND -reuse -domain PD_PLL

create_supply_net PWR -reuse -domain PD_CLKMUX
create_supply_net GND -reuse -domain PD_CLKMUX

create_supply_net PWR -reuse -domain PD_G2
create_supply_net GND -reuse -domain PD_G2

create_supply_net PWR -reuse -domain PD_G3
create_supply_net GND -reuse -domain PD_G3

#Power switch for switched domain
create_power_switch SW \
```

Export UPF and Testbenches for downstream use



UPF file and System Verilog files

- High level UPF containing Domain and Voltage information Power test bench based on the state transitions of the blocks in the model) are also generated in the model Results Directory.
- To **enable, select the Generate_UPF_TB option in the power Table.**

UPF File

Power domains added based on 'Domain' column in powerTable

Supply nets and ports based on 'Voltage" column in powerTable

Power switch added by default for all domains – swctrl can be used in testbench to enable or disable the switch

Value from "Volts" will be added for Active state of the port. Other values are default

Power state table based on all the supply ports

```
create_power_domain PD_Top -include_scopecreate_power_domain \
-name PD_1_1.0 -elements {"Scheduler_0"}
create_power_domain PD_Top -include_scopecreate_power_domain \
-name PD_2_1.0 -elements {"Scheduler_1","Scheduler_2"}
create_power_domain PD_Top -include_scopecreate_power_domain \
-name PD_3_1.0 -elements {"Scheduler_3"}
create_supply_port -port VDD_1.0 -direction in -domain PD_Top
create_supply_port -port VSS_0.0 -direction in -domain PD_Top
create_supply_net VDD_1.0 -domain PD_Top
create_supply_net VSS_0.0 -domain PD_Top
connect_supply_net VDD_1.0 -ports VDD_1.0
connect_supply_net VSS_0.0 -ports VSS_0.0

#Power switch for switched domain
create_power_switch SW \
-domain PD_1_1.0 \
-output_supply_port {swout VDDsw}\
-input_supply_port {swin Pwr} \
-control_port {swctrl} \
-on_state {SWon swin swctrl} \
-off_state {SWoff !swctrl}

#adding port states
add_port_state VDD_1.0 \
-state {Active=1.0, Standby=0.8, Wait=0.8,IDLE=0.7}

add_port_state VSS_PROC \
-state {Active 0.0}

add_port_state SW/swout
-state {Active 1.0} \
-state {Standby 0.7}

create_pst pwr_state_table \
-supplies {VDD_1.0 SW/swout VSS_0.0}
```

VCD Output from System Verilog Files

VCD file having input and output signal transitions for that model can be generated by using pmu.sv and testbench.sv in any of the opensource or commercial EDA tools that support System Verilog

The user can observe the States that each of the Resources were in throughout the simulation.

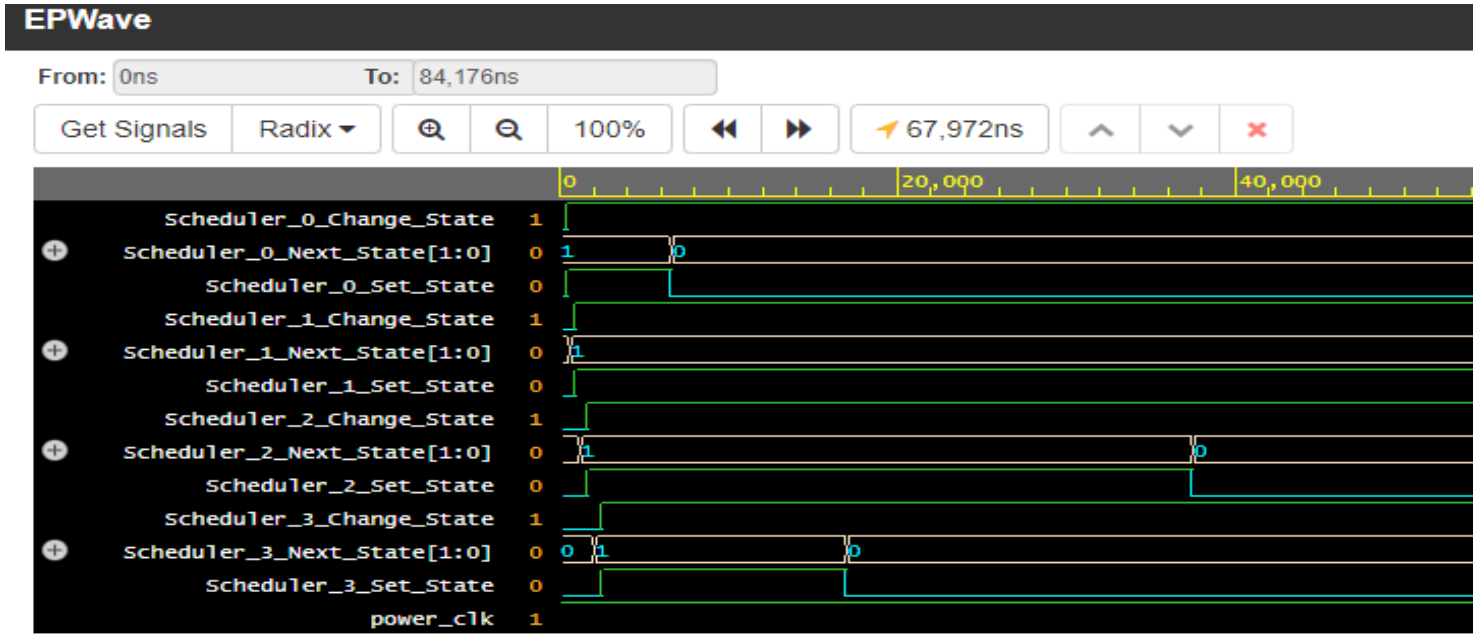
Signals:

1. Change_State = when it is high, the Power Manager applies the transition from current state to next state for that Block

2. Next_State = This signal holds the binary equivalent of the next state (Example: 00, 01, 10,11 – active, standby, wait, idle)

3. Set_State = This signal will indicate that the transition is complete successfully to the new intended state

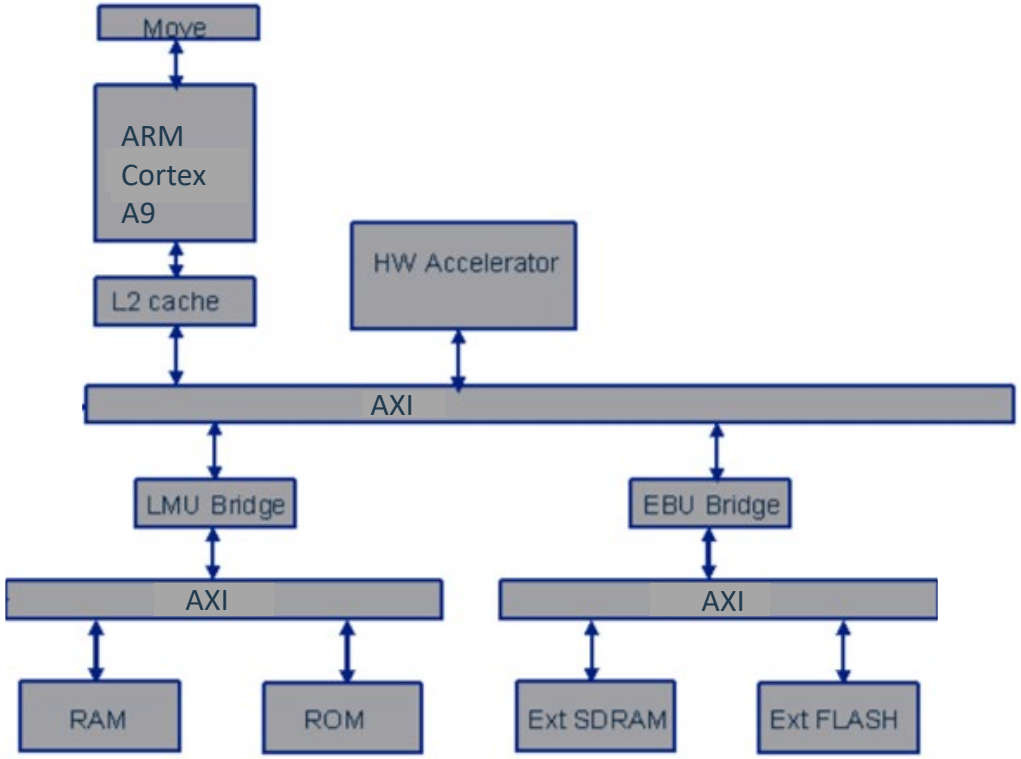
The user can observe the delay between transitions by zooming in the waveform.



Note: These files can be useful for downstream integration in the RTL power verification environment.

Power Perf Tradeoff Analysis

SoC Architecture for Media Application



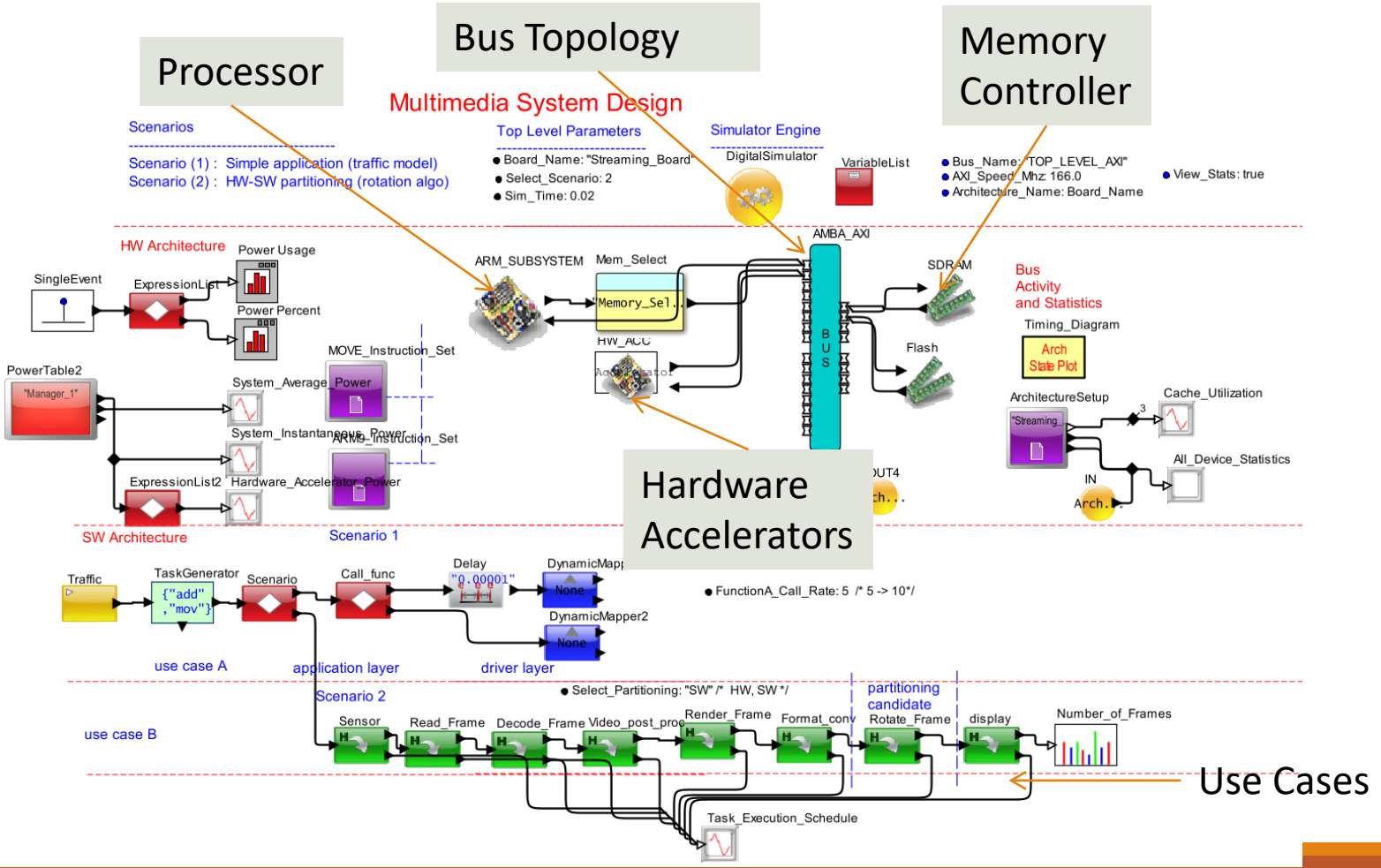
Target

SoC Power Target < 1.5W

No. of Frames in 20 msec>= 18K

Power and Performance Trade-off must be done concurrently

Model SoC Architecture and Map the MPEG Application



MPEG Application

IP or ARM level

- Evaluate pipeline stages
- Width, Speed
- Number of execution units, Levels of cache

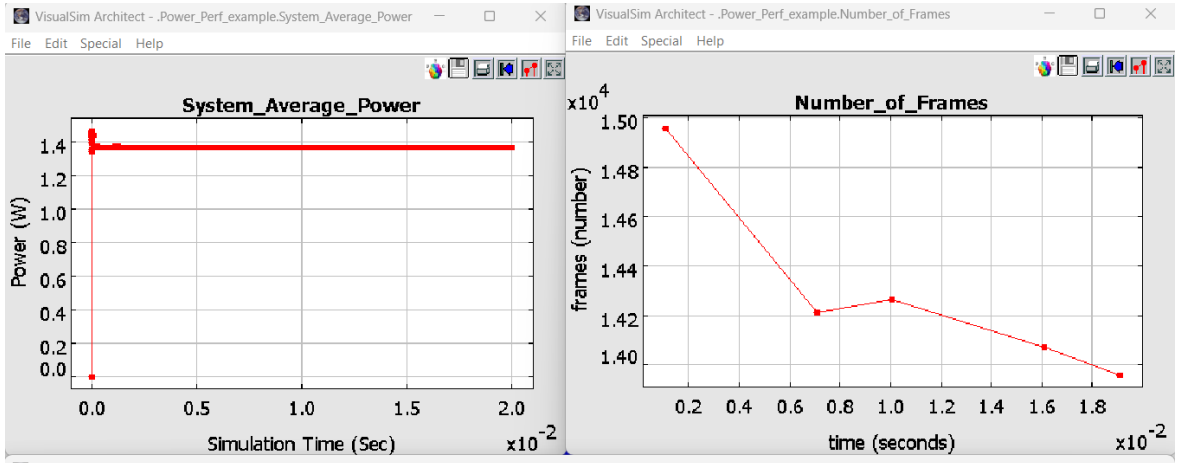
SoC

- Number of ARM cores
- Accelerators
- Cache memory hierarchy and coherence

System level

- Development of an IoT device, ECU or an integrated platform

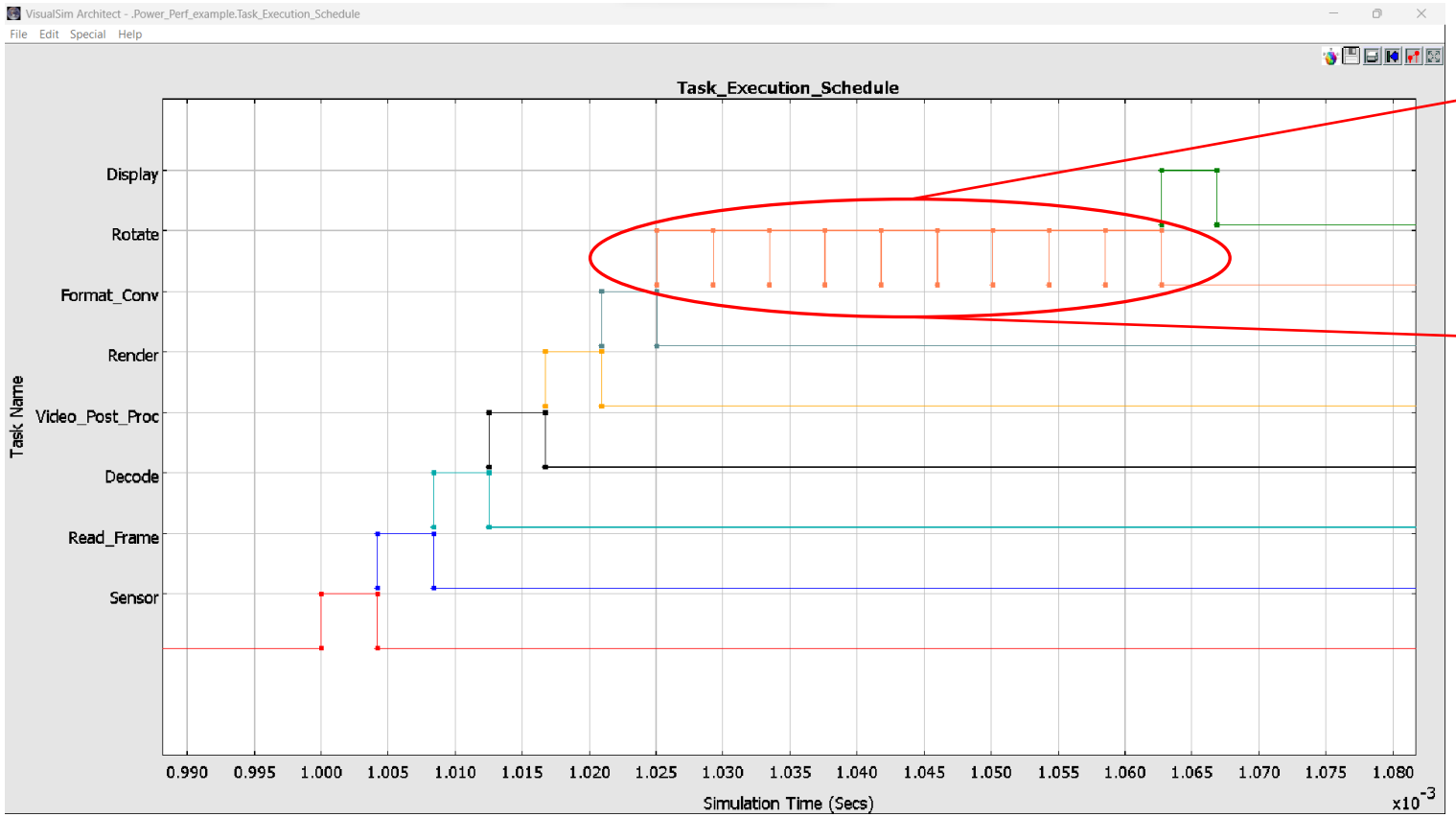
CASE 1: Run all tasks on SW(on A9 core)



Observations:

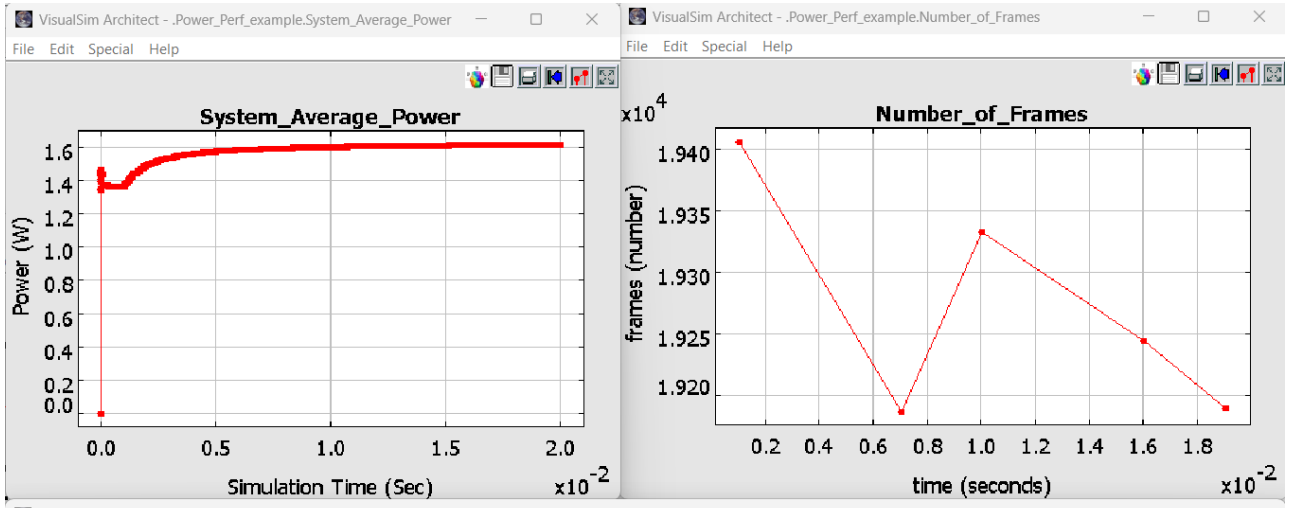
1. Avg power consumption within requirements (<1.5 W)
2. Performance requirement not achieved (Only a max of 15K frames)

Sequence diagram



Rotate Frame task is found to be resource intensive

CASE 2: Run Rotate Frame task on HW Acc



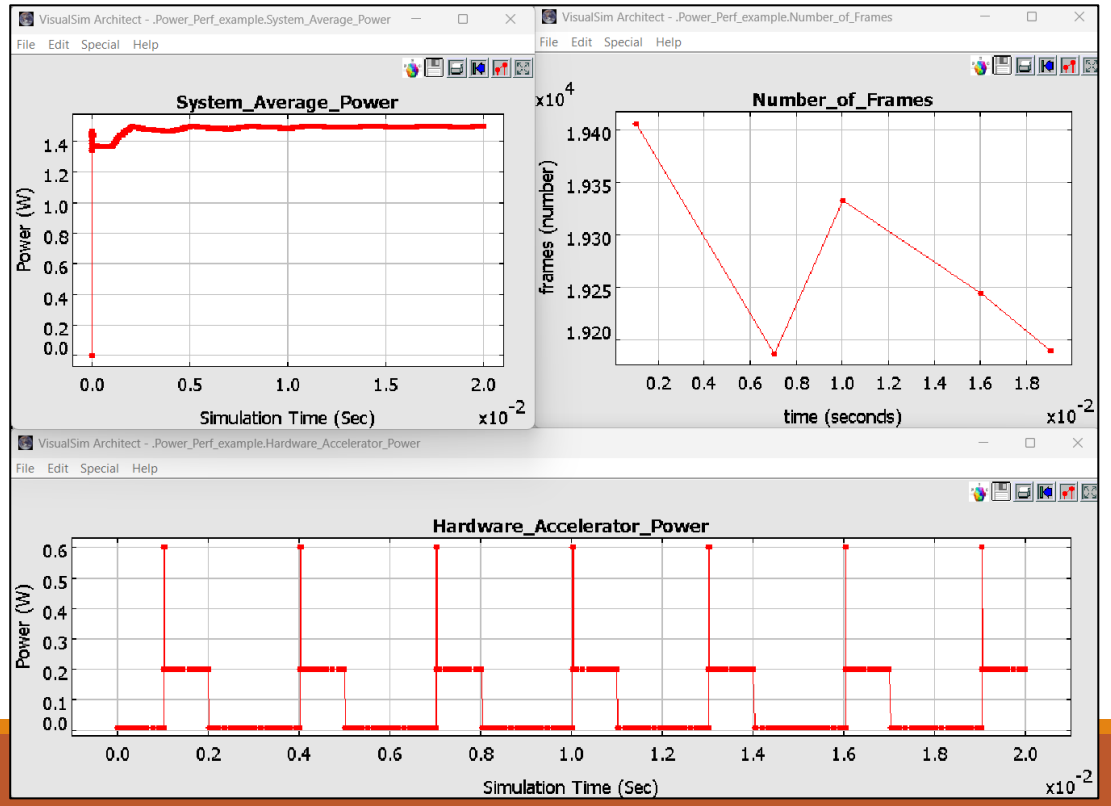
- The Avg power consumption is greater than the threshold
- Options for the Architect:
  - Use HW accelerator from another vendor
  - Use same HW accelerator, but apply power management
    - From the power plot for HW accelerator, it could be observed that the HW accelerator is active only for a short period of time

Observations:

1. Avg power consumption requirement not met (>1.5 W)
2. Performance requirement achieved (max of 19 K frames)

CASE 3: Run Rotate Frame task on HW Acc + Power management

```
Delay_to_Change_State:  /* Async_State_Change.  First row contains Column Names, expressions va

--------Device Name-------  ------------Time State--------- */
    Architecture_Block      State     Time_or_Express  Next ;
 Scheduler_HW_Engine         Standby   1.0e-3            Idle ;
```



Power management being applied across HW accelerator -> If Hardware Accelerator is in standby state for more than 1 msec, then it is moved to Idle state

Observations:

1. Avg power consumption requirement met (<1.5 W)
2. Performance requirement achieved (max of 19.4K frames)