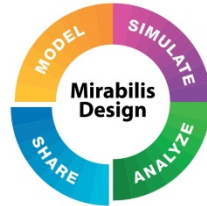


REFERENCE GUIDE

INTRODUCTION TO THE CONCEPTS AND USING VISUALSIM



MIRABILIS DESIGN INC.

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1 Scope and Purpose of the Document

1.1 Introduction

Mirabilis Design provides systems engineering solutions for performance analysis, power estimation, and architecture exploration of electronics and real-time software. Mirabilis' product **VisualSim** is used for performance, functional, and power exploration of network of systems, large systems, sub-systems, components (IC, SoC, FPGA, and boards) and real-time software. VisualSim models are constructed in a graphical block diagram editor using a parameterized modeling blocks library.

1.2 Scope


This document provides the information required to enable the reader to construct system models, execute simulations, and analyze the results with an intent to optimize the specification. This document explains the basic components in this framework, the simulator, modeling language, and provides an overview of the libraries.

The intended audience for this document is an engineer or researcher who wishes to construct models in VisualSim, debug these models, and conduct analysis. The goal of the exploration is to architect the right product, that is one which minimizes product failures and has not been over or under designed.


2 Starting VisualSim

2.1 Running VisualSim Architect

To start Architect, do one of the following:

- ⇒ Double-click Architect  icon on the Window or in the Application Menu.
- ⇒ Double-click VisualSim.bat (WINDOWS) or VisualSim.sh (UNIX) in the VisualSim directory viewer.
- ⇒ From a Command-line or system-prompt or shell window, go to the VisualSim install and type VisualSim.bat (Windows) and VisualSim.sh (UNIX).

To start the Post Processor, do the following:

- ⇒ Double-click the Post Processor  icon in the Window or in the Application Menu.
- ⇒ Double-click PostProcessor.bat (WINDOWS) or PostProcessor.sh (UNIX) in the Post Processor directory.
- ⇒ From a Command-line, system-prompt or shell window, go to the Post Processor install and type PostProcessor.bat (Windows) or PostProcessor.sh (UNIX).

2.3 Running VisualSim Explorer

To start VisualSim Explorer, do the following:

1. The user needs to start the License Server located in the Web Server.
2. To start the License Manager, locate the install directory and navigate to VS_LM.
3. From a Command-line, system-prompt or shell window, type StartServer.bat (Windows) or StartServer.sh (UNIX).

4. The user can access html pages on this system by opening the page in their respective browser.

The Interfaces > Export to Web can be used to export the model for use in the browser.

3 VisualSim Products, Editors, and Tools

3.1 Block Diagram Editor

The Block Diagram Editor (BDE) is the main editor in the VisualSim Architect environment. Users construct, debug, validate, and optimize the models of their system in this environment. Simulations to validate the model and get early feedback on the architecture are conducted from the Editor. After the model is stable and simulations are restricted to parameter changes, the Batch Mode can be used for large scale system analysis.

In the BDE, select blocks from the core libraries, place them on the BDE canvas, and then connect the blocks to represent the functions of the system. Group the various functions of the system to form a hierarchical model representing a sub system. Make use of hierarchy and aggregation to manage the complexity of large systems. Include adjustable parameters in any model so as to easily modify the system performance as per the requirement. Users can alter random number seeds to investigate system stability through analysis of variance. Prior to simulation, assign each parameter a value to execute a simulation over a range of conditions. Moreover, easily incorporate measured characteristics of the system, such as traffic traces, into VisualSim models.

3.1.1 Menu Commands

Menu	Sub Menu	Explanation	Shortcut
File	Open File	Select and open an existing model, text or html file on a local or networked disk.	Ctrl+O
	Open URL	Select and open an existing model, text or html file using the URL address. The file can be located anywhere on the Internet.	

Menu	Sub Menu	Explanation	Shortcut
	New	Open a new Block Diagram Editor (BDE), Icon Editor, FSM-Controller, FiniteStateMachine, Text Editor, Expression Evaluator or Tcl Evaluator.	
	Save	Save the active file with its current file name, location, and format.	Ctrl+S
	Save as	Save by opening a window to change the file name, location or format.	
	Print	Print the active file. User can change the print options.	Ctrl+P
	Import	Import an existing file.	
	Export	Export to png, gif, Web Page (Different from the dynamic Export to HTML), and Save in Library (Saves the entire model content as a library in User_Library).	
	Recent Files	View a list of the last 10 files that are saved for you to easily select.	
	Close	Close the active window.	Ctrl+W
	Exit	Close the application.	
View	Block Diagram Editor	Switch from the existing window to Block Diagram Editor window. This feature is disabled.	

Menu	Sub Menu	Explanation	Shortcut
	Simulation Cockpit	View Simulation Cockpit of the model to modify the parameters and to run the model. This feature is being disabled from the next release.	
	JVM Properties	View the Java Virtual Machine Properties.	
	Zoom In	View a smaller part of the diagram in the screen view.	Ctrl+Shift+Equal Symbol
	Zoom Reset	Reset the screen view to the original size.	Ctrl+M
	Zoom Fit	Fit the content of the block diagram into the viewable page.	Ctrl+Shift+Minus Symbol
	Zoom Out	View a larger part of the diagram in the screen view.	Ctrl+Minus Symbol
	Full Screen	Hide the menu and folder bar to display the model to cover the full screen.	
Edit	Undo	Last action disappears from the screen.	Ctrl+Z
	Redo	Repeats your last action.	Ctrl+Y
	Cut	Removes the selection from the active file and places it on the clipboard.	Ctrl+X
	Copy	Copies the selection to the clipboard.	Ctrl+C

Menu	Sub Menu	Explanation	Shortcut
	Paste	Inserts the selected contents to the clipboard.	Ctrl+V
	Send to Back	When the blocks are overlapped, select the required block, and click Send to Back to place the block behind the adjacent block.	Ctrl+B
	Bring to Front	When the blocks are overlapped, select the required block and click Bring to Front to place the block in front of the adjacent block.	Ctrl+F
	Edit Preferences	Used to define graphical and model-level properties. Currently there are only a few properties predefined.	
Graph	Find	Search for a keyword among the model blocks, parameters, expression, and memories.	
	Automatic Layout	Rearranges the layout of the blocks, connectivity, and relations in the model. DO NOT USE. THIS IS A PROTOTYPE	Ctrl+T
	Save in Library	Saves the current block diagram as a Library. The model must be saved for this feature to be used.	
	Import Library	Open an XML file containing the list of library items and add it to the Folder structure on the left. The current version does not remember the update when the tool is closed.	

Menu	Sub Menu	Explanation	Shortcut
	Instantiate Class	<p>Select the class file to be placed in the BDE. This can be a Java class or an XML class. Use the File Selector to select the file. The file must be located in a directory that is within the CLASSPATH.</p> <p>Example: VisualSim.actor.lib.AbsoluteValue</p>	
	CreateHierarchy	<p>Select the blocks, connections, and parameters and create a Hierarchical_Block.</p> <p>Note: All parameters that are used in the selected blocks must be included in the selection; else multiple errors are generated. In some cases, the creation may have errors. All the connected wires must be selected or the input/output ports for this hierarchical block will be generated automatically. All the created ports are consolidated at the top-left of the screen within the hierarchical block.</p>	
	Xml Comparator	Compares the current Model with another model file.	
	New input port	Places an input port in the BDE.	
	New output port	Places an output port in the BDE.	
	New input/output port	Places an input/output port in the BDE.	

Menu	Sub Menu	Explanation	Shortcut
	New input multiport	Places an input multiport in the BDE.	
	New output multiport	Places an output multiport in the BDE.	
	New input/output multiport	Places an input/output multiport in the BDE.	
	New Relation	Places a Relation (black diamond) in the BDE.	
Debug	Listen to Simulator	This is a dialog window that is linked to the Digital Debug setting of the Digital Simulator. This displays the block activity and usage statistics.	
	Animate Execution	Set time to view the dynamic operation of the system model. S Model is animated by highlighting the executing block.	
	Stop Animating	Turns-off the animation.	
Interface	Generate Wrapper	This is used with the C, Application Interface, SystemC, and Verilog links. This generates the required code files to interface with the third-party code and simulator. A single selection generates a wrapper for all the links.	

Menu	Sub Menu	Explanation	Shortcut
	Compile Wrapper	This goes through a sequence to compile the code generated by “Generate Wrapper” along with the user code. A single selection compiles all the blocks that have wrappers generated.	
	Export to Html	This Menu item enables the user to open any model and generates an html document. The tool generates a separate page for each Hierarchical level. The page contains all the parameters, images, blocks, and any documentation described using Annotations. At the bottom of each page, the Applet containing the model is included. On the top page of the model, the simulation is executable. For all other pages, the view of the model alone is provided. When this export occurs, a separate html page is created for each Hierarchical block. The model that shows on these pages will not simulate. The top-level BDE that is exported will have the simulation ability.	
Help	About	View a brief description about the company and product.	
	Help	Opens the starting page of the documentation.	

3.1.2 Details of Menu and Toolbar Operation

3.1.2.1 Open a New Window

(Includes Block Diagram, Icon Editor, Expression Evaluator, TCL Evaluator, and Text Editor)

1. In your Mirabilis Design VisualSim program, click **File > New**.
2. From this menu, select the window of choice – Block Diagram, Icon Editor, Expression Evaluator, TCL Evaluator or Text Editor.
3. A new window is displayed.

3.1.2.2 Existing Window (Model, Hierarchical Block, and URL)

1. In your Mirabilis Design VisualSim program, click File, and then click either **Open File** or **Open URL**.

For a File

- a) In the **Look in** list, click the drive, folder, or Internet location that contains the files.
- b) In the folder list, locate and open the folder that contains the file.
- c) Select the file, and then click **Open**.

For a URL

- a) In the text window, type the full path to the Internet location.
- b) Click OK.

In addition, quick keys can be used:

1. CTRL+O – To open a file.
2. CTRL+U – To open an Internet location.

3.1.2.3 To open recently opened models – Recent Files




You can select from a list of most recently saved models.

3.1.2.4 Saving Options (Model, Block Diagram, FSM, and Text Editor)

1. To quickly save a document, click **Save** on the Standard Toolbar or CTRL+S or click File and then click Save.
2. To save the models in a different location, use the procedure below.
 - a. On the File menu, click **Save As**.
 - b. In the File name box, enter a new name for the file.
 - c. Click **Save**.

3.1.2.5 Editing Options (Model, Block Diagram, FSM, and Text Editor)

To move or copy a single item:



1. Select the item you want to move or copy.
2. Do one of the following:
 - ⇒ To move the item, click  **Cut** on the Standard toolbar.
 - ⇒ To copy the item, click  **Copy** on the Standard toolbar.
3. If you want to move or copy the item to another document, switch to the document.
4. Click where you want the item to appear.
5. Click  **Paste** on the Standard toolbar.

Alternate methods:

- Use the Cut, Copy, and Paste functions in the Edit Menu.

- Use Cut (CTRL+X), Copy (CTRL+C) and Paste (CTRL+V).





To undo or redo an operation on a model:

1. Click  undo or  redo in the Edit Menu or from the Toolbar.

To delete a block or link:





1. Select the block, state, link or transition you want to delete.
2. Press DELETE on keyboard, or click Delete or on the Edit menu, click Delete.

3.1.2.6 Zoom In or Out of a model

1. You can “Zoom In” to get a closer view of the model or FSM or “zoom out” to see more of the hierarchy at a reduced size.
2. Click **Zoom In**  and **Zoom Out**  on the standard toolbar.
3. In addition, you can **Zoom To Fit** to view the entire model or FSM on the screen.
4. Click **Zoom To Fit**  on the standard toolbar
5. Finally you can also **Zoom Reset** to bring the view back to the previously saved state.
6. Click the **Zoom Reset**  on the standard toolbar.
7. In addition to the standard toolbar option, you can also click **View** on the Menu and select the item.
8. Finally, you can also use the shortcut keys – Zoom in (CTRL+SHIFT+=), Zoom Out (CTRL+-), Zoom Reset (CTRL+=), and Zoom to Fit (CTRL+F) to achieve the same result.

3.1.2.7 Stop and Resume

The simulation can be executed from the BDE window also. These operations are similar to the operations in the Simulation Cockpit:

- ⇒ Click **GO**  to start the simulation.
- ⇒ Click **STOP**  to terminate the simulation and not continue further.
- ⇒ Click **PAUSE**  to temporarily halt the simulation.
- ⇒ Click **RESUME**  to restart the simulation from the point where it was paused earlier.

The simulation can be stopped at any time. The displays can be viewed. The simulation can be resumed from that point forward.

3.1.2.8 Editorial Functions

VisualSim provides the following Editorial functions:.

Automatic Layout: This modifies the layout of the blocks and parameters in the current window. Do not use this feature as it incorrectly applies the layout for certain types of models.

Find: Search for a word among all the items in the model including the block names, expressions, parameters, memories, and annotations. This does not find the keyword in class files.

Import a Library: If you want to import a library acquired from another install of VisualSim or hand coded XML file, select Import Library from the Graph menu. Now, select the XML file.

Save in Library: The current model and its entire hierarchical list can be saved in the local library as a block. This is done by clicking the “Save in Library” on the Graph Menu.

Create Hierarchy: A section of the current window can be made into a hierarchical block by selecting the set of blocks and the relations and clicking “Create Hierarchy” in the Graph Menu. This function creates a new block with all of these selected blocks inside. All the required port for the interfaces are automatically created. It is important to select the links connected to the ports at the periphery of the area selected. This ensures that the correct ports are generated.

Instantiate Entity: This instantiates a sub-model or class as a block in the BDE window.

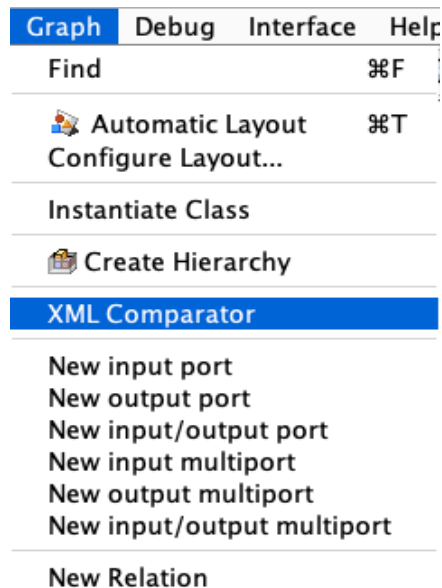
3.1.2.9 Xml Comparator

Xml Comparator can be used to compare two model XML files. The user selects a second model xml file to compare with the current open model file. The results of the comparison are stored in the same folder as the model with the name- nameofModelFile_XML_Comparator.

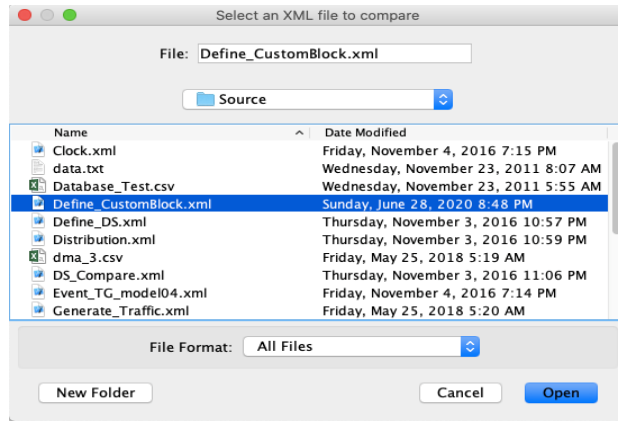
NOTE: A file path or file name containing should not be selected for comparison. If selected, an Illegal Action Exception will be thrown.

Steps to perform the comparison

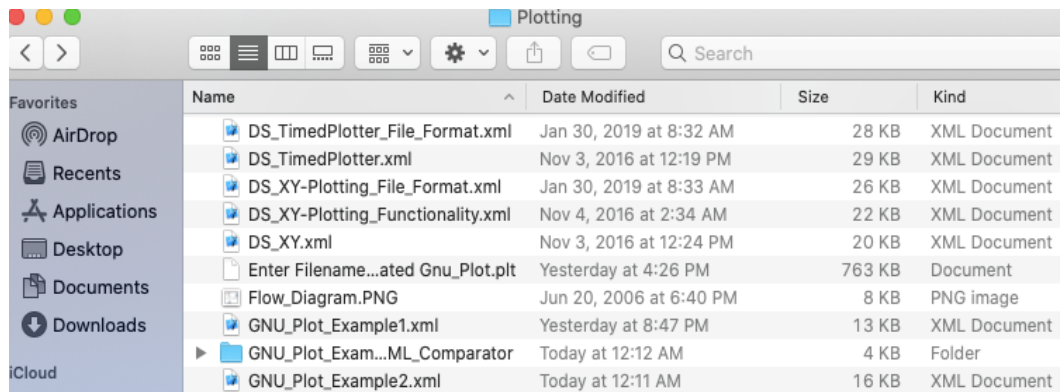
- Select the Xml Comparator for the Graph menu.



- Select another xml file for comparison.



- Go to the location of the Model xml file.
- Go into the parent folder created in the location.



- Open the .txt file contained in the folder to view the result.

```

| XML_Comparator Results
Valid Relations === [relation3, relation2, relation, relation4, relation5, relation6]

Valid Ports === [EventSource.output, FSM_Hierarchical.trigger, Integrator.input, Scale.output, Integrator.output, Integrator2.input, Integrator2.output, Scale.input, FSM_Hierarchical.input2, Const.output, FSM_Hierarchical.input1, xTimeyDataPlot.input, FSM_Hierarchical.output]

Invalid Relations === []

Invalid Ports === []

Actor and parameter comparison ====
No differences were observed between the two XML files
File = /Applications/VisualSim/V_S_AR/demo/analog/Switch/Switch.xml , All relations and Ports connected :
-----
* relation3
  EventSource.output
  FSM_Hierarchical.trigger
* relation2
  Integrator.input
  Scale.output
* relation
  Integrator.output
  Integrator2.input
* relation4
  Integrator2.output
  Scale.input
  FSM_Hierarchical.input2
* relation5
  Const.output
  FSM_Hierarchical.input1
* relation6
  xTimeyDataPlot.input
  FSM_Hierarchical.output

```

Figure 1

- Figure 1 shows the result of the comparison between VS_AR/demo/analog/Switch/Switch.html with VS_AR/demo/AADL/TeleModel_VS.xml.

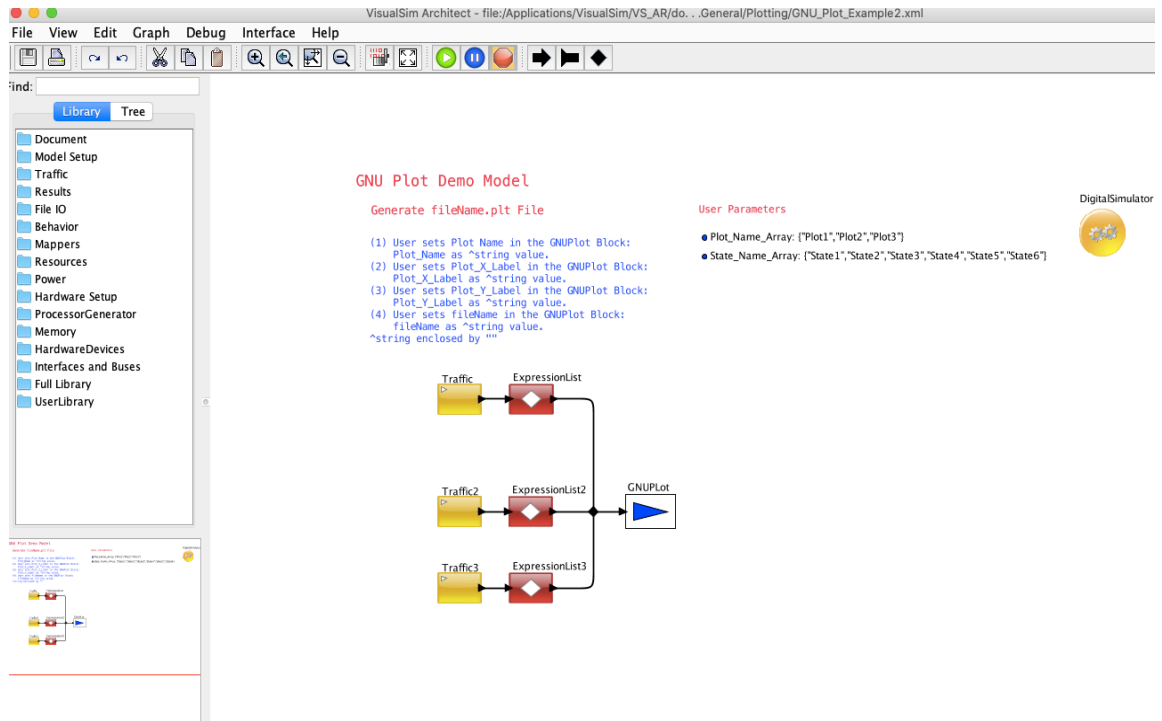





Figure 2

- Figure 2 shows the example of a Model xml file.

3.1.2.10 Model Hierarchy:

The model hierarchy can be viewed in two ways.

- ⇒ Click the Tab on the left that says Tree. You can now select and view any Hierarchical block in the model.
- ⇒ Click the  icon to see more details about inside of each hierarchical block.
- ⇒ You can drag and drop entities from the hierarchy diagram on to the canvas.
- ⇒ Click the  or  icons to see the characteristics of the entity.

3.1.2.11 Find

This resides about the Library folder list. This is used to search all the blocks in the library folder list.

3.1.2.12 System Properties

To view the system properties, click View in the Menu, and then click JVM Properties.

3.1.2.13 System Functions

Compile and Generate Wrapper in ModelBuilder

The Generate Wrapper option generates all the required interface blocks to construct a VisualSim block out of existing Custom C, Custom C++, SystemC, and Verilog wrapper. A note on the Command-line indicates that the operation has completed.

The Compile option compiles all the custom-coded block in the model. Current support is for C, C++, SystemC, and Verilog. The output window indicates when the compile is completed.

Memory Management or Garbage Collect

Operation: Select the Garbage Collect icon () in the standard toolbar.


Details: This is useful when there are custom-coded blocks. Use the Garbage collection at regular intervals and before starting a simulation.

Export to Html

Operation: Generate a document from the model.

Details: This Menu item enables the user to open any model and generate a html document. The tool generates separate pages for each Hierarchical level. The page contains all the parameters, images, blocks, and any documentation described using Annotations. At the bottom of each page, the Applet containing the model is included. On the top page for the model, the simulation will be executable. For all other pages, the view of the model alone is provided.

3.1.2.14 Open the Containing Model

Click on the big triangle  in the toolbar to open the hierarchy window containing the current block diagram.

3.1.3 Listeners

- Listen to Block: Right click the required block and select Listen to Block. The Pop up text window displays the progression of execution in the block. Then run the model. This feature is not available for Hierarchical blocks and instantiated hierarchical classes. If you need to see the details of operation within a Hierarchical block, you need to Open Block and select the block to view the execution details. If you need to view the detailed operation of a Instantiated class, you need to select Open Instance and select the block to view the execution details.
- Listen to Port: Right click the required port and select Listen to port. The Pop up text window displays each Token passing through the port. This feature is not available for Hierarchical blocks. It is supported for regular blocks and instantiated hierarchical classes. If you need to see the data flowing into and out of a Hierarchical block, you could add a

“relation” in front of the port. You can connect a Text_Display to this relation to view the activity.

3.1.4 Folders and Tree

Folders:The list of pre-built and user library are provided in the Library folder on the left-side of the Block Diagram Editor. Click on any of the names to see the library blocks listed below. To use a block, simply select the block name in the Library and drag-n-drop the block into the Editor space.

Tree:The Tree tab allows the user to view the list of Hierarchical blocks in the model. The user can click on a name and the respective hierarchical block opens. After the block is open, go back to the original Window, select, and drag-n-drop the hierarchical into the canvas.

Find: The Find function in the Folder can search the entire library table and find the block that matches the search word. Currently this only searches for an exact match.

3.2 Text Editor and Listener Windows

3.2.1 Introduction

The text editor is used extensively for authoring code in the Script. It is also used to view text files. The Listener windows use the Text Editor. So, all the commands listed below are supported by those viewers also.

3.2.2 Commands

All the File, View, and Help commands match the Block Diagram Editor.

3.2.3 Quick Key Commands

The Text Editor does not have the Menu Bar. The user will have to know that CTRL+C, X, V, CTRL+F,H, R are for copy, cut, paste, find, forward, and backward.

3.3 Plotters and VisualSim Post Processor

3.3.1 Introduction

VisualSim Plot provides comprehensive charting and analysis capability that enables the modeler to remain within the VisualSim environment for all complex analysis. The Plot graphs are instantiated in a model and are displayed as independent viewers when a simulation is started. The independent Post Processor application allows the user to set the view vs. save options for the plots and the plot file name. An associated index file allows for the plots from multiple runs to be combined and viewed in a single display. The graphs can be generated using various Display blocks in VisualSim and by importing XML data files from an external source. The graphs can also be embedded in an HTML executable specification as a Java Applet. Plot includes all the format functions required to modify the view. A variety of charts including, XY, bar, histogram, timeline, and signal are available.

VisualSim Plotting is a set of two-dimensional signal plotters that enhance the capability of the VisualSim simulation platform. Plotting is sometimes viewed as a "post" modeling activity. You can use the VisualSim Post and the Post Processor application to graphically display and analyze data collected from the simulation. The Plotters can organize results into a variety of x-y graphs and histogram plots for graphical display. An XML extension language for plot data has been created and is available for the user to extend.

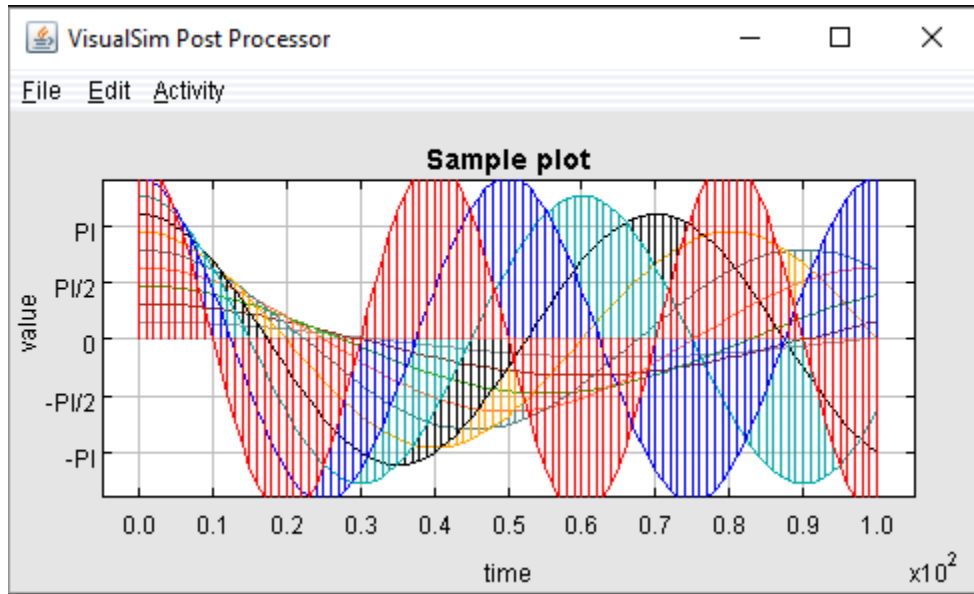


Figure 1. VisualSim Plot Application Window

The following are the key properties of the product:

- Embeddable in applets or applications
- Auto-ranging
- Automatic or manual labeling of axes
- Automatic or manual tick marks
- Logarithmic axes
- Live, animated plots
- Zooming upto the resolution
- Various plot styles: connected lines, scatter plot, bars, and so on
- Various point styles: none, dots, points, and unique marks
- Multiple data sets and a legend
- Color or black and white plotting
- Error bars

- Editable plots
- XML language for specifying plots
- Within a folder if there are multiple files having same name with consecutive numbering like myfile_1, myfile_2, myfile_3, then on selection, all 3 plots will be combined into a single plot and thus a single metric can be compared for different test cases easily.

3.3.2 Post Processor Window

File	Same as Block Diagram Editor. Note that Print, Export, and Import are disabled.	
Edit	Format	Modify the layout of the plot.
Special	Clear	Empties the plot.
	Export to File	Export to eps/gif/png format.
	Export to Clipboard	Saves in clipboard for use by other applications.
	Fill	Populate the plot.
	Reset Axis	Reset axis to include all values.
	Sample Plot	Puts a generic set of values in the plot window.
Help	About	View a brief description about the company and product.

3.3.3 Using Plot

3.3.3.1 Zooming and filling

To zoom in, drag the left mouse button down and to the right to draw a box around an area that you want to see. To zoom out, drag the left mouse button up and to the right. To just fill the drawing area with the available data, type Control-F, invoke the fill command from the Special menu or click the Fill icon (☒). In applets, the fill command is a button at the upper right of the plot.

3.3.3.2 Printing and exporting

The File menu includes a Print and Export command. The Print command works as you expect. The export command produces a png, gif, and black-and-white encapsulated PostScript file (EPS) suitable for inclusion in word processors and Web Pages.

Note: At this time, the EPS file does not include preview data. This can make it somewhat awkward to work with in a word processor, as it will not be displayed by the word processor while editing (however it prints correctly). It is easy to add the preview data using the freely available program Ghostview¹. Just open the file using Ghostview and, under the edit menu, select "Add EPS Preview." Export facilities are also available from a small set of key bindings, which permits them to be invoked from applets (which have no menu bar) and from the invoked VisualSim Plot.

Note further that with applets, you may find it best to click near the title rather than clicking inside the graph itself and then type the command.

Exporting to the clipboard and to standard output, in theory, is allowed for applets, unlike writing to a file. Thus, these key bindings provide a simple mechanism to obtain a high-resolution image of the plot from an applet, suitable for incorporation in a document.

¹ Ghostview is available in <http://www.cs.wisc.edu/~ghost>.

However, in some browsers, exporting to standard out triggers a security violation. You can use Sun's *appletviewer* instead.

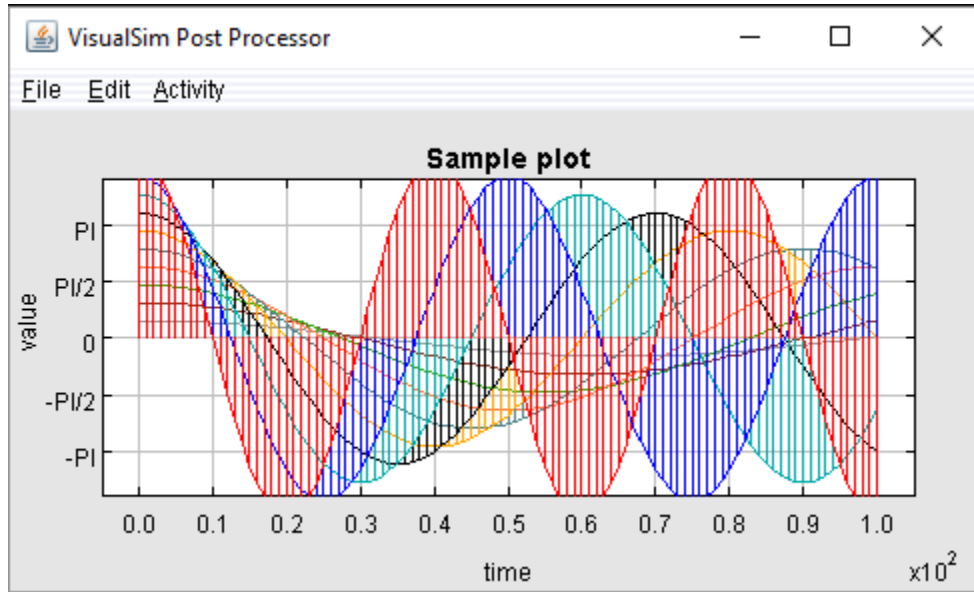


Figure 2. AppletViewer

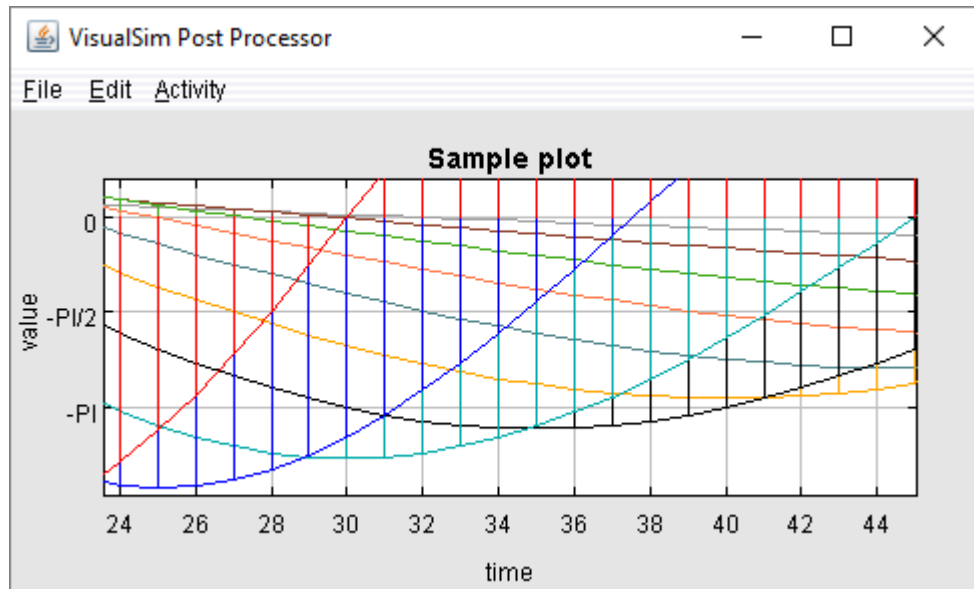


Figure 3. Zoom in.


To zoom in, drag the left mouse button down and to the right to draw a box around the region you wish to see in more detail.

1. Control-c: Export the plot to the clipboard.
2. Shift-d: Dump the plot to a standard output.
3. Shift-e: Export the plot to a standard output in EPS format.
4. Shift-f: Fill the plot.

3.3.3.3 Editing the data

You can modify the data that is plotted by editing the plot file.

3.3.3.4 Modifying the format

You can control how data is displayed by invoking the Format command in the Edit menu or the Format Icon () on the Toolbar. This brings up a dialog like the one in Figure 4. At the left, are the dialog and the plot before changes are made, and at the right are after changes are made. In particular, the stems are added, the lines connecting the data points are added, and the data points are rendered with points. Use the **Save** or **Save As** command in the File menu to save the modified plot. More sophisticated control over the plot can be had by editing the Plot file, which is a text file.

The entries in the format dialog are all straightforward to use except the "X Ticks" and "Y Ticks" entries. These are used to specify how the axes are labeled. The tick marks for the axes are usually computed automatically from the ranges of the data. Every attempt is made to choose reasonable positions for the tick marks regardless of the data ranges (powers of ten multiplied by 1, 2, or 5 are used).

To change what tick marks are included and how they are labeled, enter into the "X Ticks" or "Y Ticks" entry boxes a string of the following form:

`label position, label position, ...`

A label is a string that must be surrounded by quotation marks if it contains any spaces. A position is a number giving the location of the tick mark along the axis. For example, a horizontal axis for a frequency domain plot may have tick marks as follows:

XTicks: `-PI -3.14159, -PI/ 2 -1.570795, 0 0, PI/ 2 1.570795, PI 3.14159`

Tick marks could also denote years, months, days of the week, and so on.

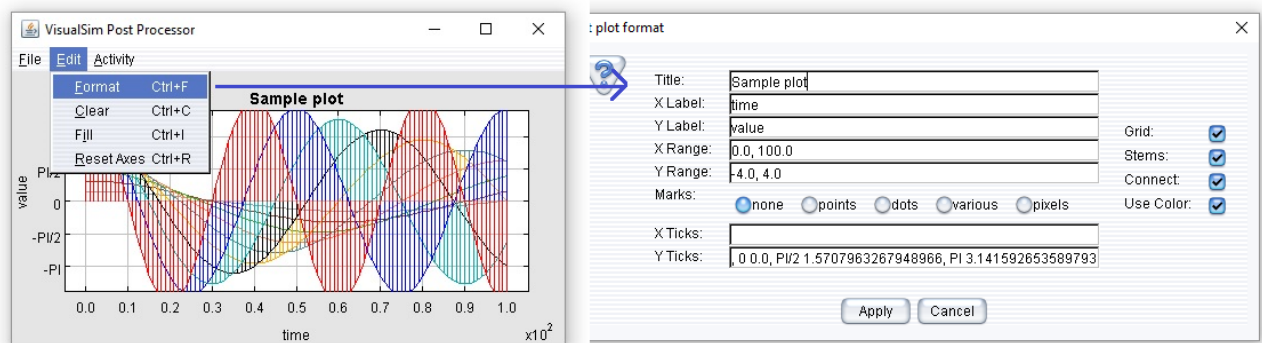


Figure 4. Plot

The above plot displays the Control data using the Format command in the Edit menu.

3.3.4 Commands Configuring the Axes

The following commands are understood by the Application. These commands can be placed in a file and then read as a local file or via a URL. The recognized commands include:

- **TitleText:** string
- **XLabel:** string
- **YLabel:** string

These commands provide a title and labels for the X (horizontal) and Y (vertical) axes. A string is simply a sequence of characters, possibly including spaces. There is no need here to surround them with quotation marks, and in fact, if you do, the quotation marks will be included in the labels.

The ranges of the X and Y axes can be optionally given by commands like:

- **XRange:** min, max
- **YRange:** min, max

The arguments min and max are numbers, possibly including a sign and a decimal point. If they are not specified, then the ranges are computed automatically from the data and padded slightly so that datapoints are not plotted on the axes.

The tick marks for the axes are usually computed automatically from the ranges. Every attempt is made to choose reasonable positions for the tick marks regardless of the data ranges (powers of ten multiplied by 1, 2, or 5 are used). However, they can also be specified explicitly using commands such as:

- **XTicks:** label position, label position, ...
- **YTicks:** label position, label position, ...

A label is a string that must be surrounded by quotation marks if it contains any spaces. A position is a number giving the location of the tick mark along the axis. For example, a horizontal axis for a frequency domain plot might have tick marks as follows:

```
XTicks: -PI -3.14159, -PI/ 2 -1.570795, 0 0, PI/ 2 1.570795, PI  
3.14159
```

Tick marks could also denote years, months, days of the week, and so on.

The X and Y axes can use a logarithmic scale with the following commands:

- **XLog:** on
- **YLog:** on

The tick labels, if computed automatically, represent powers of 10. The log axis facility has a number of limitations, which are documented in “Limitations”.

By default, tick marks are connected by a light grey background grid. This grid can be turned off with the following command:

- **Grid:** off

It can be turned back on with the grid.

- **Grid:** on

Also, by default, the first ten data sets are shown each in a unique color. The use of color can be turned off with the command:

- **Color:** off

It can be turned back on with a check box in the Format window.

- **Color:** on

Finally, the rather specialized command format window item.

- **Wrap:** on

Enables wrapping of the X (horizontal) axis, which means that if a point is added with X out of range, its X value is modified modulo the range so that it lies in range. This command only has an effect if the X range has been set explicitly. It is designed specifically to support oscilloscope like behavior, where the X value of points is increasing, but the display wraps it around to left. A point that lands on the right edge of the X range is repeated on the left edge to give a better sense of continuity. The feature works best when points do land precisely on the edge, and are plotted from left to right, increasing in X.

3.3.5 Commands for Plotting Data

The following set of commands are understood by the Application support:

- **Specification** of data to be plotted
- **Control** over how the data is shown

The style of marks used to denote a data point is defined by one of the following commands:

- ◆ **Marks:** none
- ◆ **Marks:** points
- ◆ **Marks:** dots

- ◆ **Marks: various**
- ◆ **Marks: pixels**

Here, points are small dots, while dots are larger. If various is specified, then unique marks are used for the first ten data sets, and then recycled. If pixels are specified, then a single pixel is drawn.

Using no marks is useful when lines connect the points in a plot, which is done by default. If the above directive appears before any DataSet directive, then it specifies the default for all data sets. If it appears after a DataSet directive, then it applies only to that data set.

To disable connecting lines, use:

- ◆ **Lines: off**

To re-enable them, use

- ◆ **Lines: on**

You can also specify "impulses", which are lines drawn from a plotted point down to the x axis. Plots with impulses are often called "stem plots." These are off by default, but can be turned on with the command:

- ◆ **Impulses: on**

or back off with the command

- ◆ **Impulses: off**

If that command appears before any DataSet directive, then the command applies to all datasets. Otherwise, it applies only to the current data set.

To create a bar graph, turn off lines and use any of the following commands:

- ◆ **Bars: on**
- ◆ **Bars: width**
- ◆ **Bars: width, offset**

The **width** is a real number specifying the width of the bars in the units of the x axis. The **offset** is a real number specifying how much the bar of the i-th data set is offset from the

previous one. This allows bars to "peek out" from behind the ones in front. Note that the forward-most data set is the first one. To turn off bars, use:

◆ `Bars: off`

To specify data to be plotted, start a data set with the following command:

◆ `DataSet: string`

Here, `string` is a label that appears in the legend. It is not necessary to enclose the string in quotation marks.

To start a new dataset without giving it a name, use:

◆ `DataSet:`

In this case, no item appears in the legend.

If the following directive occurs:

◆ `ReuseDataSets: on`

then datasets with the same name are merged. This makes it easier to combine multiple data files that contain the same datasets into one file. By default, this capability is turned off, so datasets with the same name are not merged.

The data itself is given by a sequence of commands with one of the following forms:

◆ `x, y`
◆ `draw: x, y`
◆ `move: x, y`
◆ `x, y, yLowErrorBar, yHighErrorBar`
◆ `draw: x, y, yLowErrorBar, yHighErrorBar`
◆ `move: x, y, yLowErrorBar, yHighErrorBar`

The `draw` command is optional, so the first two forms are equivalent. The `move` command causes a break in connected points, if lines are being drawn between points. The numbers `x` and `y` are arbitrary numbers as supported by the Double parser in Java (e.g. "1. 2", "6.39e-15", and so on.). If there are four numbers, then the last two numbers are assumed to be the

lower and upper values for error bars. The numbers can be separated by commas, spaces or tabs.

3.4 VisualSim Post Processor

3.4.1 Introduction

VisualSim Post Processor application is a network-based application that can be shared across a division or a corporation. VisualSim Post Processor is platform and OS-independent, enabling different users to maintain the same experience. In addition, a mobile provision enables the Post Processor to be used offline. This enables flexible usage during travel, design review, and remote presentations.

3.4.2 Key Features

1. Uses an open XML DTD for data management with a .plt extension.
2. Graphical user interface with built-in error checking.
3. Manages the plot selection for viewing and display.
4. Configure a model to save the plots in a specific destination directory.
5. Creates an index for all the simulation runs of the model along with the associated plot.
6. Open plots from different simulation runs simultaneously for easy comparison.
7. Combine datasets from multiple plots into a single graph (Future release).

3.4.3 Quick Key Command

File	Same as the Block Diagram Operations	
	Export	Export plot image as a eps, gif, and png.
Edit	Format	Modify the layout of the plot.

	Clear	Empties the plot.
	Reset Axis	Reset axis to include all values.
Activity	About	View a brief description about the company and product.
	Configure Model	Create an index for the plot and select the simulation parameters to save.
	Open Plot Index	Select plots from multiple simulations to combine and view.
	Combine Simulation Plots	Plot all the individual plots in a directory in a single window.
XML	XML Comparator	Compare two models
	Parse ARXML	Parse the ARXML into a csv file for input to a VisualSim model
GNUPlot	Open File	Open a GNUplot file that was saved from a VisualSim model
Comparator	Select Directory	Open two directories and compare files that are listed in the input.csv file.

3.4.4 Usage

To understand the usage of the Post Processor, let us look at the example available in the Post Processor install under Model_Plots.

- **Step 1:** From the VisualSim Architect Block Diagram Editor, add the PlotManager block (Results > PlotManager) to VME_Bus_Model1.xml. The Plot_Path is updated to the destination of the output plot files.
- **Step 2:** From the Post Processor window, select Activity > Configure Model. Now, select the VME_Bus_Model1.xml. Click the parameters that are varied to create the different unique simulation runs of the model. Also specify which plots need to be viewed and which one must be saved. Click OK or Apply + OK. This creates an index file in the destination directory.
- **Step 3:** Now run the simulation in batch or interactive mode by varying the selected parameters. If parameters not selected in Step 2 are used, these runs are not to be treated as unique. Other runs could overwrite the plots from these runs.
- **Step 4:** Now return to the Post Processor. From Activity > Open Plot Index, select the VME_Bus_Model1_Index.xml that is located in the destination directory. The list of simulations runs for the model and the associated plots are listed. Select any number of runs and any number of plots. Click OK. The plots are now displayed as separate windows.

3.4.5 VisualSim Architect Models

VisualSim Post Processor works with two Display (Unbuffered and Buffered), TimeDataPlotter, Histogram Plotter, XYPlotter, DS_TimeDataPlotter, DS_XYPlotter, ArrayPlotter and BarGraph blocks of the VisualSim model. The Display blocks are supported for the purpose of setting View and Save only. They can not be opened with VisualSim Post Processor. The graphs are stored in XML files with a .plt extension. Simulation results from a single model are stored together and are tagged with the simulation run ID and the plot name. A simulation index file maintains the connection between the simulation run and the graphs. The simulation runs are uniquely identified by the variation of the parameter.

3.4.6 Usage

VisualSim provides all the standard graphical user interface capability. These include edit functions such as open a new plot file (single file), print, save, and export to eps format. The format functions provide the ability to modify the view of a single plot. The Activity menu configures simulation model and opens the index file containing references to plot data.

3.4.7 Activity Menu

The Activity contains the “Configure Model” and “Open Plot Index”.

Configure Model- This is used to configure a model to view or save plots. Step-by-step instruction:

1. Add **PlotManager** block in VisualSim Block Diagram of the model to be configured.
2. Specify output directory path in the PlotManager block parameter Plot_Path.
3. Select **Activity > Configure Model** from the main Post Processor application window.
4. From the parameter list, select the parameters that are modified during this batch run of simulation results. Leave out parameters that are modified during this run. You can always go back and redo this listing for a different run.
5. For each plot in the model, you can view (during the simulation), save or both. Select the radio button to enable this.
6. Click **OK**. You can also click Apply and then OK. Cancel exits this Configure screen without making any changes.

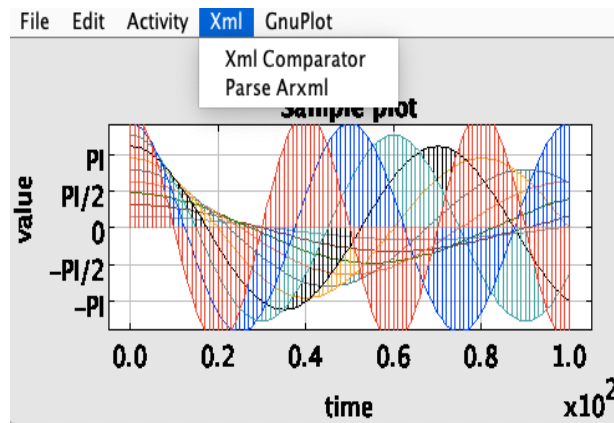
Open Plot Index - This opens the reference to the simulations and their respective plots.

1. After completing the simulation runs, return to the Post Processor.
2. Select **Activity > Open Plot Index**.
3. Go to the output directory and select the Plot Index.

4. A list of simulation runs identified by the values of the selected parameters are displayed on the top-half of the window. A list of the plots is displayed in the bottom.
5. Select one or more simulation runs and one or more plots (all is also an option).
6. The select plots open in separate windows.
7. Sometimes, a blank plotter screen may appear. Click on Format → Fill to view the Files.

Note: All plot windows appear one on top of the other.

3.4.8 XML Menu



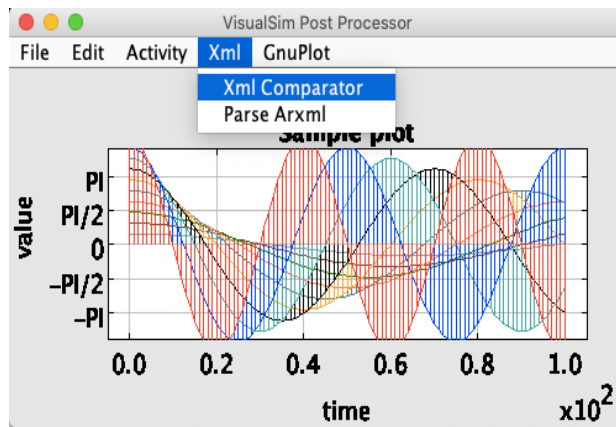
3.4.8.1 Xml Comparator

Xml Comparator can be used to compare two .xml files. The user has to select two xml files the files selected can be same or different. The result of the comparison is stored in the form of .txt file in a parent folder named as nameofsecondfile_XML_Comparator created in the location of the second xml file that is selected.

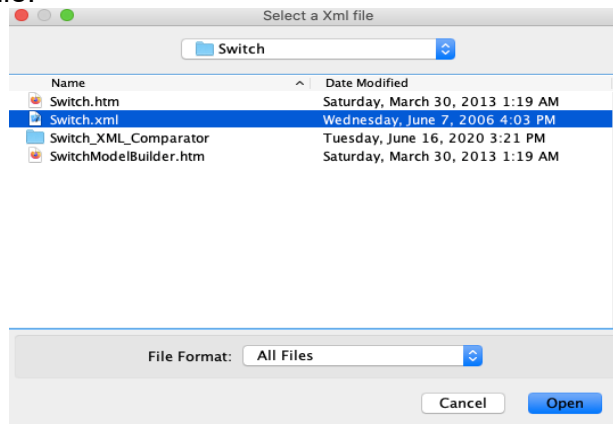
NOTE: A file path or file name containing should not be selected for comparison. If selected an Illegal Action Exception will be thrown.

Steps to perform the comparison

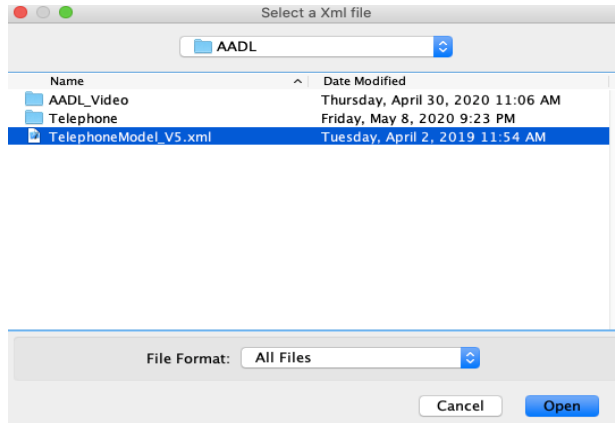
- Firstly, select the Xml Comparator for the Xml menu.



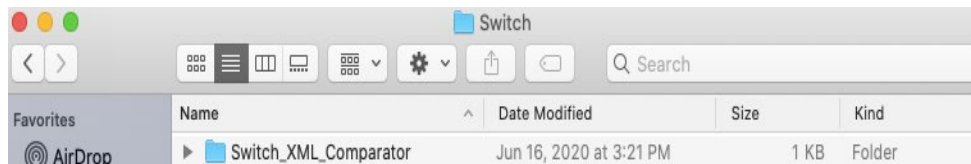
- Select the first xml file.



- Select the second xml file.



- Go to the location of the second xml file.
- Go into the parent folder created in the location.



- Open the .txt file contained in the folder to view the result.

```

XML_Comparator Results
Valid Relations === [relation3, relation2, relation, relation4, relation5, relation6]

Valid Ports === [EventSource.output, FSM_Hierarchical.trigger, Integrator.input, Scale.output, Integrator.output, Integrator2.input, Integrator2.output, Scale.input, FSM_Hierarchical.input2, Const.output, FSM_Hierarchical.input1, XTimeDataPlot.input, FSM_Hierarchical.output]

Invalid Relations === []

Invalid Ports === []

Actor and parameter comparison ===
No differences were observed between the two XML files
File = /Applications/VisualSim/VS_AR/demo/analog/Switch/Switch.xml , All relations and Ports connected :
-----
* relation3
  EventSource.output
  FSM_Hierarchical.trigger
* relation2
  Integrator.input
  Scale.output
* relation
  Integrator.output
  Integrator2.input
* relation4
  Integrator2.output
  Scale.input
  FSM_Hierarchical.input2
* relation5
  Const.output
  FSM_Hierarchical.input1
* relation6
  XTimeDataPlot.input
  FSM_Hierarchical.output

```

Figure 1

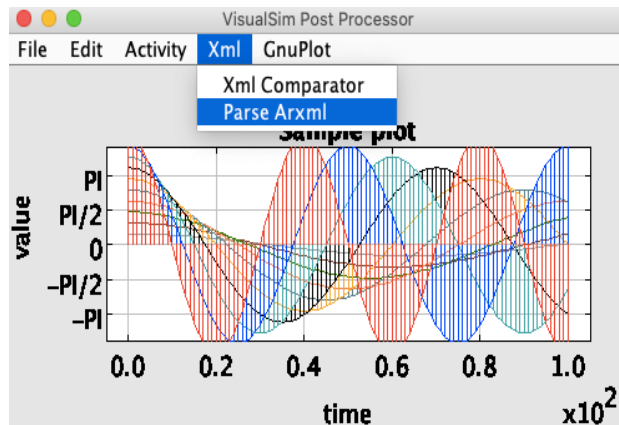
- Figure 1 shows the result of the comparison between VS_AR/demo/analog/Switch/Switch.xml with VS_AR/demo/AADL/TelephoneModel_VS.xml.

3.4.8.2 Parse Arxml

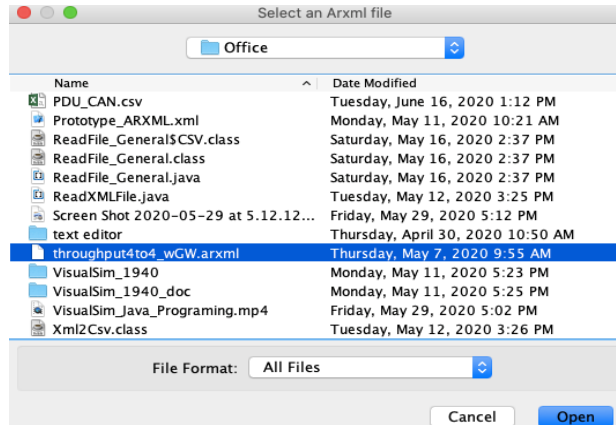
The Arxml Parser can be used to parse the selected arxml file. The result is generated in the form of CSV files stored in the location of the selected file.

Steps to Parse an Arxml file:

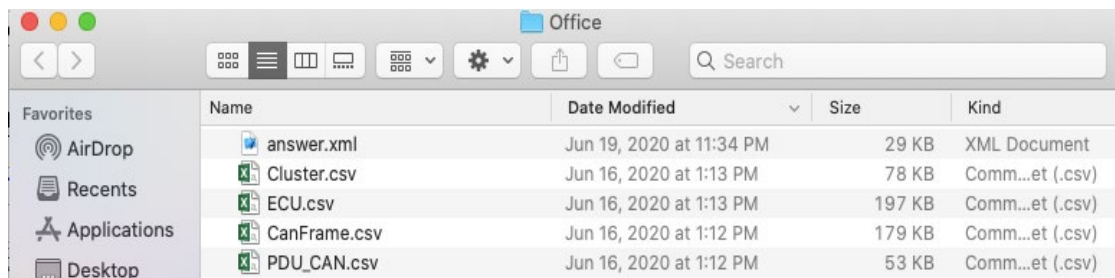
- Select Parse Arxml from the Xml Menu.



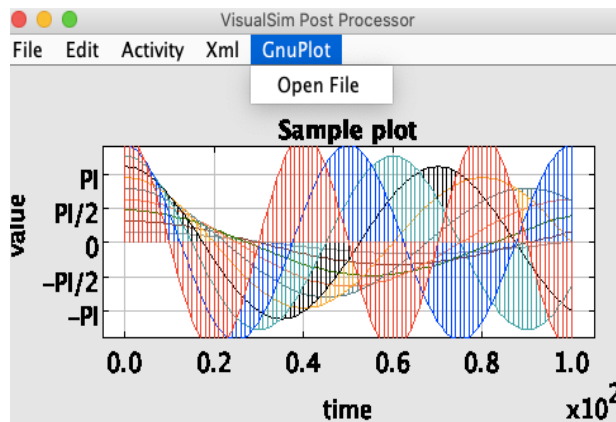
- Select a .arxml file.



- Go to the location of the selected file.
- Open the CSV files to view the result of parsing.



3.4.9 GnuPlot Menu

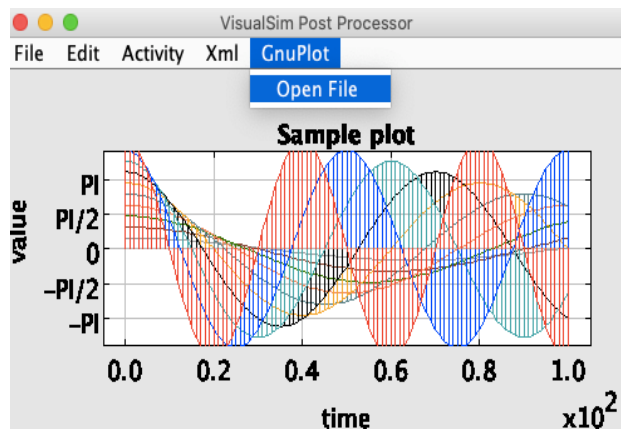


Open File

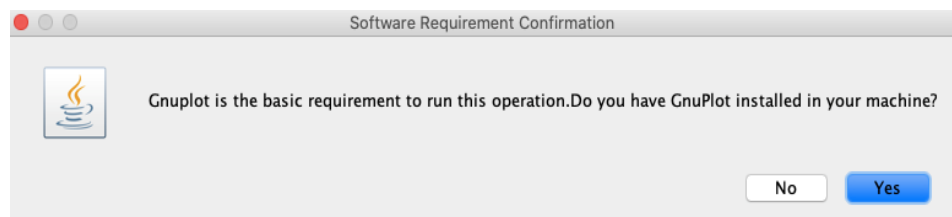
Open File option can be used to open any .plt file stored on the user's machine.

Steps to open a PLT file

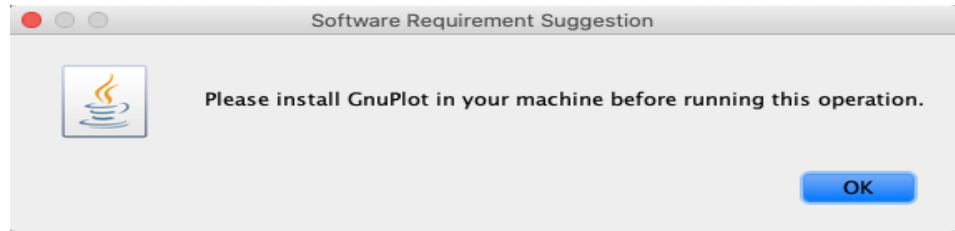
- Select open file from the GnuPlot menu.



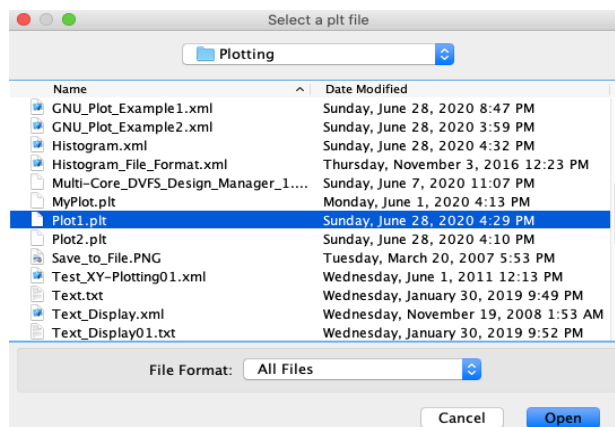
- Then a message box will be displayed as given in the figure below.



- If GnuPlot application is not installed on your machine select 'No' and the below message box will be displayed.



- If you have the GnuPlot application installed on your machine then select 'Yes' And select a .plt file to opened.



- The selected file will be opened in GnuPlot application.

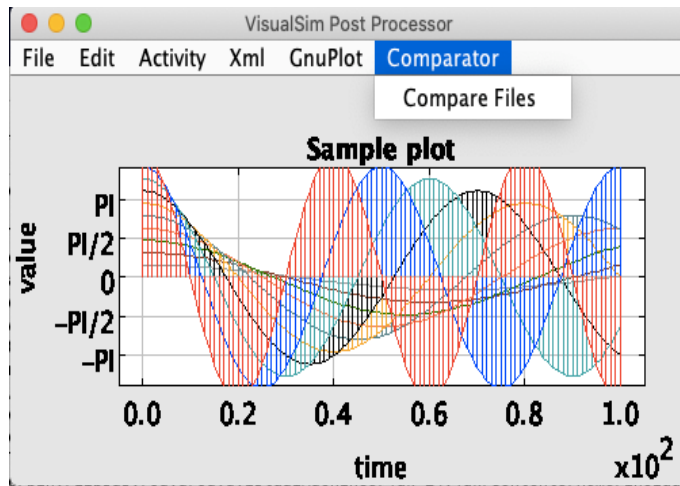
3.4.10 Post Processor-> Comparator

- Comparator is one of the functionalities integrated in the Post Processor under the Comparator menu.
- Simulate models and generate Text files or CSV files
- Make sure to store the results from different runs in their own directories.
- Select one directory as the base and the second as the compare directory.
- Create a configuration csv file with the base and compare file name, list of items to compare, and file types.

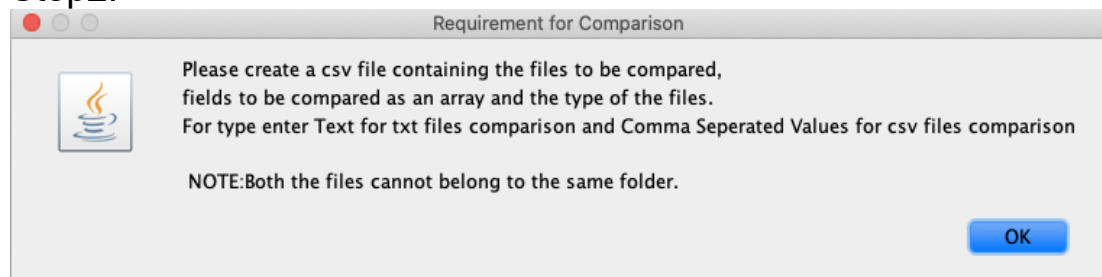
- Open the Post Processor go to the comparator menu and run the comparator.
- Select the input configuration csv file, base directory and the compare directory.
- The result files will we stored in the first directory that was selected.

3.4.10.1 Demo Run of the Comparator

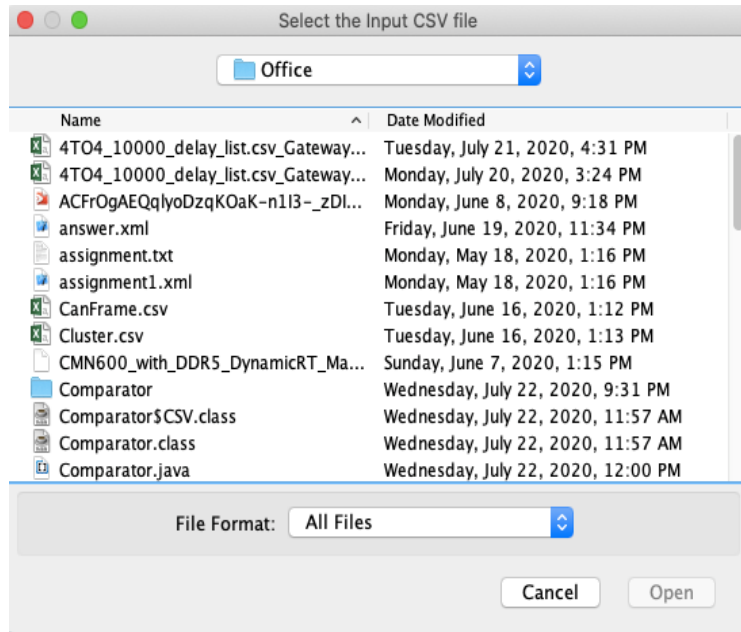
- Step1:



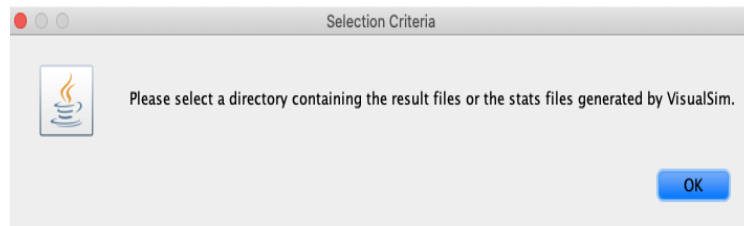
- Step2:



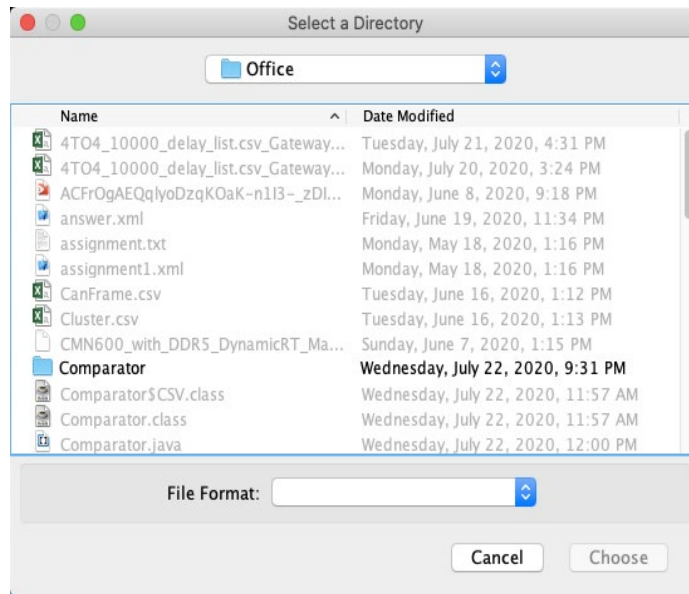
- Step 3:



- Step4:



- Step 5:



- Step 6: Repeat Step 4 and Step 5 to select the compare directory
- Results are stored in the first directory.

Name	Date Modified	Size	Kind
Datacenter_Resource_Stats.txt	Yesterday at 4:27 PM	98 KB	Plain Text
Datacenter_Res...e_converted.csv	Today at 12:27 PM	215 KB	Comm...et (.csv)
Datacenter_Res...comparison.csv	Today at 12:27 PM	38 KB	Comm...et (.csv)
datacenter_stats.txt	Yesterday at 4:27 PM	77 KB	Plain Text
datacenter_stat...arison_result.txt	Today at 12:27 PM	209 KB	Plain Text
Latency_Stats.csv	Yesterday at 4:27 PM	537 KB	Comm...et (.csv)
Latency_Stats.c...comparison.csv	Today at 12:27 PM	1.6 MB	Comm...et (.csv)

- Examples of input file and directories.

Datacenter_Resource_Stats.txt	Yesterday at 4:27 PM	98 KB	Plain Text
Latency_Stats.csv	Yesterday at 4:27 PM	537 KB	Comm...et (.csv)
datacenter_stats.txt	Yesterday at 4:27 PM	77 KB	Plain Text
Latency_Stats.csv	Yesterday at 4:30 PM	717 KB	Comm...et (.csv)
datacenter_stats.txt	Yesterday at 4:29 PM	374 KB	Plain Text
Datacenter_Resource_Stats.txt	Yesterday at 4:29 PM	98 KB	Plain Text

- Example of the input csv file

Datacenter_Resource_Stats.txt	Datacenter_Resource_Stats.txt	{Total_Delay_Max / Total_Delay_Mean / Total_Delay_Min / Total_Delay_StDev / Utilization_Mean}	Text
datacenter_stats.txt	datacenter_stats.txt	{All}	Text
Latency_Stats.csv	Latency_Stats.csv	{latency}	CSV

3.4.11 Packaging and Archiving

To package and ship the simulation results, simply tar or zip the output directory. This can be shipped to the end-user. The end-user then unzips the content. The model index is contained in the package and can be used for viewing the graphs.

3.5 Icon Editor

This Editor is used to create custom icons for the blocks. This editor has a number of standard shapes, lines, colors, and functions to access block parameters.

If editing a block in a model, then the resulting icon details are stored in the model XML file. If a new icon is being constructed, the resulting icon is stored in an XML format.

An icon can be constructed using shapes such as lines, circles, and rectangles. Alternately, there can be an image used for the icon. The one restriction is that the icon must be in the same directory as the XML file containing the reference.

3.6 Expression Evaluator

This uses the extensive expression language available in VisualSim to evaluate equations

```
>> a = {1,2,3,4}
{1, 2, 3, 4}
>> b = a.append(4)
{1, 2, 3, 4, 4}
>> a = a*b
multiply operation not supported between VisualSim.data.ArrayToken '{1, 2, 3, 4}'
and VisualSim.data.ArrayToken '{1, 2, 3, 4, 4}'
'
Because:
The length of the argument (5) is not the same as the length of this token (4).
>>
```

and algorithm. This can be used for conducting quick studies that are algorithm in nature and do not require simulation. Also, this can be used to test a sequence of expressions and see if they work before using in the Script Block. This supports variables defined in the environment and can be used with any of the functions in the RegEx language. Below is an example:

Notice that the errors in the expressions are also displayed here. This can be used to fine tune your sequences. This window does not support C language functions such as while, if-else, and switch-case.

To learn more about the RegEx language, refer to the RegEx language documentation.

3.7 Simulation Cockpit

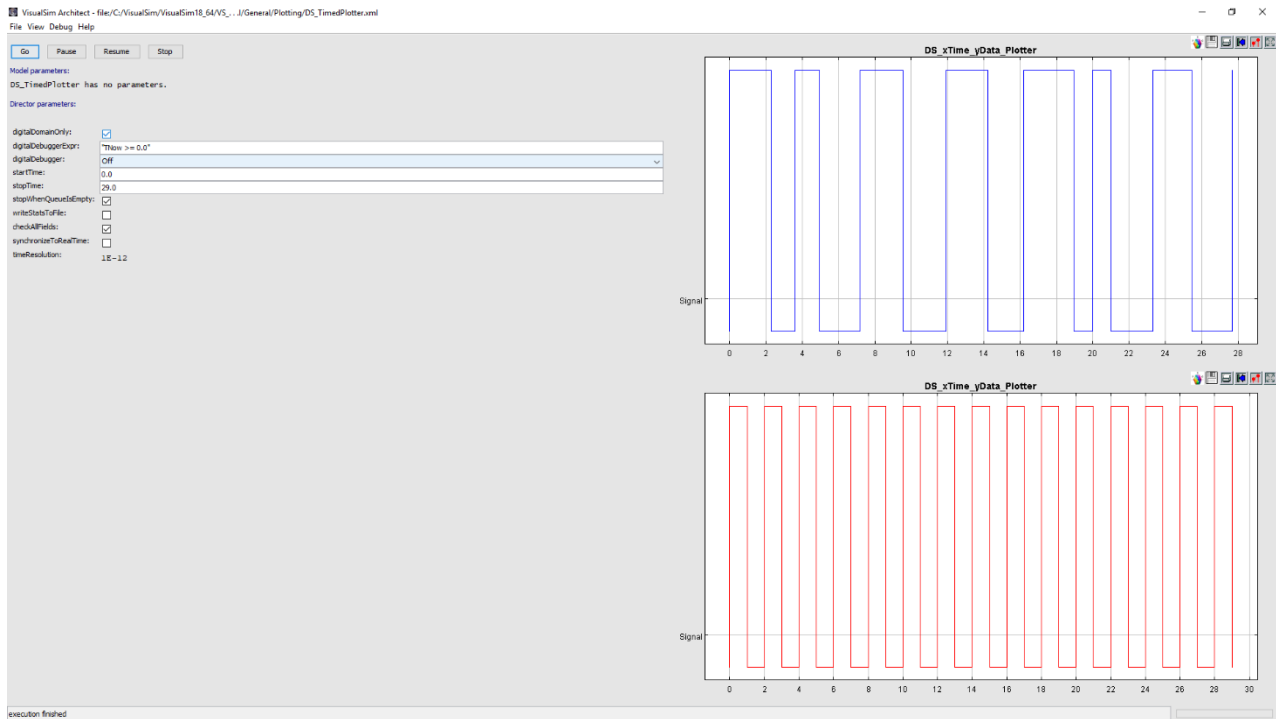
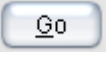
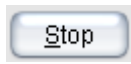
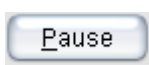
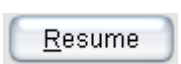


Figure 5. Simulation Cockpit

The simulation cockpit provides a single window to set parameter values, simulate, listen to simulator activity, and view the plotted result. The Simulation Cockpit has been included with VisualSim as a legacy support.

3.7.1 Operation

These functions are the buttons in the Simulation Cockpit.

- ⇒ Click **GO**  to start the simulation.
- ⇒ Click **STOP**  to terminate the simulation and not continue further.
- ⇒ Click **PAUSE**  to temporarily halt the simulation.
- ⇒ Click **RESUME**  to restart the simulation from the point where it was paused earlier.

3.7.2 Listen to the Manager and Simulator

Operation: Click **Debug** in the Menu of the Simulation Cockpit and then click **Listen to Manager/Simulator**.

Details: The **Listen to Manager** has been disabled to speed up the simulation. Future applications of this interface are being considered. The **Listen to Simulator** can report the sequence of block execution and the model profile statistics at the end of the simulation. The setting of the Digital Simulator determines the output. Other simulators do not provide any data to this window.



Note

The **Listen to Simulator** is used in conjunction with the Digital debugger. Refer to the Digital debugger under Model debugging sections.

3.7.3 Stop and Resume

Operation: These functions are the buttons in the Simulation Cockpit.

- ⇒ Click **GO** to start the simulation.
- ⇒ Click **STOP** to terminate the simulation.
- ⇒ Click **PAUSE** to temporarily halt the simulation.
- ⇒ Click **RESUME** to restart the simulation from the point where it was paused earlier.

The simulation can be stopped at any time. The display can be viewed and the simulation can be resumed from that point forward.



Note

For the Pause and Resume to work effectively, the Listen to Manager Dialog window must be started. The simulation is faster than the keyboard access and the Pause request is lost.

3.7.4 Simulation Parameters

Modify the values of the parameters in the Simulation Cockpit and restart the simulation. There are two types of parameters that can be finalized prior to simulation - Simulation parameters and Model parameters. The Simulation parameters modify the actions of the kernel while the model parameters modify the operating of the simulation.

3.7.5 Plot viewers in the Simulation Cockpit

Save : Click this icon to save the data into a file. Specify location and file name and click **OK**.

Print : Click the icon to print the window. In the Print window, select printer, and then click **OK**.

Fill : Rescale the plot to fit the data.

Format : Click the **Format** icon, specify the various attributes, and click **OK**.

Reset : Reset X and Y axis to their original values.

4 Blocks

A block is a basic modeling component available in VisualSim. Every icon in VisualSim is considered a block. A block contains an icon, ports, parameters, and logic inside. The user can modify the parameters. Associated with each are a standard documentation and the ability for the user to create custom documentation. Some of the blocks have the ability to add additional ports. The user can change the graphic image of the icon using the Custom_Icon option. If an attribute such as a rectangle is covering a Block, right-click on the attribute and “Send to Back”.

4.1 Block Execution Semantics

VisualSim supports a common set of block execution semantics. Here we focus on the Digital domain. A Digital library block can optionally execute the following internal methods:

<code>initialize ()</code>	Initialize Block parameters, attributes, memories, and so on
<code>prefire()</code>	Pre-Fire Block once per simulation iteration
<code>fire()</code>	Fire Block, input Tokens processed, outputs generated
<code>postfire ()</code>	Post-Fire Block, iterations, scheduled events
<code>wrapup ()</code>	Wrap-Up Block, free memory, collect ending stats

It is not necessary to become familiar with the details of internal block execution, unless one is planning to create their own custom blocks. The typical block that are shipped with VisualSim executes the `initialize()` and `fire()` methods. In the `initialize ()` method, block parameters, and block menu entries are read, as the block is initialized into the modeling space. In the `fire()` method, input port Tokens are processed, and output port Tokens are generated based on the Block functionality. Graphically, block execution looks similar to the following image:

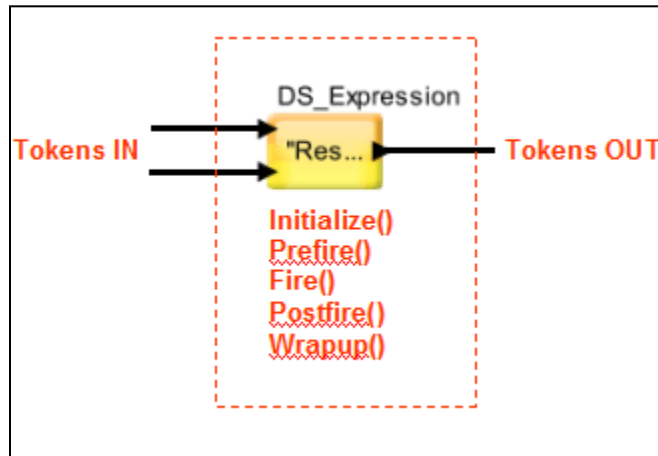


Figure 6. Block Execution Semantics

4.2 Block Layout

A typical Digital Block contains the following attributes:

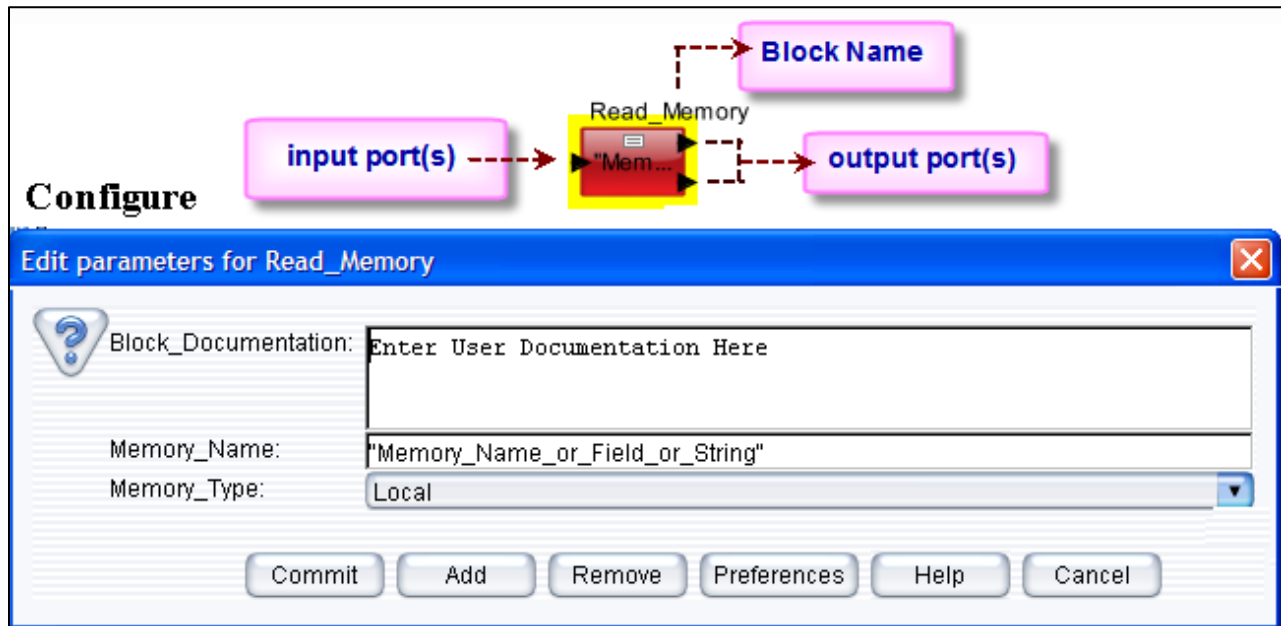


Figure 7. Block Attributes

The user notices that a “Name” sometimes appears on the front of the block symbol. This text typically describes the beginning of the first statement, or other parameter of the block, so the user can quickly identify the block functionality without having to open it.

4.3 Block Context Menu

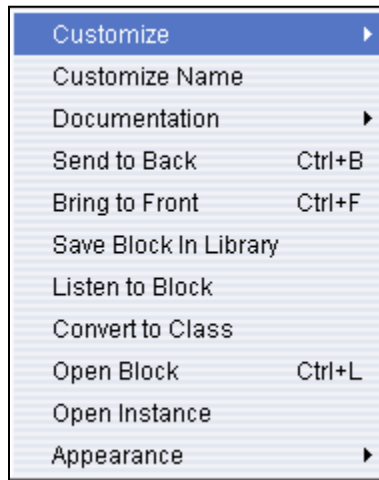


Figure 8. Block Context Menu

The **Block Context Menu** options are explained in the following sections:

4.3.1 Customize

The **Customize Parameters** is available for the parameters, annotation, blocks, and modules. This function can be called to modify or add parameters. After the parameters are modified, click **OK** to update the model or click **Cancel** to retain the current settings.

The **Customize Ports** is available for the ModelBuilder background, blocks, and modules. Click in the cell to be edited. Some properties may not be editable because they are part of block definition. These cells have a red background and ignore any attempts at editing as shown below.

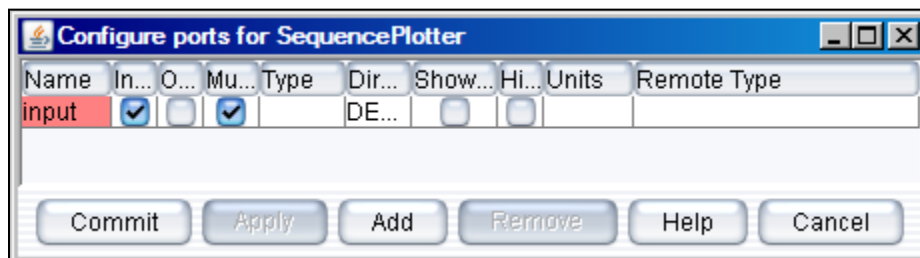


Figure 9. Ports that cannot be edited

Name - Names must not contain a period or a space, must not be blank, and should be unique.

Input, Output, Multiport – Checkboxes that determines if a port is input, output, or both.

Type – The type can be given by any expression that can be evaluated (this expression is called a "prototype"). For example, you can specify the type to be double by giving the string "0.0" (or any other number with a decimal point). However, this does not look very good as a designator for a type. The VisualSim expression language defines the constant "double" to equal "0.0". Thus, the preferred way to specify that a port has type double is to give its type as "double".

The primitive types include:

- o Data Structure
- o boolean
- o complex
- o double
- o fixedpoint
- o general
- o int
- o long
- o matrix
- o object
- o scalar
- o string
- o unknown

The constant "unknown" has a rather special behavior, in that it sets the type of the port to be unknown, allowing type resolution to infer it. The constant "matrix" designates a matrix without specifying an element type, in contrast to, for example, "[double]", which specifies a double matrix (see below). Similarly, the constant "scalar" designates a scalar of any type (double, int, long, etc.). The constant "general" designates any type.

As the type is given by a "prototype", any data type that can be given in an expression can be specified as a type. For structured types, follow the same syntax as in expressions. For example:

`{double}` - double array

`[int]` - int matrix

`{field1 = string, field2 = int}` - For Data Structure

Direction – The Direction determines which side of the icon the port is located on. Clicking in this cell brings up a menu that provides the means to select a specific side, that is. NORTH, EAST, SOUTH, and WEST. DEFAULT can also be selected. Below are the defaults:

- Input ports are usually on the West side.
- Output ports are usually on the East side.
- Ports that are both an input and an output are located on the South side.

Show Name – Disabling this option causes the name of the port to be displayed. Enabling removes the name from the display.

Hide – Disabling this option causes the port to be displayed. Enabling removes the port from the display.

Units – The units specification for the port. This is currently not being used.

Remote Types – This column is used to define the data types on the remote system or application. This is used to define the data types for the Verilog, Application Interface, and SystemC only. This is a string field and must be enclosed by “”. The content in this column text depends on the type of block and the interface.

4.3.2 Customize Name

This feature is available for the parameters, annotation, blocks, and modules. This function is called to modify the name of this entity. After the name has been modified, click **OK** to update the model or click **Cancel** to retain the current settings.

4.3.3 Get Documentation

This feature is available for the blocks and modules. This function opens a new window that provides access to the complete documentation associated with that block. If there is no

documentation provided for the entity, then a dialog window appears indicating that there is no documentation available. The **Customize Documentation** enables the user to override the default documentation and add their own information. This is associated with that block in the model. Note that once the user selects the Customize Documentation item, the documentation shows the new format. To undo this option, the user must go to **Remove Custom Documentation**.

4.3.4 Send to Back

This moves the selected block behind whatever is in front. For example, it can be a Annotation or a Rectangle.

4.3.5 Bring to Front

This moves the selected block to the front.

4.3.6 Save Block in Library

The selected block can be saved in the local library. This is a useful way to store the frequently used blocks in a local list.

4.3.7 Listen to Block

This feature is available for the blocks and modules. A new text window opens. This feature enables the user to view the progression of the execution through the selected block. This feature is not available for Hierarchical blocks. It is supported for regular blocks and instantiated hierarchical classes. If you need to see the details of operation within a Hierarchical block, you need to Open Block and select the block to view the execution details. If you need to view the detailed operation of a Instantiated class, you need to select Open Instance and select the block to view the execution details.

4.3.8 Set Breakpoint

This feature allows the user to set the breakpoints at any block. This feature is available only for Digital and Untimed Digital Domains. This can be used to move the simulation to a particular point in the simulation and then debugging operation such as a listen to block.

4.3.9 Convert to Class

This feature converts this block into a class. A class is a master version of the block. This class can be instantiated multiple times in the model. Changes made to this class block (identified by a blue halo), are replicated to all linked instances. The information in the XML for the instances are all linked to this class block.

4.3.10 Create Instance

This creates an instance of the class block.

4.3.11 Create Subclass

This creates a subclass of the class block. Instances can also be created of the sub-classes. Changes made to this block propagate to the instances. Changes made to the class block are propagated to this block.

4.3.12 Convert to Instance

This converts the class or subclass back to an instance.

4.3.13 Open Block

This feature is available for hierarchical blocks and those shipped with source code. All other blocks show up with an error message.

4.3.14 Open Instance

This opens the details of the instance and not the original class. This is very important for models constructed with XML classes. The instance code must not be modified. Modify the

code in the block definition. If the instance code is modified, the reference to the original class is disconnected. Use the Instance to do Listen to Block/Port for debugging in the model.

4.3.15 Edit Custom Icon

This menu item is used to replace the current icon for the selected block with a custom drawn icon. This item opens the Icon editor. The user can create a custom icon in the Editor and save it in the XML file along with the current model.

4.3.16 Remove Custom Icon

This restores the original icon and removes the custom icon.

4.4 Setting up a Block

4.4.1 Blocks Overview

1. All Data Structures enter on the top-left (input port) and exit on the top-right (output port). Blocks have parameters that can be populated by the user. There is a format for filling the values for every block.
2. The traffic is the stimulus that goes through from block to block. The input into a block causes the block to fire, meaning that the block takes the content of the input; does modification to the content or does some action based on the content; and then places it on the output port.
3. Block field entry rules:
 - a. Any parameter field that is shaded blue is a string expression. All values placed within this string do not require "" around them.
 - b. If the entry is an expression and the background of the parameter space is not blue, the complete expression must be enclosed in a "".
 - c. If the entry is a number or a parameter, then no quotes are required.

- d. Memories and field names must be always within "", if the parameter field is not shaded blue.
- e. ExpressionList, Script, and Smart Controller blocks support multiple input ports. Hence the field names on any input port must be identified with the prefix of "port_name.". For example, input.INDEX is the INDEX field in the Data Structure arriving on the port called "input".
- f. The Script block also supports a generic port, called port_token, that represents any input port, and the current executing thread.
- g. In the Basic Processing and Resource blocks, there can be only a single input port. Here, the field name does not contain the "port_name" prefix.

4.4.2 Updating Parameters and adding additional parameters

To set up a block in VisualSim, double click the library and select the required block. Drag and drop the block into the BDE and double click the block to set the parameters. You can also right click and select **Customize > Configure**. The Edit Parameter window is displayed. Set values for the predefined parameters. You can create a new parameter for the block. To add a new parameter, click **Add**, enter the parameter name, default value and class. Click **OK**.

4.4.3 Updating Ports and adding additional ports

You can add ports to block. By default, every input port is located on the left hand side of the block and the output port is on the right hand side of the block. To add a port, right click the block and select **Customize > Ports**. Click **Add** and a new field is created. Enter the name of the port and select the type of the port. The type of the port is described in detail as follows:

If **input** is selected, the new port is created on the left side (default-West) of block.

If **output** is selected, the new port is created on the right side (default-East) of the block.

If **multiport** is selected, the new port is created on the left side (default-West) of the block.

If both **input** and **output** are selected, the new port is created at the bottom (default-South) of the block.

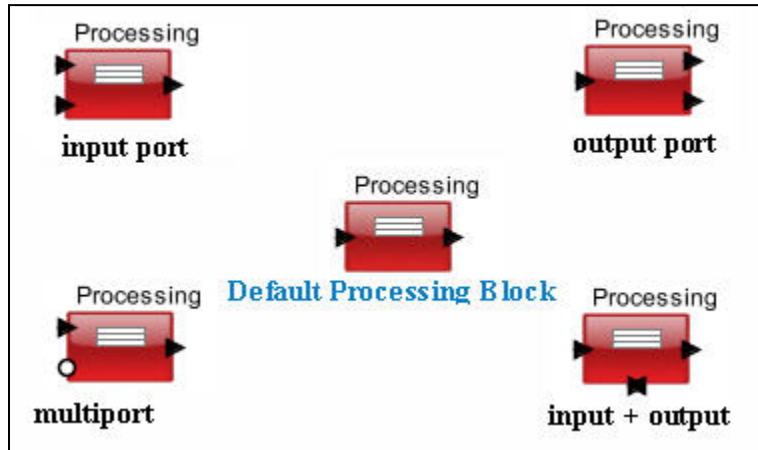


Figure 10. Set Ports to Block

User can also change the direction of the port to North, East, South or West. There are options to display the port name or hide it. Units or the Remote type can also be set.

Port data type- general (Default). In most cases, the port type does not have to be changed. It can be maintained in the default state. There are certain instances when the connected input port has a fixed data type. In that case, the output port connected to it must be modified.

Show Name – To display the port name

Hide - To hide the port name.

Remote Types- This column is used to define the data types on the remote system or application. This is used to define the data types for Verilog, Application Interface, and SystemC blocks only. This is a string field and must be fully contained within “”. The content in this column text depends on the type of block and the interface.

4.4.4 Setting Port Types

Some block ports may have pre-defined data types. For example, the plotter input and the pop input of the Queues. In these cases, the ports connected to these fixed data types must be modified. If the ports are not correctly specified, an exception is reported. To modify the

port type, right mouse-click on the block to "**Customize > Ports**". To see the current type prior to modifying, context display by passing the mouse pointer over the specific ports. If the connected ports have type General, then no change is required. If either the input or output type has a specific type set, then the other one must also match this value. If a port has type Unknown, and is connected to a type of General, then set the Unknown to General.

4.4.5 Linking Parameters

Block Parameter is the default parameter available in a block. User can also add or remove block parameter. **Model Parameter** is available in the VisualSim library: **Model Setup > Parameter=**. How to set a model parameter to the model is explained below.

To set a new parameter to model, drag and drop the model parameter from **Model Setup > Parameter=**. Right click the model parameter and select **Customize Name**. Enter the name of the parameter and click **Show name** to display the name in BDE. Now, double click the **Parameter:** to set the value for the parameter. Copy the model parameter name and paste it in the block parameter. Now you have successfully linked a model parameter with a block parameter.

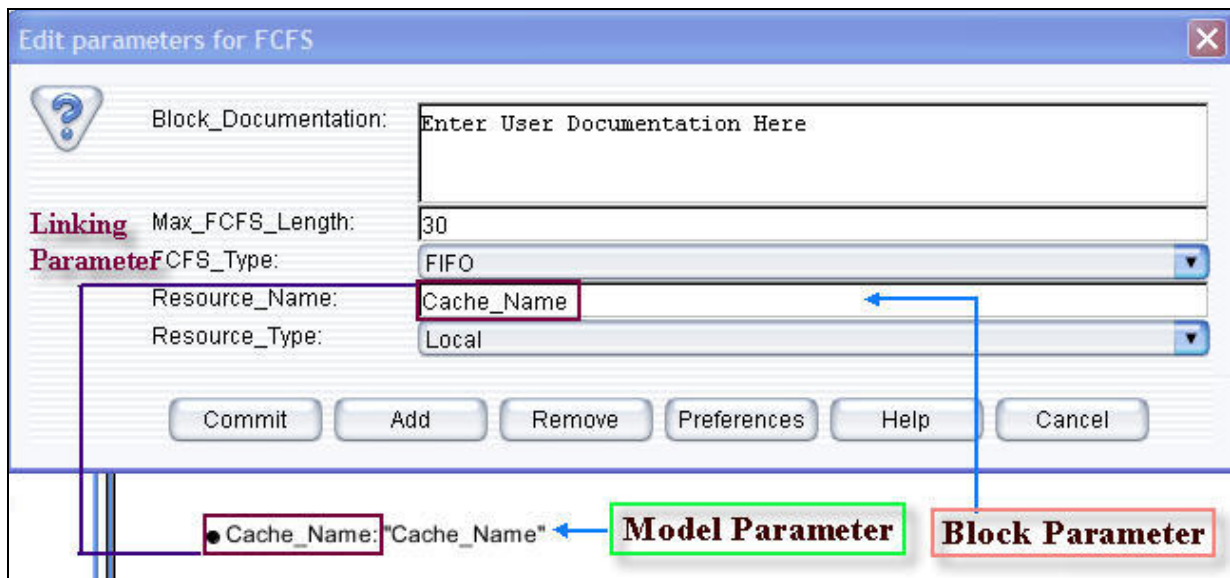


Figure 11. Linking Parameter

4.4.6 Block Documentation

Every block in VisualSim contains block documentation. To view the block documentation right click the block and select **Documentation > Get Documentation**.

User can create documentation for the block. To create a new document, right click the block and select Open Block. A new BDE is opened. Right click in the white space and select **Documentation > Customize Documentation**. Enter the new documentation details and click **Commit**. Save the model.

4.4.7 Icon Display value

By default, the block icon has the name of the block instance. This is unique in the model window. It is possible to display something different by adding a line to the XML as follows:

```
<display name="This is a test of the display system."/>
```

Where the item in "" is the value to be displayed on top of the icon. In this case, the Block Instance name is replaced with this value.

4.4.8 Tooltip value

It is possible to customize the tooltip, which is the string that appears when you move the mouse over a block. To do this, add a parameter called `_explanation`, with a default value without any "" and class as `VisualSim.kernel.util.StringAttribute`. The default value is displayed as the tooltip.

4.4.9 Creating Generic Port Icon

Port icons are dynamically created in VisualSim during the block instantiation on the Block Diagram Editor. The icon and color for Input, Output, Input/Output, and none port types are fixed and cannot be modified by the user. For a number of reasons, the user might want to keep the look of the port different from the standard view. A generic icon of rectangular shape and green fill is provided. The port icon looks the same for input, output, and input/output. The users can modify their port icon to this generic type by doing the following:

1. Drag a block into the BDE.
2. Right-click on the port and select "Configure".
3. Now click Add.
4. Enter the following information.
 1. Name: `_icon` ; Value: `true`; Class: `VisualSim.kernel.util.StringAttribute`
5. Click OK.
6. Click OK.
7. Now, you see that the port icon has changed to a green rectangle.

You can do the same thing by updating the xml file:

```
<port name="input" class="VisualSim.actor.TypedIOPort">  
  <property name="input"/>  
  <property name="_icon" class="VisualSim.kernel.util.StringAttribute" value="true">  
  </property>  
</port>
```

You need to add the property name `_icon` with the associated class and value to each port that needs to be converted to this generic icon.

5 Hierarchical Block Semantics

5.1 Using Hierarchical blocks

A Hierarchical block is a container of a number of basic and other Hierarchical blocks. A hierarchical block is used when the Editor Window runs out of space, or combines blocks that perform a specific function. Each level of a Hierarchy must have the same simulator. Levels below and above this Hierarchy can have a different simulator, as far as they conform to the simulator rules.

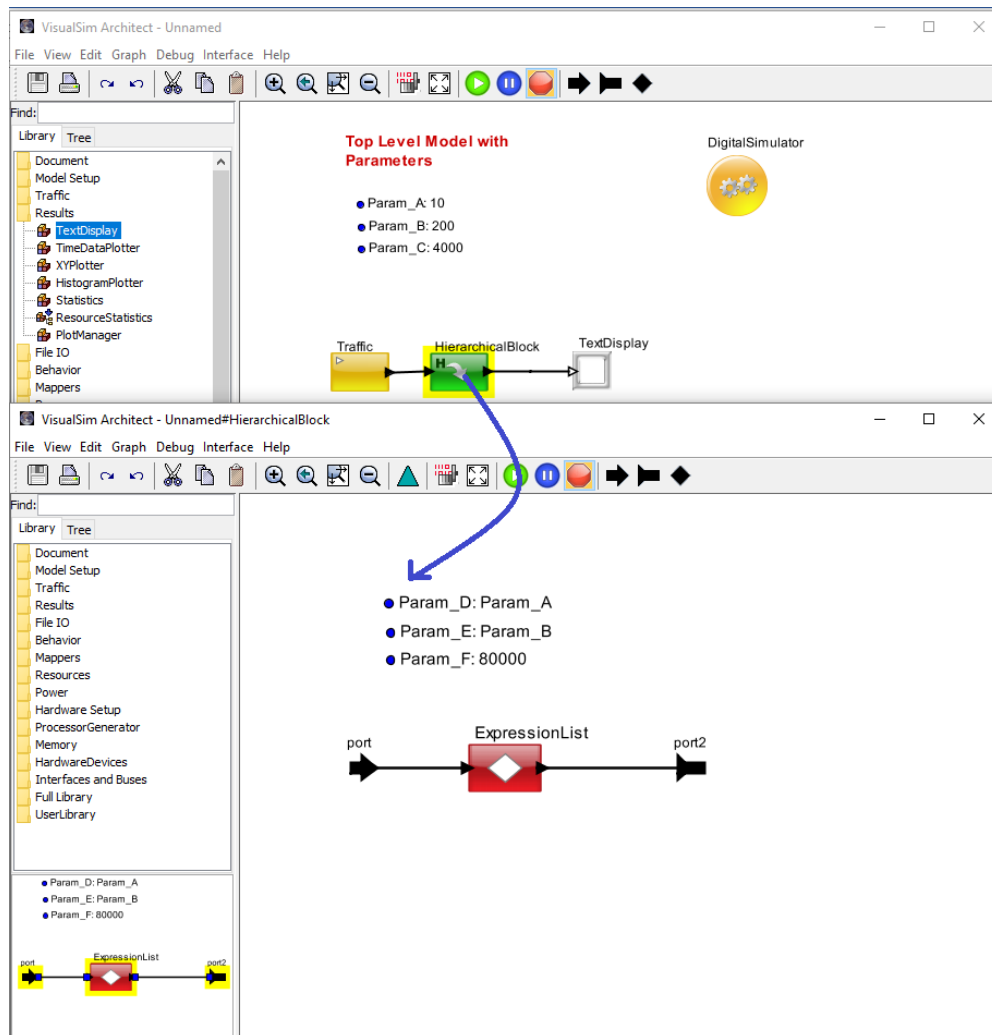


Figure 12. Hierarchical Block -> Open Block

To create a hierarchical block, drag "Hierarchical Block" from the Library Full Library > Model> Hierarchical Blocks into an existing BDE window. To view the inside of the Hierarchical block, right-click the icon and select "Open Block". Select the input and output Toolbar Icons to add input and output ports. These are displayed as input/output ports at the parent level model. Example of a simple Hierarchical Block is shown in Figure 13.

A simple Hierarchical Block looks similar to the below image:

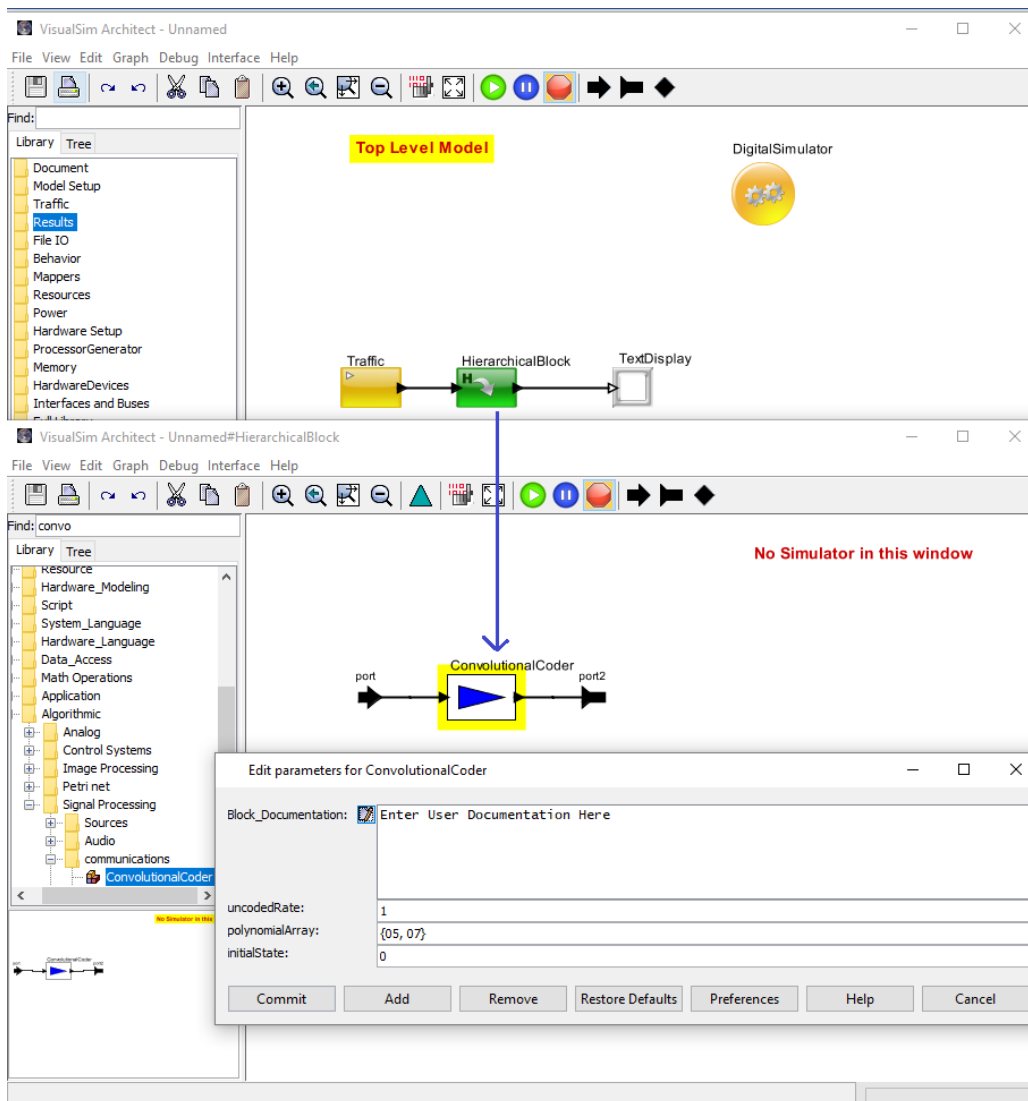


Figure 13. Adding Blocks to a Hierarchical block

Port Type (input (input), output (output)) are set by right-mouse click in white space or by selecting the icons from Menu/Toolbar. See notes on "Configure Ports" for more details.

Simulator Type None is required if the Hierarchical Block is using the same time semantics as the parent window. For example, this block is a Digital and parent is Digital. Mixed domain modeling requires a simulator to be defined with the hierarchical block and is discussed as separate topics. For example, a DSP Algorithm (Untimed Digital Simulator) can exist within a Digital.

In terms of model execution, Hierarchical blocks initialize, the first time they receive an input Token. In terms of animation, one can animate a single hierarchical block, using the same procedure as a flat model topology.

5.2 Model Execution Semantics

The Digital domain execution is a sequence of synchronous block execution between asynchronous time. This means that blocks with no delay are all executed at the same time (synchronous time) in the flow order. When a flow encounters a relation or a branch, it returns to the last branch and picks another flow to execute. It continues to do this until no more blocks can be executed at that time. At that point, it looks at the Master calendar and determines the next time point where there are asynchronous events. VisualSim schedules all delays and events on a master calendar queue in the Digital domain. All events executed on the master calendar queue are deterministic, meaning that the simulation executes the events, whether synchronous or asynchronous, in the same order each time the simulation is run. This is important for model development, repeatability during model validation, and obtain the same timing results for every run.

Synchronous Events: Synchronous events occur at the same simulation time, meaning more than one event is scheduled on the calendar queue for the same simulation time.

Asynchronous Events: Asynchronous events occur at a future simulation time, relative to the current simulation time and by implication there are no outstanding synchronous events.

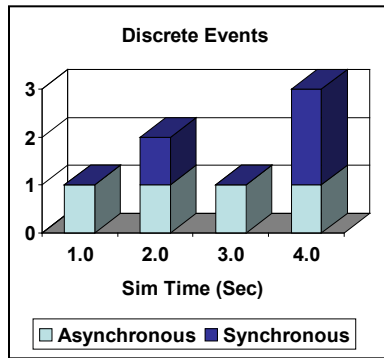


Figure 14. Model Execution Semantics

5.3 Model Execution Flowchart

This figure depicts the overall model execution flowchart which combines the Model Execution semantics and Block Execution semantics, shown in the previous two pages.

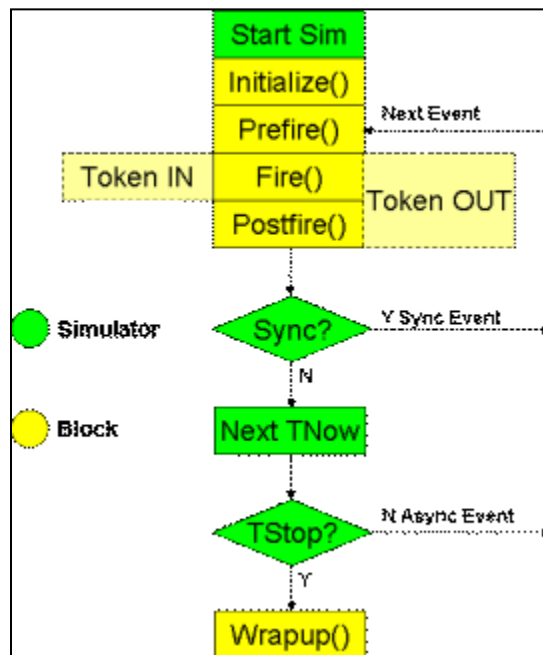


Figure 15. Model Execution Flowchart

5.4 Create Sub-Model

This feature converts this block into a Sub-model or class. A class is a master version of the block. This class can be instantiated multiple times in the model. Changes made to this class block (identified by a blue halo), are replicated to all linked instances. The information in the XML for the instances are all linked to this class block. More information on this is provided by the Sub-Model documentation page.

6 Dynamic Instantiation

6.1 Introduction

VisualSim includes a number of *Advanced Function Blocks*, that operate on the structure of the model rather than on data. These higher-order components help significantly in building large designs where the model structure scales. The most important of them is the Dynamic Instantiation. All other higher-order or Hierarchical blocks are considered experimental and are not guaranteed to work all the time. Using this block, the model can scale to any number of instances of an identical component by varying a parameter value. Each instance can have parameter values that are unique and can be accessed uniquely by an instance parameter.

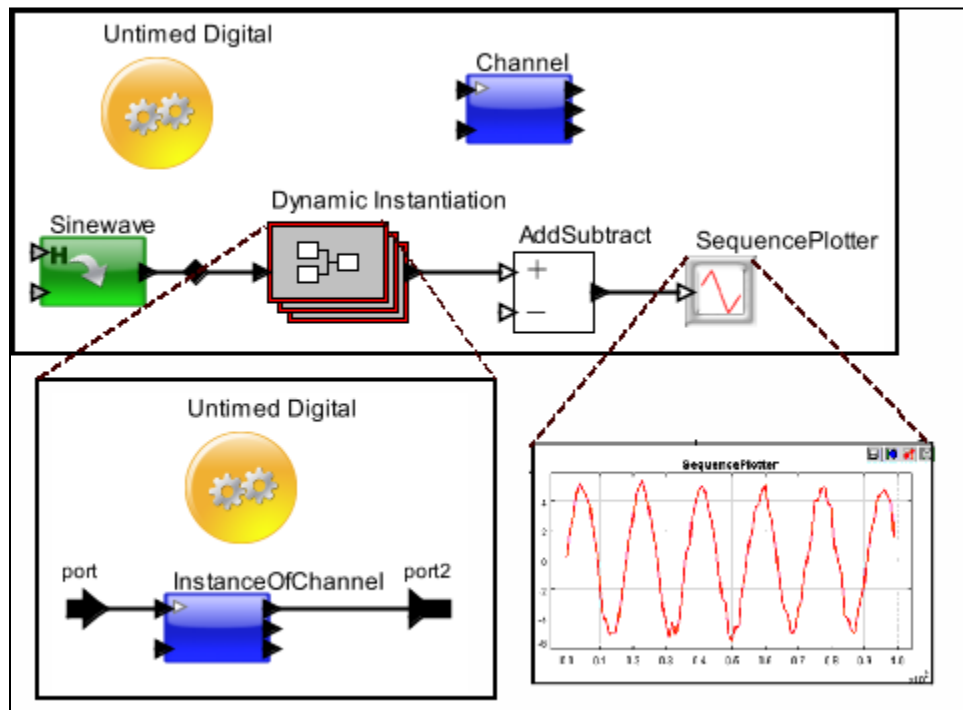


Figure 16. A model using the Dynamic Instantiation block

6.2 Example

Consider a model which has the five instances of the Channel class wired in parallel. This model has the feature that the number of instances is hardcoded into the diagram. It is awkward, therefore, to change this number, and particularly awkward to create a larger number of instances. This problem is solved by the Dynamic Instantiation block. A model equivalent to that is created using the Dynamic Instantiation block as shown in Figure 1616.

The above figure shows a model using the Dynamic Instantiation block which permits the number of instances of the channel to change by simply changing one parameter.

The Dynamic Instantiation is a hierarchical block into which we have inserted a single instance of the Channel.

The Dynamic Instantiation block has two parameters, *nInstances* and *instance*, as shown in the below figure.

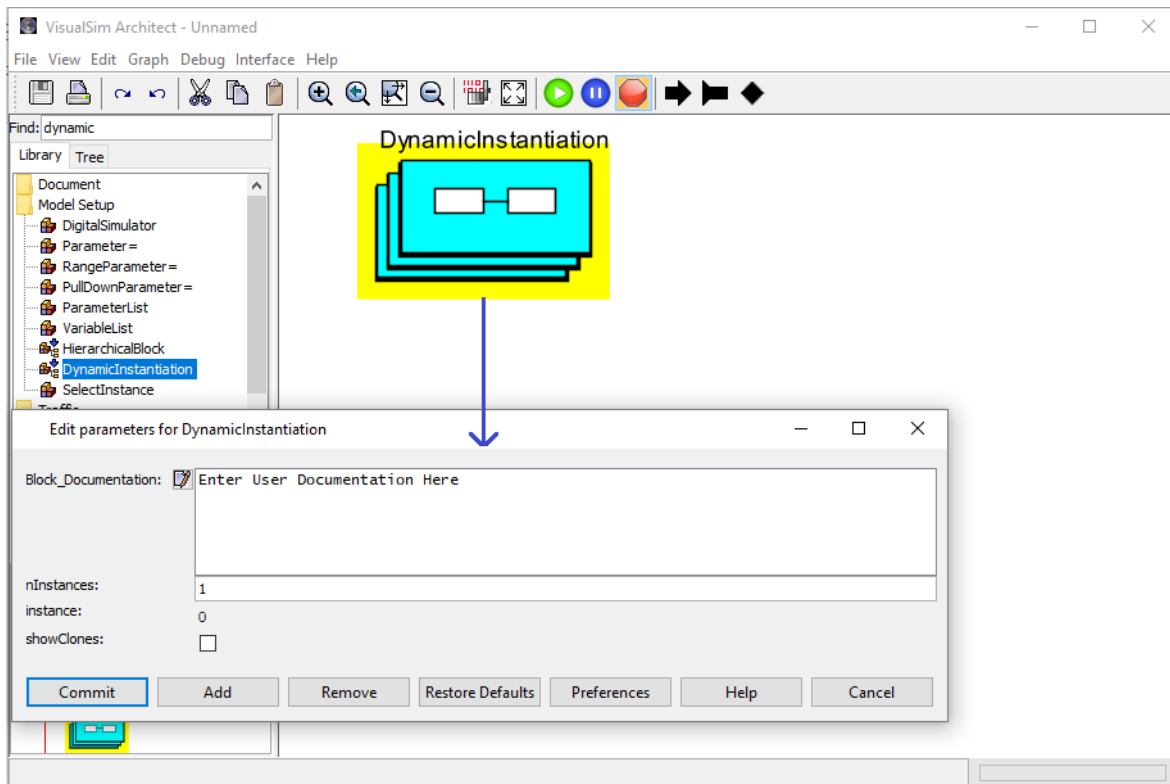


Figure 17. Configure Parameters for Dynamic Instantiation

The first parameter of the Dynamic Instantiation block specifies the number of instances while the second parameter is available to the model builder to identify the individual instance.

The first of these specifies the number of instances to create. At run time, this block replicates itself *nInstances* parameter value, connecting the inputs and outputs to the same sources and destinations as the first (prototype) instance. In Figure 16, notice that the input of the Dynamic Instantiation is connected to a relation (the black diamond), and the output is connected directly to a multiport input of the AddSubtract block. As a consequence, the multiple instances are wired in a manner similar to the above figure, where the same input value is broadcast to all instances, but distinct output values are supplied to the AddSubtract block.

The model is better in Figure 16 because now we can change the number of instances by changing one parameter value. The instances can also be customized on a per-instance basis by expressing their parameter values in terms of the *instance* parameter of the Dynamic Instantiation block. Try, for example, making the *noisePower* parameter of the InstanceOfChannel actor depend on *instance*. For example, set it to "instance * 0.1" and then set *nInstances* to 1. You see a clean sine wave when you run the model.

6.2.1 How To

Dynamic Instance (DI) block is located in the **Full Library > Model > Hierarchical Block**. Use this block in the same way that a Hierarchical Block is used. The SelectInstance is located in the **Full Library > Model > Hierarchical Block** library. The SelectInstance is required on the input side and the output side of the DI block to indicate the specific instance to be accessed.

6.2.2 Requirements

To access each instance of the Dynamic Instantiation (DI) block, a SelectInstance block must be placed on the input and output of the DI block. On the input, this block picks the instance from a value in the incoming Field or Variable. On the output, the block combines multiple instances to an output.

6.2.3 Example of the Dynamic Instantiation

To view an example of a Dynamic Instantiation model in VisualSim, view the [Dynamic Instantiation Usage Page](#) here.

Examples are located in doc\Training_Material\How_to_tasks\DI directory. One of these examples is described here.

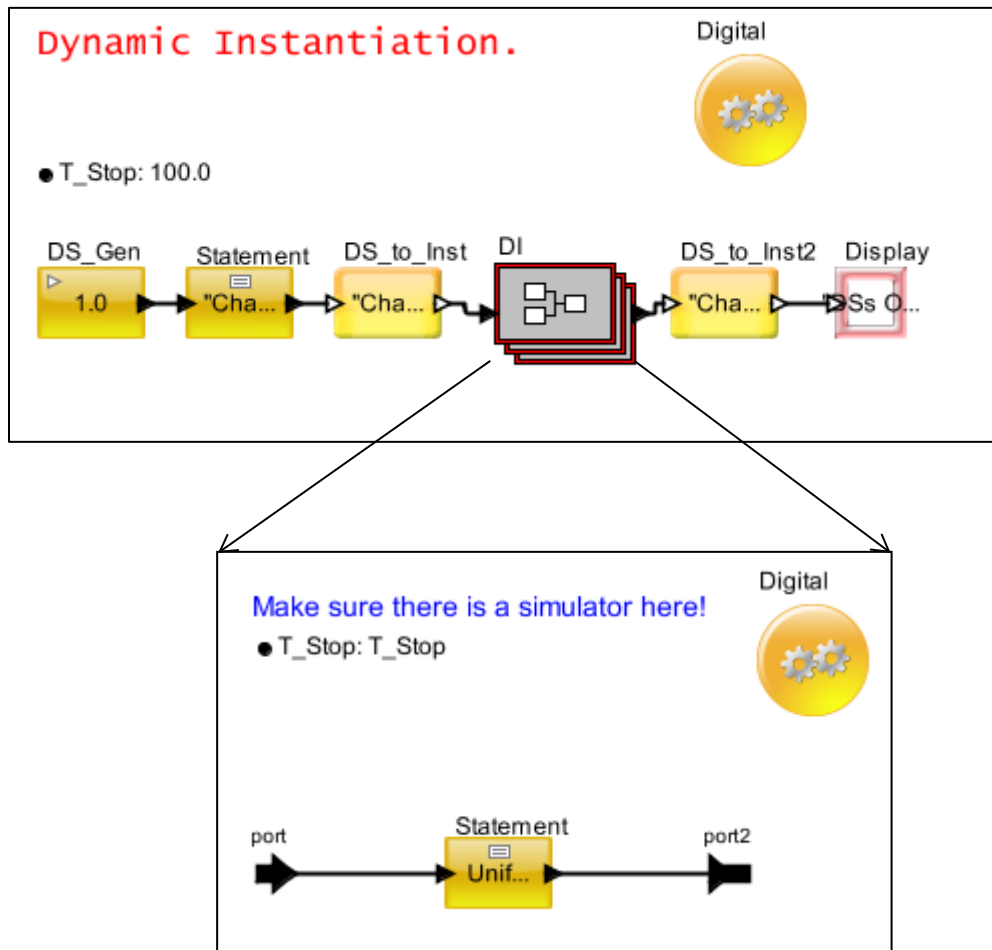


Figure 18. Dynamic Instantiation Example in VisualSim

In this simple model, there are 4 instances of the DI block. A traffic generator creates DS. The field "Channel" of the Stop_n_Wait DS provides a random number between 0 to 3. In the SelectInstance block, the value of the Channel field specifies the instance that this DS is sent to. The output of the DI also has a SelectInstance block. This combines the DS coming from all the

instances and sends them out on a single instance link, as is visible from the Display output. Also notice that any parameters can be added just as in the Hierarchical Block.

7 Library Folder Organization

In VisualSim, blocks are grouped together based on functionality and arranged in the Library.

VisualSim contains the following libraries:

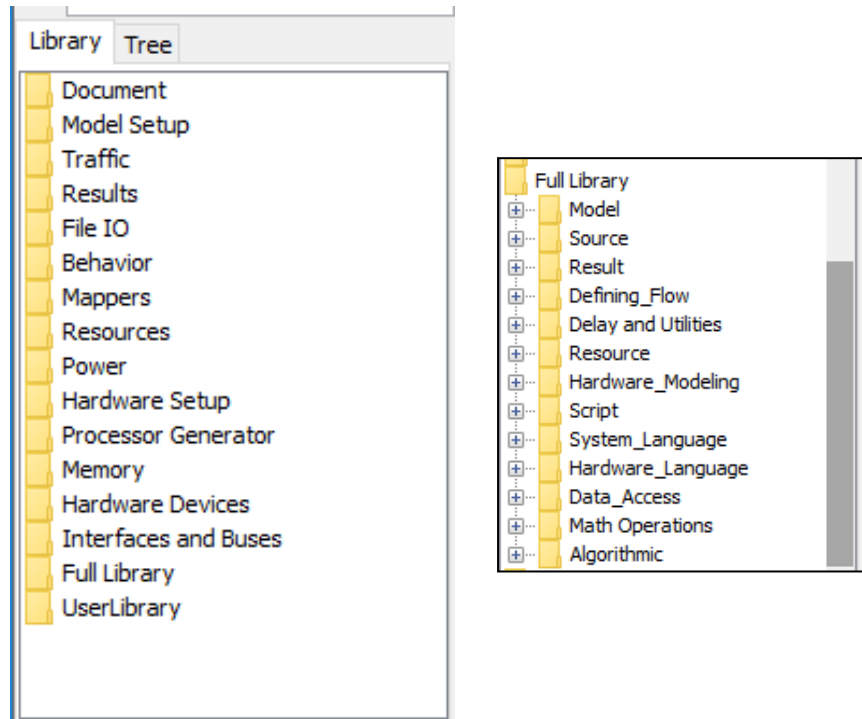


Figure 19. Library Folder Organization

7.1 Model / Document / ModelSetup

Model / Document / ModelSetup are overhead components used to setup the model. These include drawing tools, simulators, Variable, parameters, hierarchical, and FSM blocks.

Draw Tools – Contains Annotation, Rectangle, Eclipse, Model Id, Image Import, and so on.

Parameter – Used for analyzing the performance of the system by fixing their value for a simulation run.

Simulator – Translates the graphical depiction of the system into a form suitable for simulation execution, and executes simulation of the system model.

Variable – Variable that is initialized and updated during the simulation.

Hierarchical – Grouping a set of functional blocks that combine to define a function or device.

FSM – Basic block for Finite State Machine operation.

Utility – Allows the user to determine the current values of Variable and the list of virtual connections. It also has content for checking the type and the units.

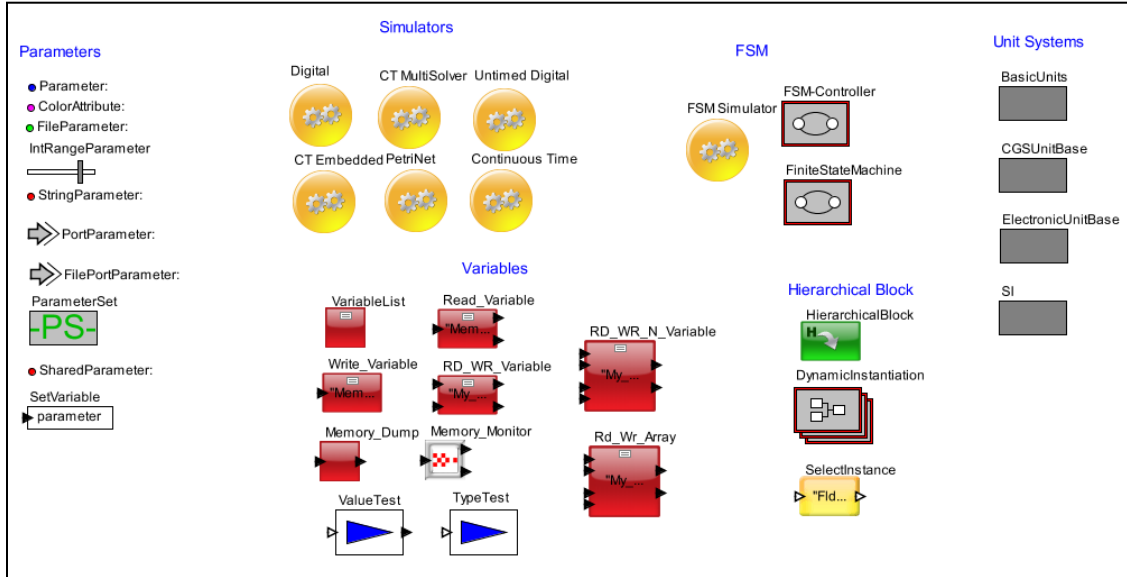


Figure 20. Blocks in Document/ Model / ModelSetup Library Folders

7.2 Traffic / Source

User can generate traffic using a standard distribution, sequences, trace files, clocks, and custom distributions.

Clock – Generate all possible clock inputs.

Event – Generate the input according to the Event set.

File Import – Input can be generated according to the file input,

Traffic – Generate input as per the specified DS and time distribution.

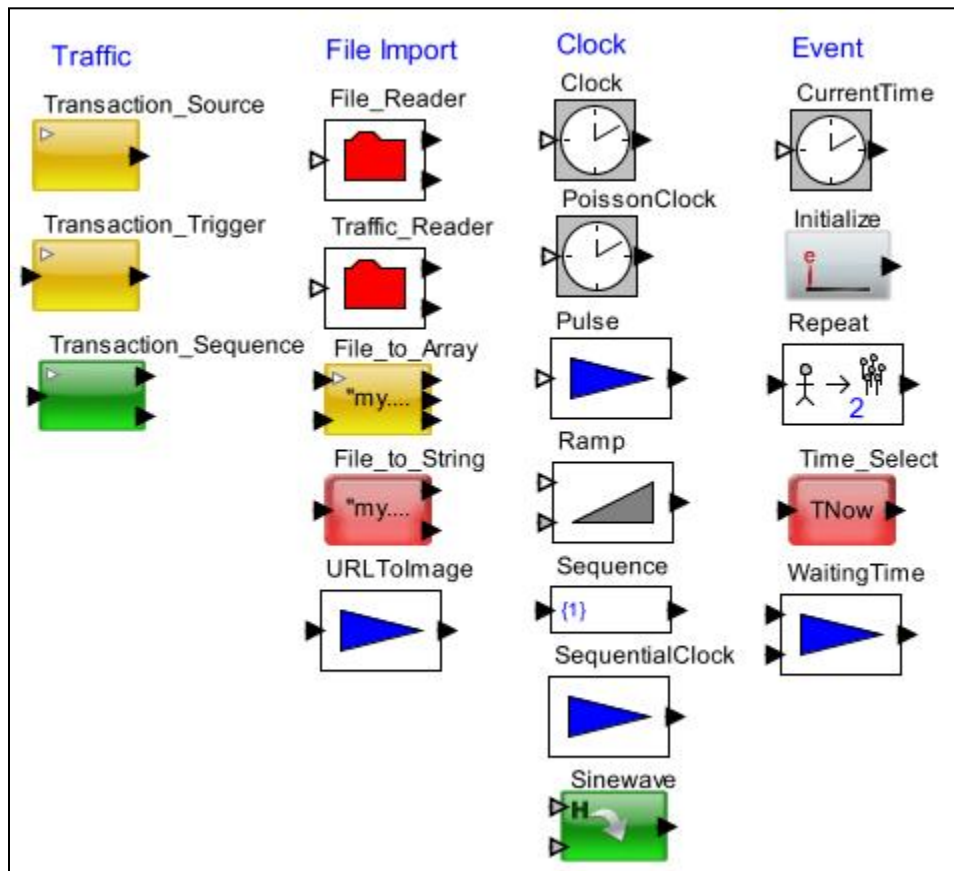


Figure 21. Blocks in Source Library

7.3 Results

The Results Library is used to evaluate the effectiveness of the system model and to estimate the performance.

Plot Manager- Link to the Post Processor.

3D Interactive Creator- Create visual and animated displays.

Statistics Generator - Generate statistics on all resources and hardware blocks.

Plotter - A complete collection of Array plotter, Bar Graph, Histogram plotter, matrix Viewer, Real-time plotters, and so on.

Text – A complete collection of text displays, monitor value, file writers, and so on.

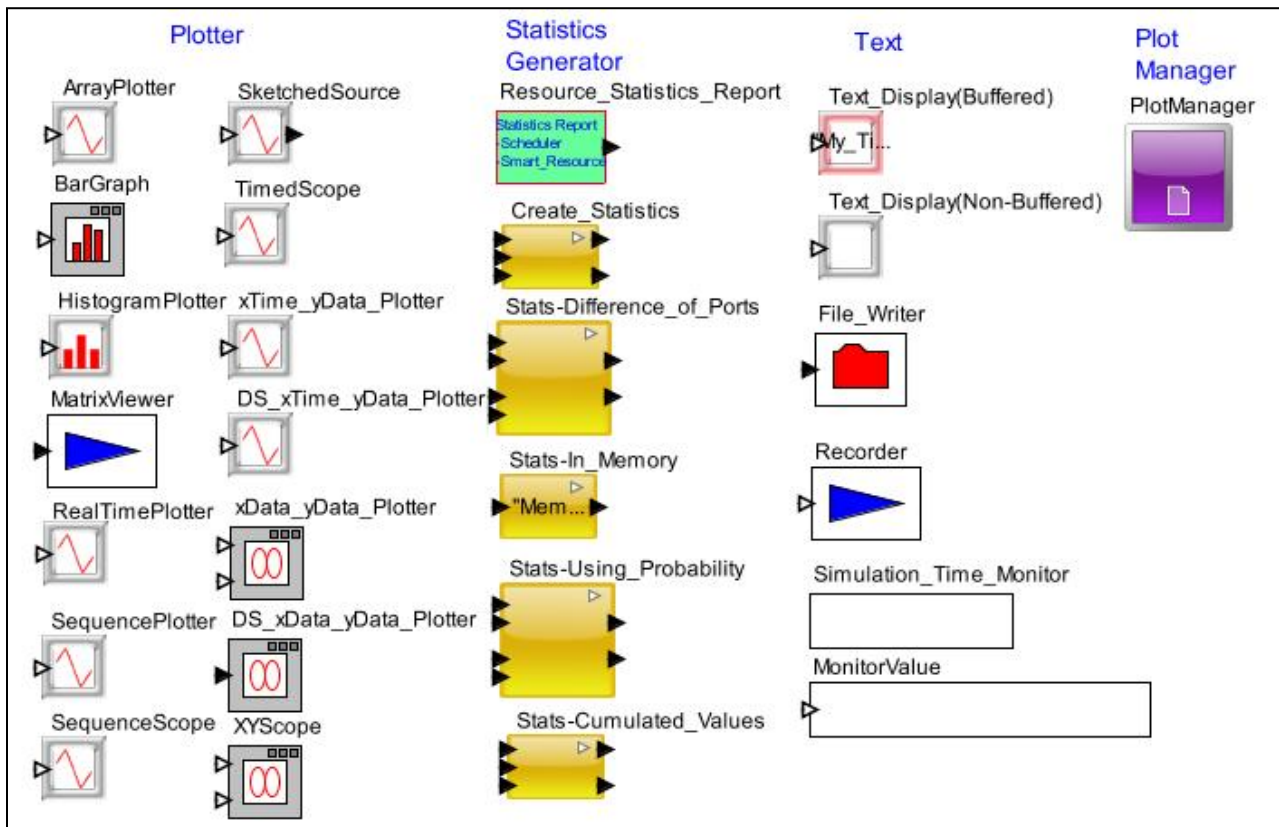


Figure 22. Blocks in Result Library

7.4 Behavior

Behavior is used in

- defining expressions,
- evaluating assignments,
- making control decisions and assigning values to a Field or Variable,
- randomizing Field values,
- calculating processing cycles on a scheduler or Queue blocks,
- computing statistics such as latency (TNow - TIME), utilization and throughput and
- creating assumption values.

Control Flow blocks are used to makes decisions, create loops and take branches.

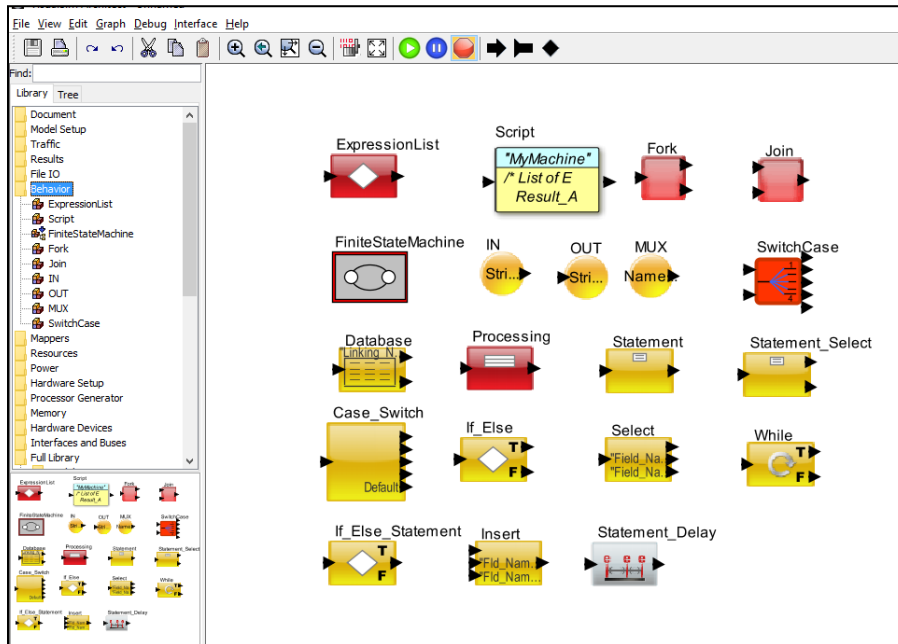


Figure 23. Control Flow blocks

Access the ExpressionEvaluator from the File->New->ExpressionEvaluator. This window allows the user to experiment with a sequence of math and logic expression.

ExpressionEvaluator- Enter a sequence of assignment statements that are executed in order and the output is controlled by an evaluating an expression.

Script- Programming block to describe behavior using the VisualSim script format and RegEx functions.

Database block - A high-performance lookup table with search, read/write/erase functionality.

Processing- Enter a sequence of assignment statements to be executed in order.

Basic Processing – Contains all decision making and control flow blocks such ExpressionList, Case_Switch, and while.

Virtual Connection – Connections between different parts of the model using names. Two of these Virtual Connection blocks- IN and OUT are in Behavior. The other two blocks are located in the Virtual Connection Folder in Defining Flow Folder.

FSM – Basic block for Finite State Machine operation.

7.5 Mappers

Mapper blocks define the connectivity between the behavior flow and the architecture flow, and within the architecture flow using a named connection. The connection can be static, that is to a single scheduler, or dynamic is based on the value of the input field content.

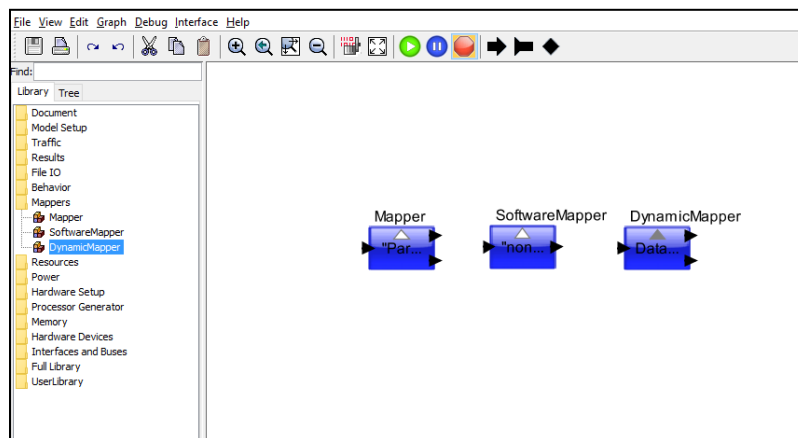


Figure 24. Mappers

7.6 Resources

- Resources model the physical aspects of the system. In the performance of a system design, a model platform is described using the physical components such as **Queue**, **Schedulers**, **Flow Control**, and **Associated Arbitration Policies**. There are two ways to define resources - **Active** and **Passive**. Active resources consume time while passive resources consume quantity. Passive resources can be created using **Arrays**, **Database** block, or **Quantity-shared Resources**. All other blocks under resources are categorized as Active.

- **Queues and Servers** – Queues with advanced content handling for both time-based and event-based. Define complex arbitration schemes that are dependent on external activity for timing and pop.
- **Channel** - The Channel block can be used to model a DMA channel, wireless channel or a bus. The channel block contains a queue and multiple channels.
- **Event Queue** - Queue stores the incoming data structure and pop it out on the arrival of a trigger. The blocks in this folder have single and multiple concurrent queues with priority.
- **Timed Queue** - Queue stores the incoming data structure and pop it out after a pre-determined delay. The blocks in this folder have single and multiple concurrent queues with priority enabled. Two variations of these blocks are also available- one with a single queue and multiple parallel time resources; and another scheduler that supports slot-based time allocation.
- **Quantity Based** - A polymorphic quantity-shared resource for N-identical resources, which enqueues input tokens in either a FIFO, or LIFO, order depending on the "Queuing_Discipline" parameter attribute.
- **SystemResource** – Defines the execution of a process in a data structure in a variety of pre-defined scheduling schemes. This block separates the behavior flow or data flow from the architecture definition. SystemResource block can be used to link multiple concurrent behavior flows into a single block.

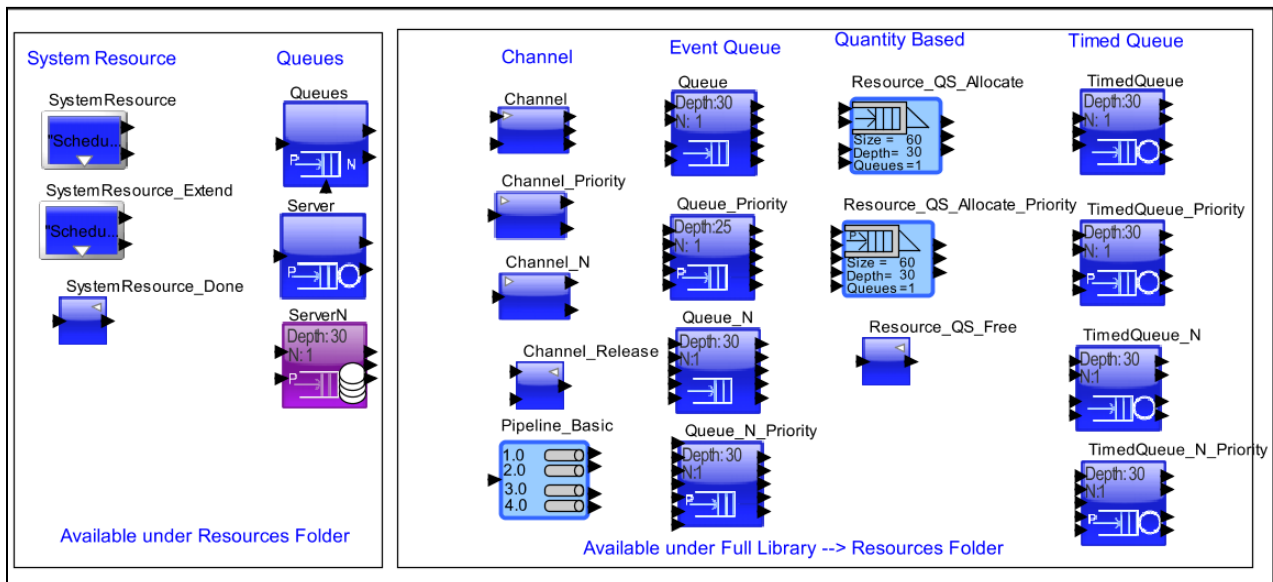


Figure 25. Blocks in Resource library

7.7 Power

Power Modeling Library blocks are available in this library folder.

PowerTable – Blocks are used to evaluate the following for individual devices - battery discharge, instantaneous power, average power, and so on.

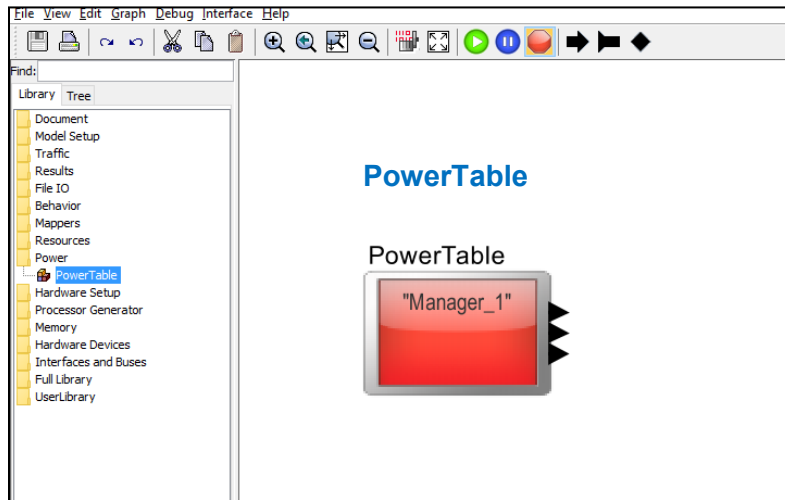


Figure 26. Power

7.8 Hardware Setup

The Hardware setup provides the list of library blocks that must be or may be included as part of a cycle accurate system model. ArchitectureSetup block handles all the address mapping, routing, plotting, statistics and debugging for the Hardware Modeling components. There can be multiple ArchitectureSetup blocks in a model. Each block instance must have an unique name. All Bus and Hardware blocks must be associated with one of the ArchitectureSetup.

Device Interface block helps the designer to model custom device interfaces and custom hardware components. Hardware setup block set also includes few utility library blocks such as VCD writer, Timing Diagram generator, and clock align.

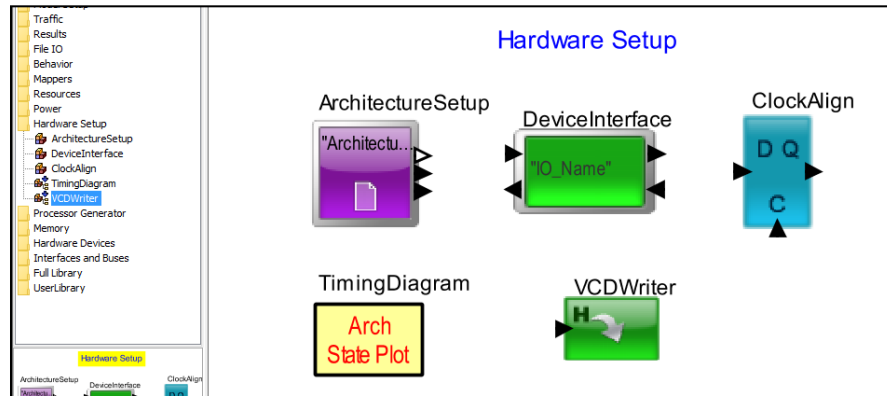


Figure 27. Hardware Setup

7.9 Processor Generator

The Processor block set is used to model variations of commercial and proprietary processors. The Processor generator block set also includes an Instruction set block. The Instruction_Set block can be used to define a set of instructions for each execution unit of the processor. It can also bunch together execution units with a common reference name. This reference name can be used in the Processor pipeline definition. The Processor block can have cache definitions within and also refer to an external cache or memory blocks. The last block is the Task_Generator block that generates an array of instructions based on the profile provided in the Instruction_Mix_Table.

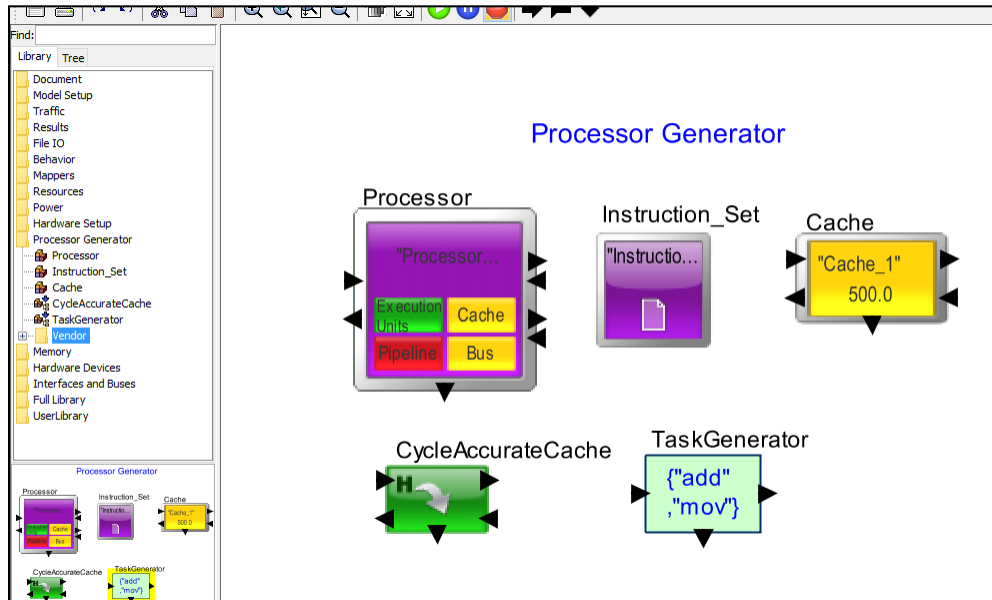


Figure 28. Processor Generator

7.10 Memory

This library folder has the configurable libraries of Memory and Memory controllers. Types of Memory technologies supported are SRAM, SDRAM, DDR, DDR2, DDR3, LPDDR, LPDDR2, LPDDR3, and LPDDR4.

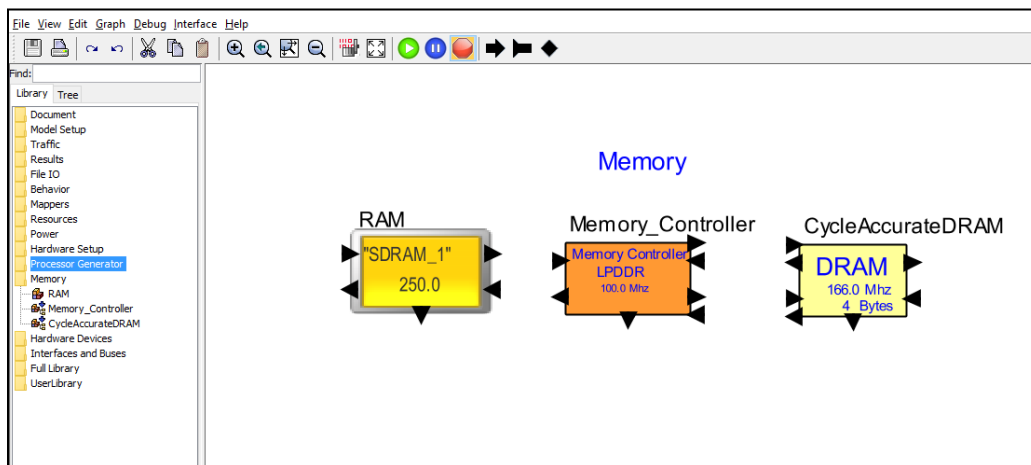


Figure 29. Memory

7.11 Hardware Devices

Hardware Device blockset includes library blocks of Custom Bus arbiter, Custom Bus Interface, DMA Controller, Blocking Switch, Bridge, and Switch.

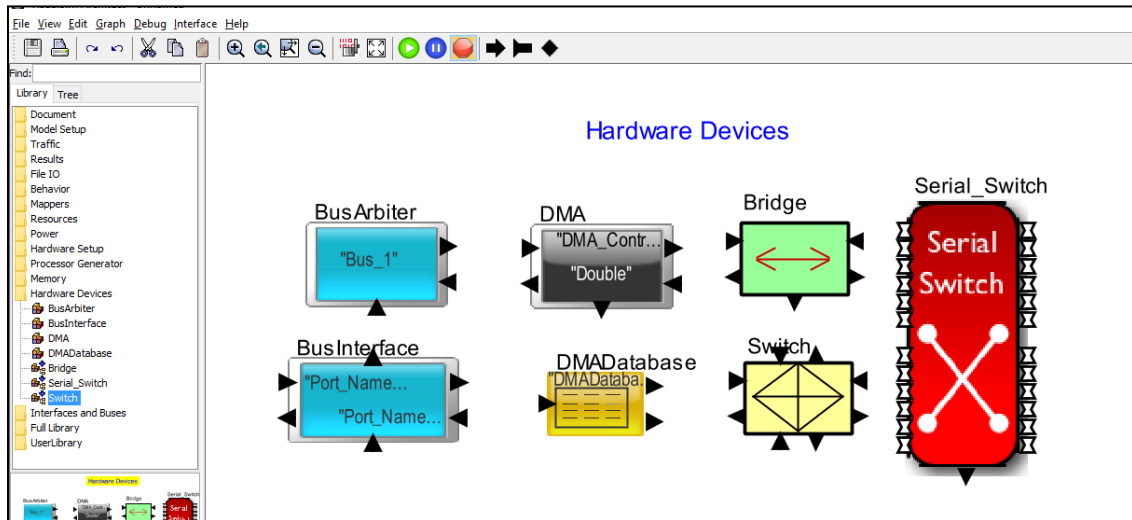


Figure 30. Blocks in Hardware Devices

7.12 Interfaces and Buses

Interfaces and Buses blockset includes list of advanced bus and interface technologies. This includes library blocks of AFDX, AMBA, AVB, Autosar, CAN, Switched Ethernet, Fibre Channel, FireWire, FlexRay, PCI, PCIe, RapidIO, Spacewire, TTEthernet, Wireless, and networking library blocks.

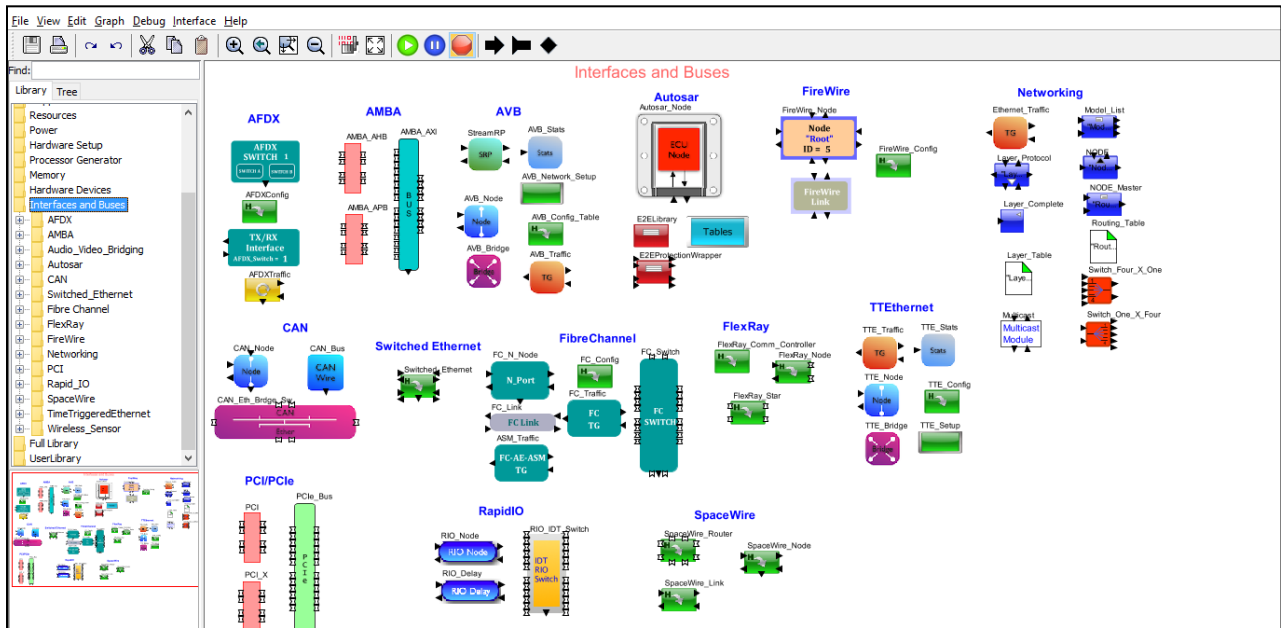


Figure 31. Interfaces and Buses

The Wireless Sensor networks library contains a separate simulator that allows communication wirelessly between the channel and the operating blocks. This library contains different antennas and channels.

7.13 System_Language

The System_Language blocks are available under Full Library > System_Language folder. These blocks provide an interface to easily import C code, applications written in C or C++, Python, MatLab, and Satellite Toolkit. The Interfaces require the licenses for MatLab and Satellite Toolkit.

7.14 Hardware Language

The Hardware Language blocks are available under Full Library > Hardware Language library folder. Interfaces are provided to run VisualSim in co-simulation with Verilog and SystemC. The Interfaces require the licenses for Verilog.

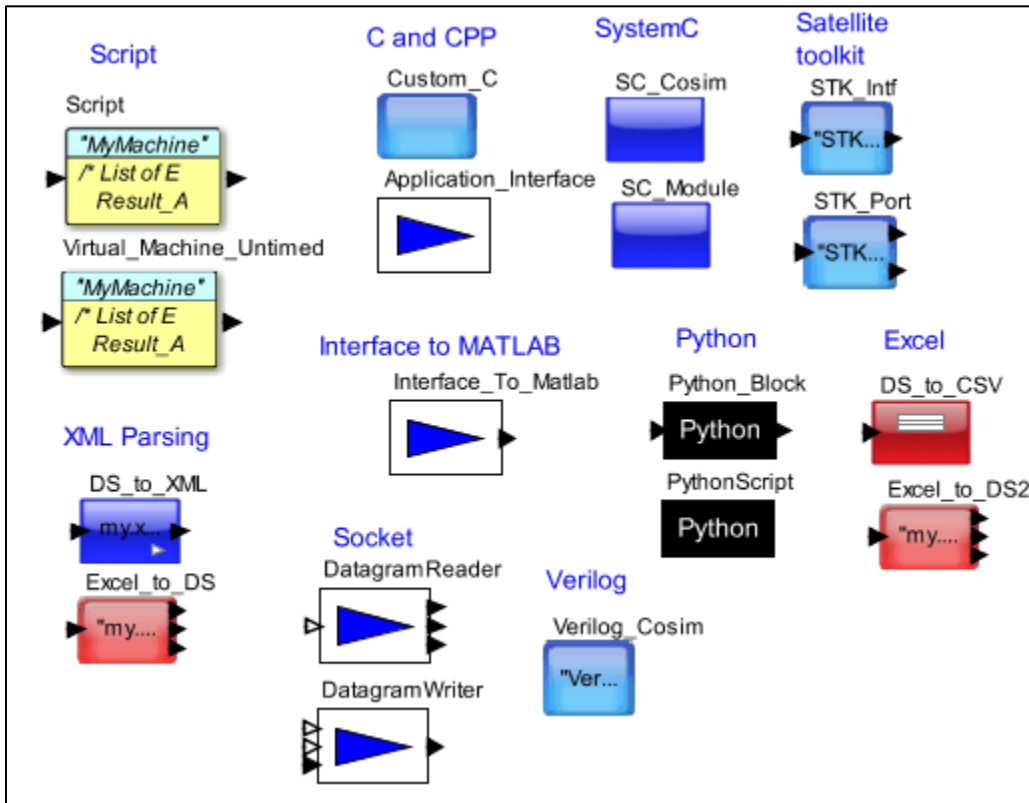


Figure 32. Interface Blocks

7.15 Math_Operations

The Math_Operations blocks are available in Full Library > Math Operations. This library contains Array, Boolean and Logic blocks that are required for the operation of system model.

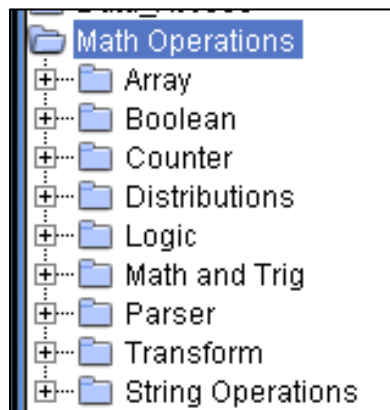


Figure 33. Math Operations Listing

7.16 Algorithmic

The Algorithmic blocks are available under Full Library > Algorithmic. This library contains blocks to generate events and wave-forms. It also contains image processing, Petri net, and signal processing blocks.

7.17 UserLibrary

The User Library is maintained in the \$User Home/.VisualSim/User_Library.xml file. Users can add Hierarchical folders with this Library. In addition, the user can add libraries using the Block Diagram Editor.

8 Block, Sub-Models (Classes) and Inheritance

8.1 Introduction

Blocks are the basic elements in VisualSim, used to construct a model. Blocks can be defined using Java, C/C++ enclosed in a Java Wrapper, Hierarchical block within a model, and a hierarchical block saved as a separate file called sub-model or class. Class and Sub-Model are the same and are used interchangeably.

One of the major capabilities in VisualSim is the ability to define block-oriented classes with instances and subclasses along with inheritance. The key idea is that you can specify that a component definition is a class, in which case all instances and subclasses inherit its structure. This improves modularity in designs. We illustrate this capability with an example.

Classes are especially useful when you need to instantiate a block multiples times in a model or used repeatedly in many models. This can be a component in your designs or a reporting utility.

Classes are the base entities. When the class is instantiated, the user can only modify the values of the parameters and not the topology or the existing list of parameters. The user can add additional details within the Instance. These details are maintained only for that particular model and does not affect the base Class.

If these new changes become the basis for another reusable block, then you can define this new block as a sub-class. The sub-class refers to the class for the basic details. Only the incremental details are stored in the sub-class.



A class or sub-class can be easily converted into a instance for use in a particular model. This is useful when a model needs to be shipped to another person that does not have access to the libraries.

The class also plays a significant role in the development of a user library. The following section discusses the construction of classes, use of the class in models, creation of libraries, and making the library in the Library Folder.

Before we get into the details, here is an example of the classes and the role they play in VisualSim modeling.

8.2 Example of Classes

Follow the steps to create the model:

1. Drag the Digital Simulator block from **Model Setup > Digital Simulator**.
2. Drag the Sinewave block from **Full Library > Source > Clock**.
3. Drag the SequencePlotter block from **Full Library > Result > Plotter**.
4. Create a Hierarchical block.
 - a) Click the New input port icon  available below the menu bar.
 - b) Drag the AddSubtract block from **Math_Operations > Math and Trig**.
 - c) Drag the Gaussian block from **Math_Operations > Distributions**.
 - d) Click the New output port icon  available below the menu bar.
 - e) Drag a parameter from **Model Setup > Parameter=**. Right click the parameter and select **Customize Name**. The Rename Parameter window is displayed. Now enter the name of the parameter as noisePower and enable Show Name.
 - f) Double click the parameter named noisePower and enter the value 0.01.
 - g) Now select all the blocks (Mentioned in points a to f). The selected blocks are highlighted in yellow color. Now click **Graph > Create Hierarchy**. The Hierarchical block is displayed. (To view the blocks, right click the Hierarchical block and select Open Block.)
5. Right click the Hierarchical block and select **Customize Name**. Rename the Hierarchical block as Channel.



Hierarchical block is referred as Channel block in following sections.

6. Configure the Ports for the Hierarchical as described below:

- a) Right click the Channel block and select Customize > Ports. The Configure Ports window is displayed as shown below:

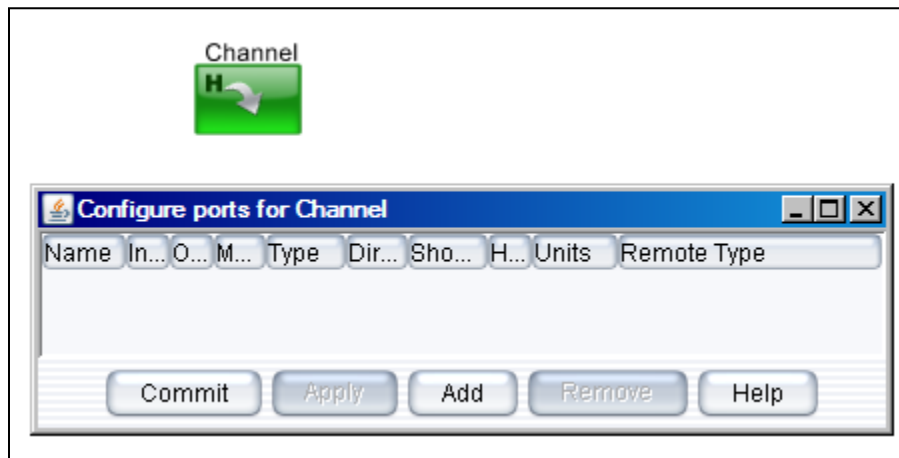


Figure 34. Configure Ports

- b) Click **Add** to add a new port.
 - c) Enter the name of the port in **Name**. For example, IN, OUT.
 - d) Enable the Input option in case of input port and Output option in case of Output port. Select the type if necessary.
 - e) Click **Commit** to submit.
7. Now connect the output of the Sinewave block to the input of Channel block.
 8. Connect output of the Channel block to the input of the SequencePlotter.
 9. The Channel Hierarchical block icon can be changed by doing a right click on channel->Appearance->Edit Cuostom Icon

Refer the following image for more details:

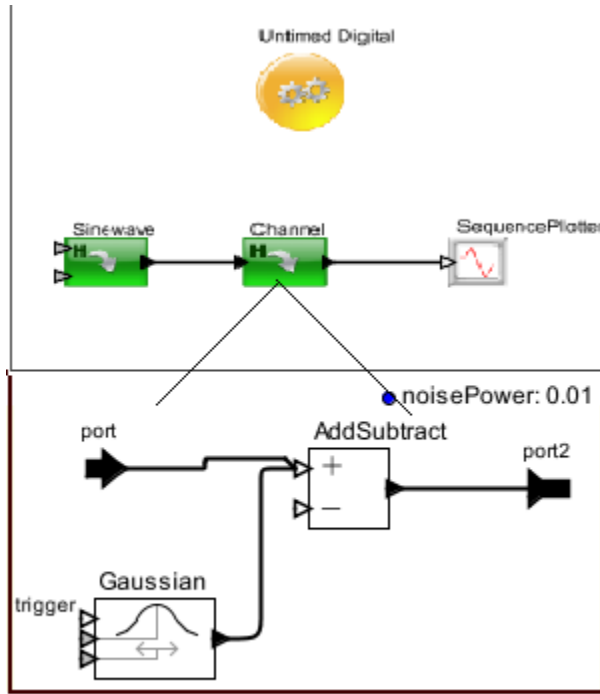


Figure 35. Hierarchical Model to create a Class

Consider the model in Figure 35. Suppose that we wish to create multiple instances of the channel, as shown in figure 36.

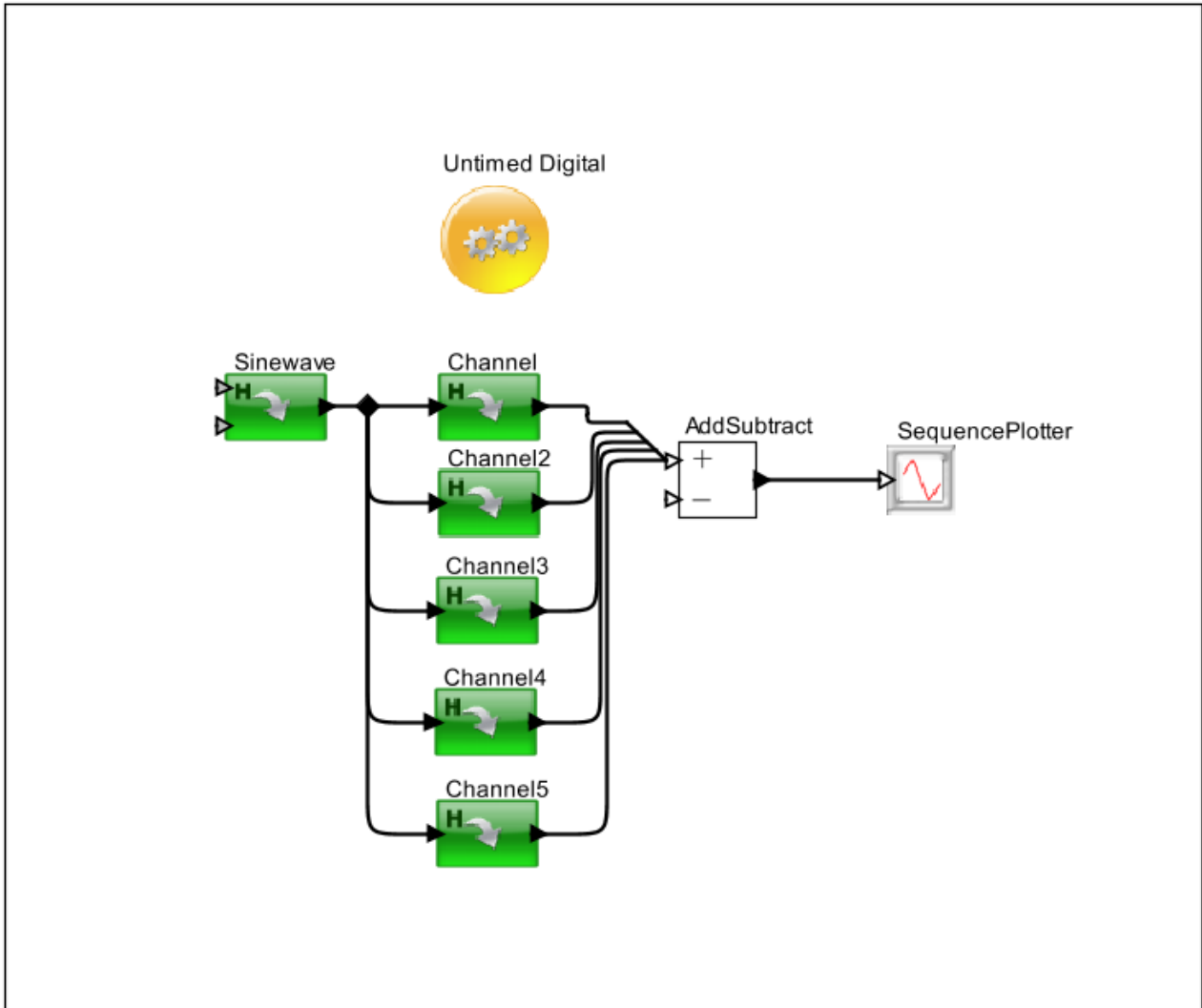


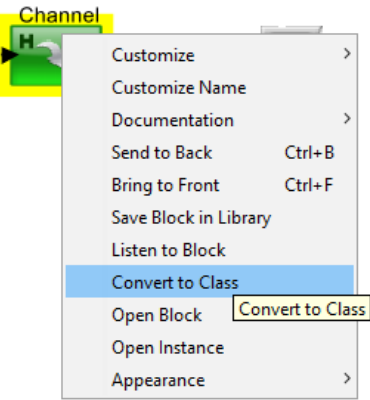
Figure 36. A poor design of a diversity communication system

The above is a poor design of a diversity communication system that has multiple copies of the channel that are defined.

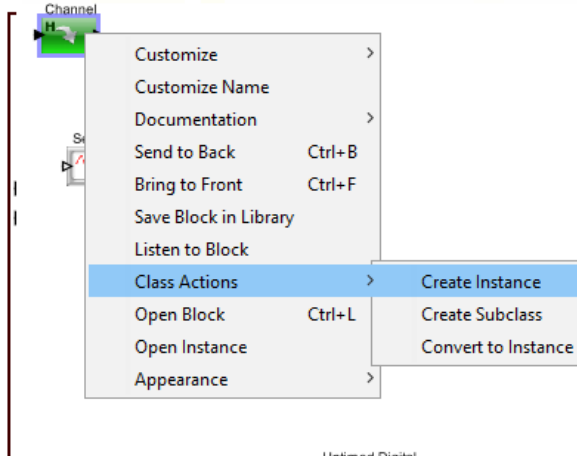
In the above figure, the Sinewave signal passes through five distinct channels (note the use of a relation to broadcast the same signal to each of the five channels). The outputs of the channels are added together and plotted. The result is a significantly cleaner sinewave than the one that results from one channel alone. However, this is a poor design, for two reasons.

First, the number of channels is hardwired into the diagram. We deal with that problem in the next section. Second, each of the channels is a copy of the hierarchical block in figure 36. This results in a far less maintainable or scalable model than we would like. Consider, for example, what it would take to change the design of the channel. Each of the five copies would have to be changed individually.

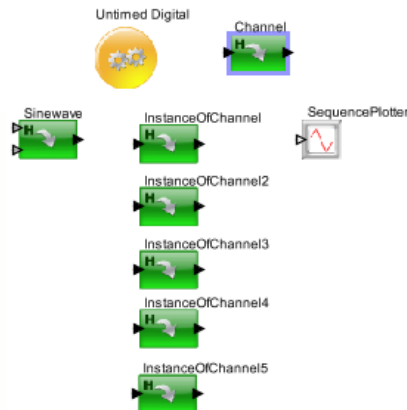
A better solution is to define a channel class or Sub Model. To do this, begin with the design in figure 35 and remove the connections to the channel, as shown in figure.



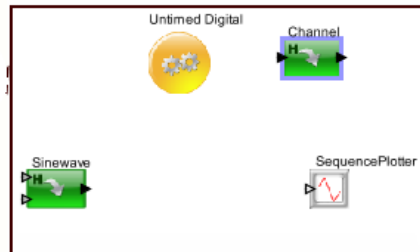
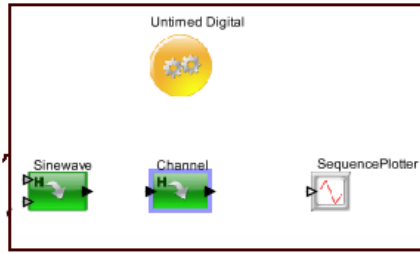
1. Model with connections removed



4. Create Instance



2. Model after channel is converted to class



3. Model after Class is moved to the top

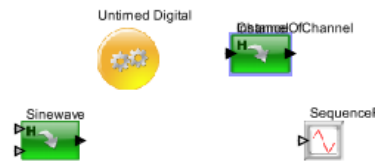


Figure 37. Creating and using a Channel Class

Then right click and select "**Convert to Class**". (Note that if you fail to first remove the connections, you get an error message when you try to convert to class. A class is not permitted to have connections.) The block icon acquires a blue halo, which serves as a visual indication that it is a class, rather than an ordinary block (which is an instance). Classes play no role in the execution of the model, and merely serve as definitions of components that must then be instantiated. By convention, we put classes at the top of the model, near the simulator, as they function as declarations.

After you have a class, you can create an instance by right clicking and selecting "Class Actions > Create Instance" or press Control-N. Do these five times to create five instances of the class, as shown in figure 37. It is in fact, a much better design and to verify this, try making a change to the class. For example, by creating a custom icon for it, as shown in figure:

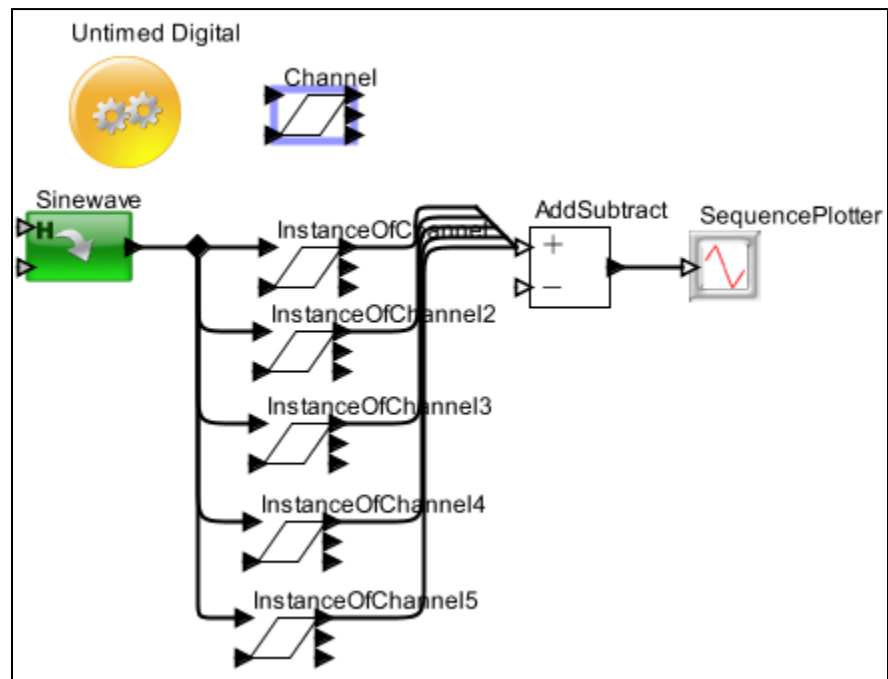


Figure 38. The icon changed for the class

Note that changes to the base class propagate to the instances of the class. A more subtle advantage is that the XML file representation of the model is much smaller, since the design of the class is given only once rather than five times.

If you look inside any of the instances (or the class), you find the same channel model. In fact, you see the class definition. Any change you make inside this hierarchical model will be automatically propagated to all the instances. Try changing the value of the noisePower parameter, for example.

8.2.1 Overriding Parameter Values in Instances

By default, all instances of a Channel have the same icon and the same parameter values. However, each instance can be customized by overriding these values. In the below figure:

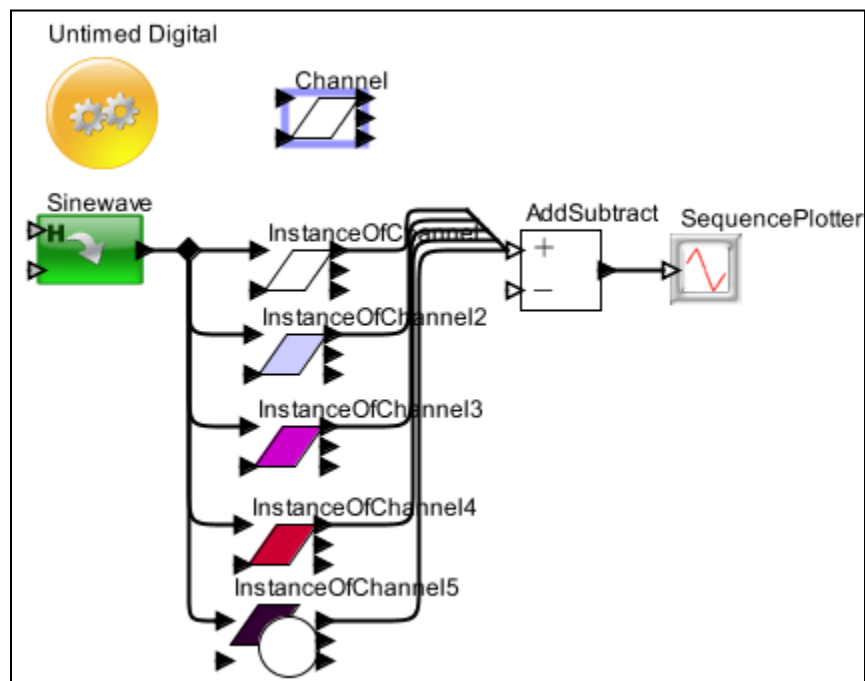


Figure 39. Model with the icons of the instance

The above figure shows a Model with the icons of the instance changed to override parameter values in the class.

For example, we have modified the custom icons so that each has a different color, and the fifth one has an extra graphical element. To do this, just right click the icon of the instance and select "**Appearance > Edit Custom Icon.**"

8.2.2 Subclass and Inheritance

Suppose now that we wish to modify some of the channels to add interference in the form of another sinewave. A good way to do this is to create a subclass of the Channel class, as shown in figure.

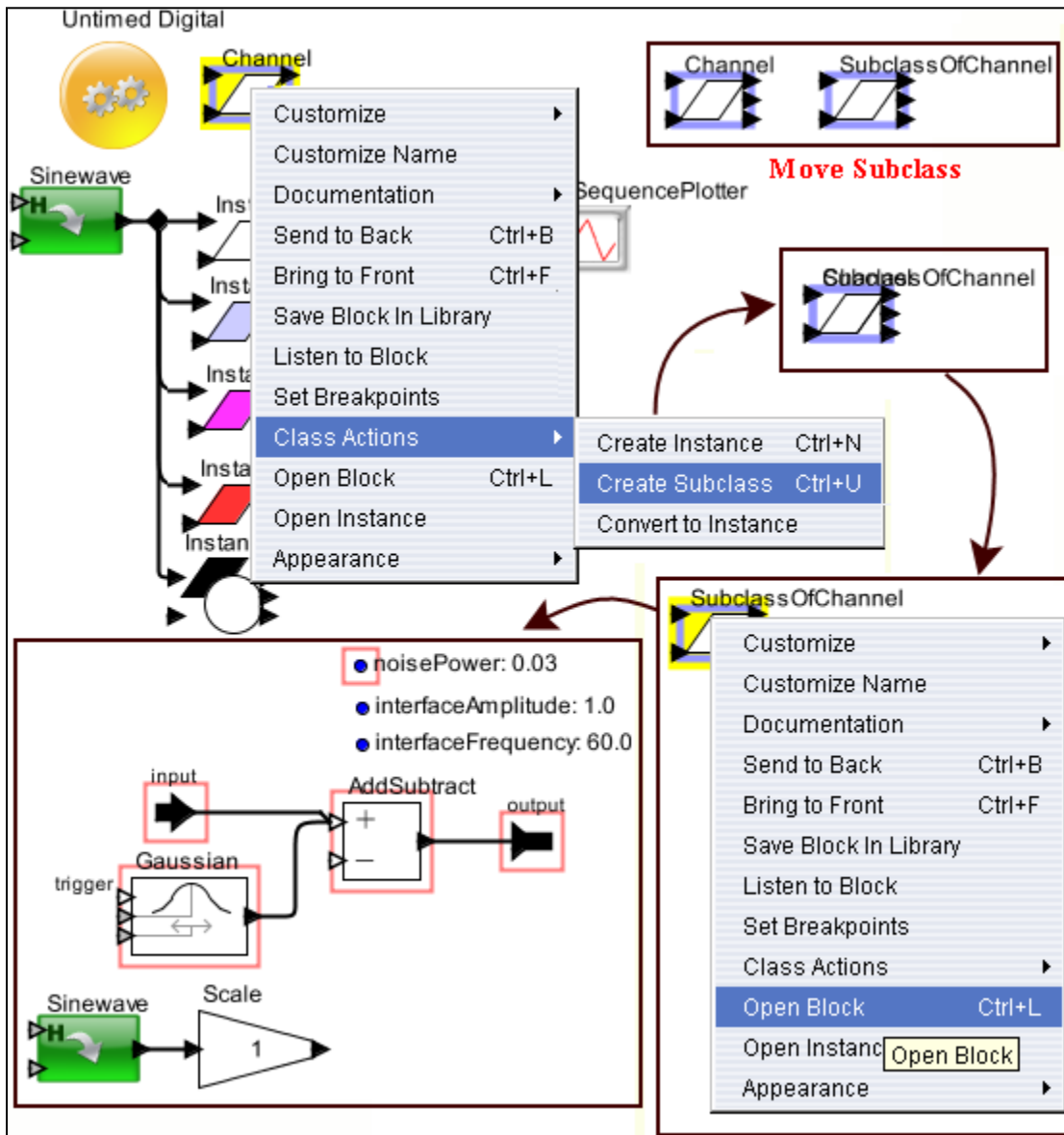


Figure 40. The model with a subclass of the channel with no overrides

A subclass is created by right clicking the class icon and selecting "**Class Actions > Create Subclass.**" The resulting icon for the subclass appears right on top of the icon for the class, so it needs to be moved over, as shown in the figure.

Looking inside the subclass reveals that it contains all the elements of the class, but with their icons now surrounded by a dashed pink outline. These elements are inherited. They cannot be removed from the subclass (try to do so, and you get an error message). You can,

however, change their parameter values and add additional elements. Consider the design shown in below figure.

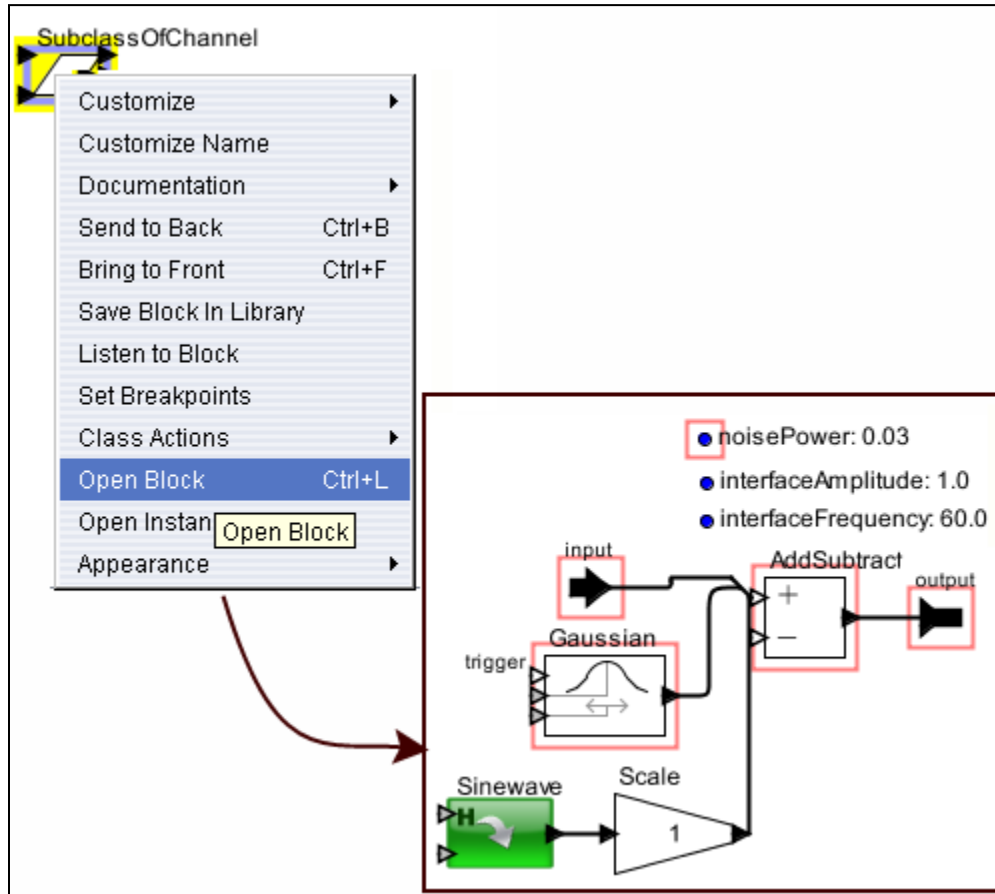


Figure 41. The subclass with overrides that add sinusoidal interferences

The above figure adds an additional pair of parameters named "interferenceAmplitude" and "interferenceFrequency" and an additional pair of actors implementing the interference. A model that replaces the last channel with an instance of the subclass is shown in the below figure.

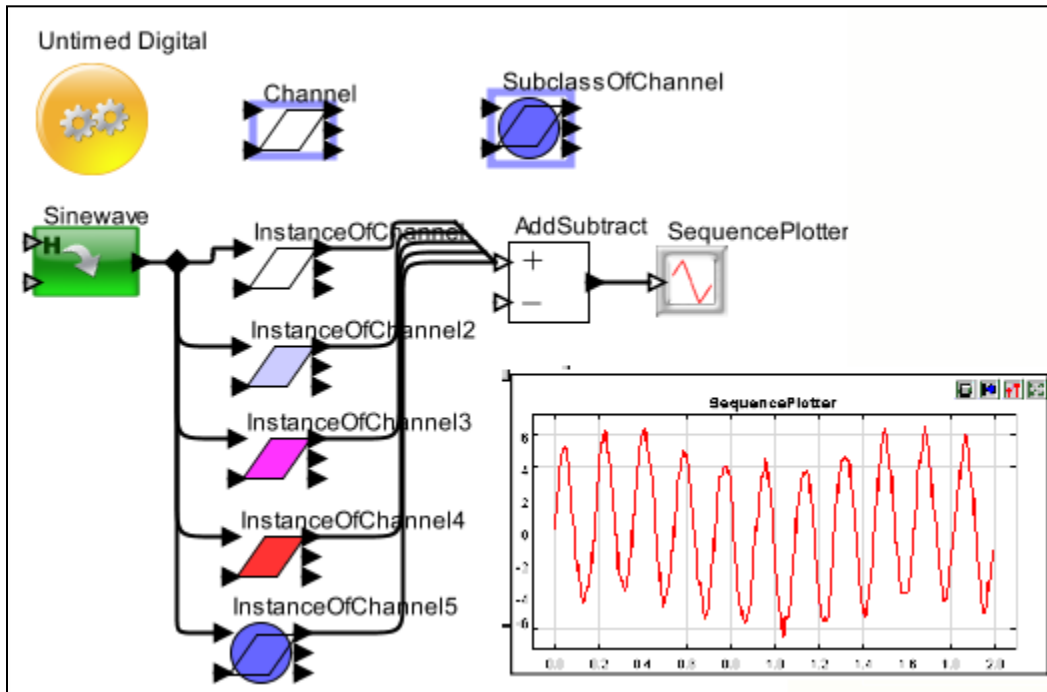


Figure 42. A model using the subclass form and a plot of the execution

The above model is along with a plot where you can see the sinusoidal interference.

An instance of a class may be created anywhere in a hierarchical model that is either in the same composite as the class or in a composite contained by that composite. To put an instance into a submodel, simply copy (or cut) an instance from the composite where the class is, and then paste that instance into the composite.

8.2.3 Sub-Models

Sub-models are an extension to the above class concept. This is a mechanism to provide a reuse and sharing of modeling components developed by team members. These are classes that are usually well understood and standard elements that require changes to parameter values only.

Classes are maintained within the model where they are used. Sub-models are stand-alone XML files that contain the model definition and a list of parameters. The procedure is still the same. The list of these sub-models can be maintained on an html page with links that can be

opened from within VisualSim. Similar to Classes, multiple instances of the same class can exist in a model and each of these instances can have different values for the parameters and icons.

9 Classes and Libraries

Before constructing classes, there are certain procedures to follow. If constructing a class using Java or C++, visit the respective documentation for details. For all blocks, there are some basic rules:

- Edit the VS_Model_Library variable in the VisualSim.bat (.sh) file. This is located in the VS_AR directory. The location of this directory becomes the baseline for all your libraries and custom blocks. The blocks are referenced relative to this base directory.
- If you have C/C+/SystemC blocks, you should also configure the VS_C_Library variable. This is the baseline for all the C++ files and the associated compiled code.
- If you have Java or custom XML class blocks, make sure the base path is included in the CLASSPATH of VisualSim.bat (.sh). All Java and XML classes are accessed relative to this CLASSPATH directory.

9.1 Create Class- Sequence of operations

1. Assemble the initial block diagram

Use the library blocks to assemble the model.

Create a Hierarchical block of this block diagram.

2. Create a class

Convert the Hierarchical block into a Class.

Save as a sub-model.

3. Instantiate a new class for use in a model

To use the Class, you need to instantiate the block in the model using Graph> Instantiate.

Entity. Make sure the Class is located within the VS_Model_Library directory.

4. To test the class

Test the class by constructing a simple model around it.

5. Save in Library. Right-click the block and select Save Block in Library.

9.2 Create Library and Instantiate in User_Library

1. Create a Library

Right-click the User_Library in the Folder and select 'Open for Editing'.

Using Graph > InstantiateEntity and entering VisualSim.moml.EntityLibrary, create a new folder.

Note: Make sure the Library name does not end in a numeral.

Convert to Class

Save as sub-model

Do a File > Open and select this file for editing.

Add the blocks that are part of this library.

Note: Make sure there is a Digital Simulator in this library folder. This is needed or you receive an error each time you open VisualSim.

2. Import Library into the User_library

Right-click the User_Library and select 'Open for Editing'.

Using Graph > InstantiateEntity and select the library created above.

Save.

3. View the Library

Restart VisualSim

The new library is visible in the User_Library.

Rules:

1. Make sure that the library blocks and the library file are located in the same directory. This becomes easy to ship to others.
2. When shipping the library, make sure to zip the file relative to the VS_Model_Library directory. Similarly, when the file is extracted, make sure to extract at the VS_Model_Library level.

A tutorial on creating the Class is provided.

9.3 Example of Creating a New Class Block

Open the above saved Class and assemble the following sequence.

- Open a New Block Diagram Editor

- Instantiate a Digital Simulation and a new Parameter (SimTime).
- Add blocks – Source >Traffic > Traffic, Defining_Flow > Processing and an output port into the model.
- Edit the Parameters of the Processing block as shown.
- Select all the items in the block diagram and select Debug->Create Hierarchy.
- A new Hierarchical block appears with a port.
- Remove the wire between the block and the port.
- Select the Hierarchical and Right-click to 'Convert to Class'.
- Open the Hierarchical 'class' and do a File->Save As.
- Select the directory under VS_Model_Library folder to save the file. Make sure to click "Save as sub-model". Name the file Traffic_Gen.xml.

Notes:

The "Open Block" shows the original version; whose content should not be modified by the user after it has been qualified. When you do an "Open Instance" for a Hierarchical block in a model, you are opening an instance of the block in the model. You have a local instance where you can add additional parameter or blocks to the model. You cannot modify the original block content. Any changes to the original Class is propagated to all models that use the block.

Notes:

- When you have global variables, Smart_Controllers and Schedulers, it is essential to have their names tied to the Block_Name such that they stay unique in the model. Otherwise the user gets an error when multiple instances are assembled.
- When you have a Script block such as a **Script** or **Smart Controller**, do not modify the Expression Script inside the Instance. This detaches the code from the original. Thus, any changes to the original are not reflected here.
- When creating a new variation of a class; do not open a model containing this block and try to save it as a new class + sub-model. This creates a class of an instance of a class and makes the solution very messy. Use the sub-class approach for doing this.

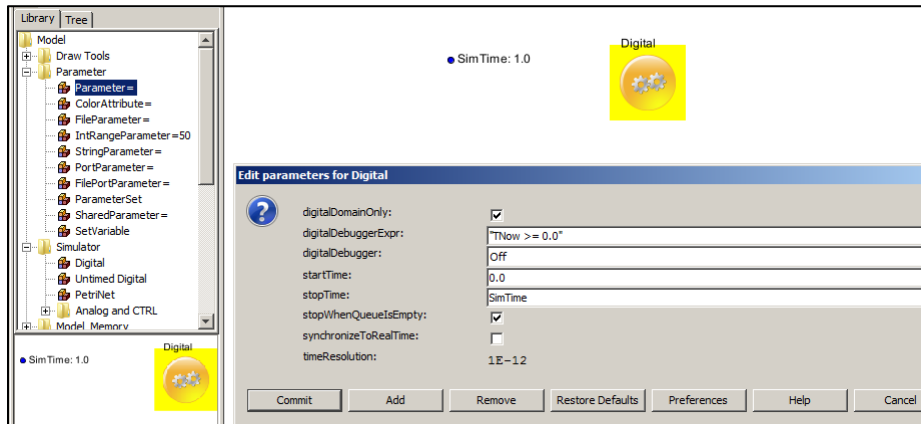


Figure 43. Create a Block Diagram

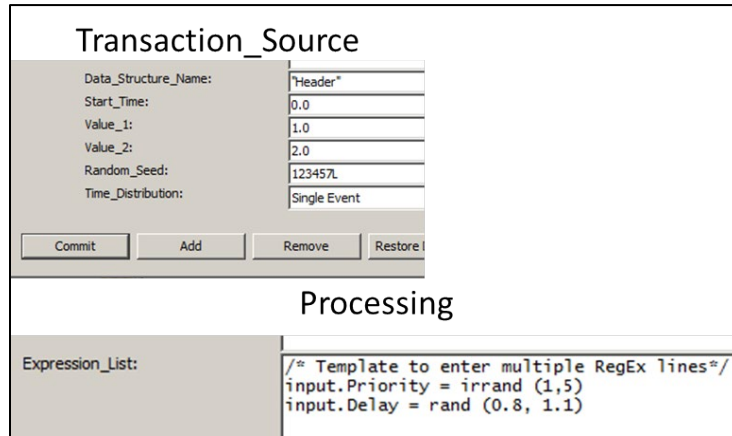


Figure 44. Block Attributes

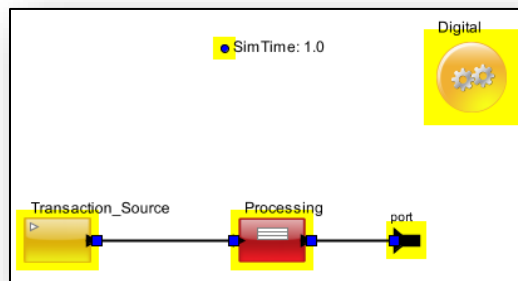


Figure 45. Making the Connection and Select+All

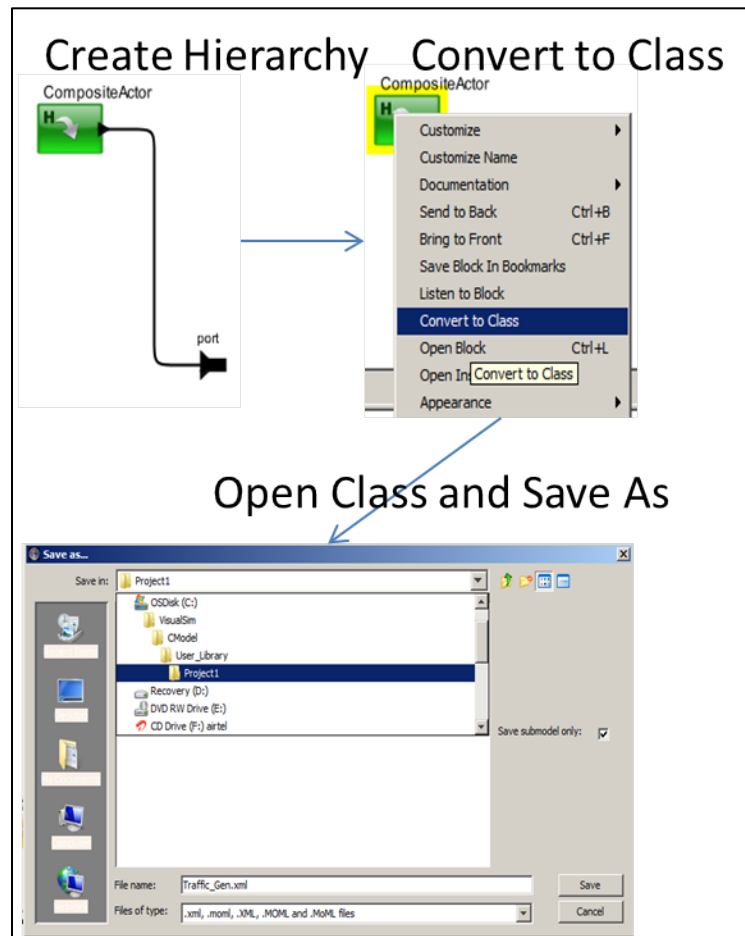


Figure 46. Create a Class

9.4 Annotating the Class

There are two things to make the Class block interesting. The first is the tooltip and the second is the block icon. The tooltip is done by adding a parameter with name `_explanation`, value string without "" and class `VisualSim.kernel.util.StringAttribute`. The icon can be updated by a right-click on the white space and selecting `Edit Custom Icon`. Make sure to Save the model after this.

9.5 Instantiating the Class in Model

A block that has been compiled to a `.class` (Java code version) file or a hierarchical block that is contained in a `.xml` file may be instantiated from ModelBuilder via `Graph > Instantiate Entity` and used in the model.

To instantiate an entity, follow these steps

1. Start up VisualSim and do File > New > Block Diagram Editor.
2. In the Block Diagram Editor, select Graph > Instantiate Class. Select the class file by traversing through the directory folders. The class must be in a Hierarchy within a Classpath location. It is best to place it within the VS_Model_Lib variable.
3. Click OK.
4. The new block is displayed in the BDE.

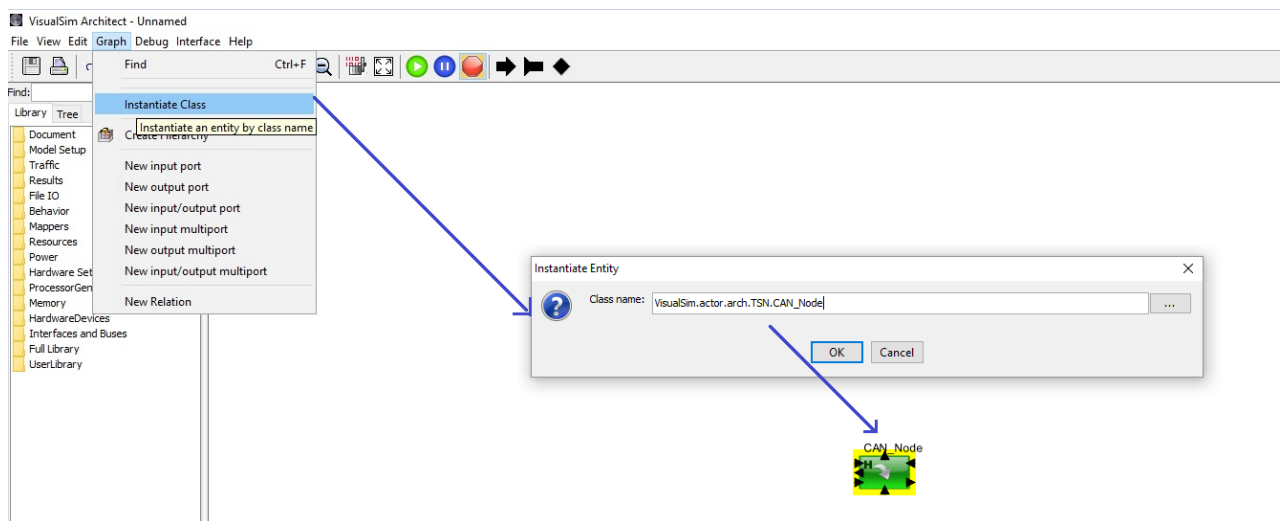


Figure 47. Instantiate Class to import a Class

9.6 Test the New Class Block:

1. After instantiating the Traffic block, drag the Digital Simulator, parameter, Server, and a TextDisplay to the BDE.
2. Set the parameter to SimTime and assign a value of 10.0.
3. Link the SimTime parameter to the EndTime of the Digital Simulator and the SimTime of the Traffic block.
4. Set the parameters of the Server.
5. Connect all the blocks as shown in the figure.

6. Select GO toolbar button to start the simulation.
7. You should see the Header Data Structure in the display.

10 Library Management

10.1 Introduction

Library management is an important enabler of IP reuse and sharing across the corporation. Library management is the organization of the key modeling components and system that are assembled with these systems. The library management system contains the following parts:

- Version control
- Library storage and Directory structure
- Accessing from the Graphical Editor

10.2 Version Control

The version control typically is the corporate storage environment. The solution utilizes a server and client solution. Typical VisualSim components and models are worked on by a single user. So, the version control, as in maintaining revisions, is not very critical. Users can manually maintain various versions in the environment.

10.3 Library Storage

The establishment of a centralized library management structure for a company is important and essential. Mirabilis Design prescribes a standard approach. The central library is accessible by all and can be stored in a version control system. There is a base directory which is <VisualSim_Top>. Within this top directory, there are two sub-structures - components and models.

- Components contain the basic components such as network node, traffic, processor, bus, and statistics creator. The Components can have sub-directories within them for different types of devices.
- Model contains platforms, boards, sub-systems, systems and networked systems. These can be organized within the model folder based on projects.

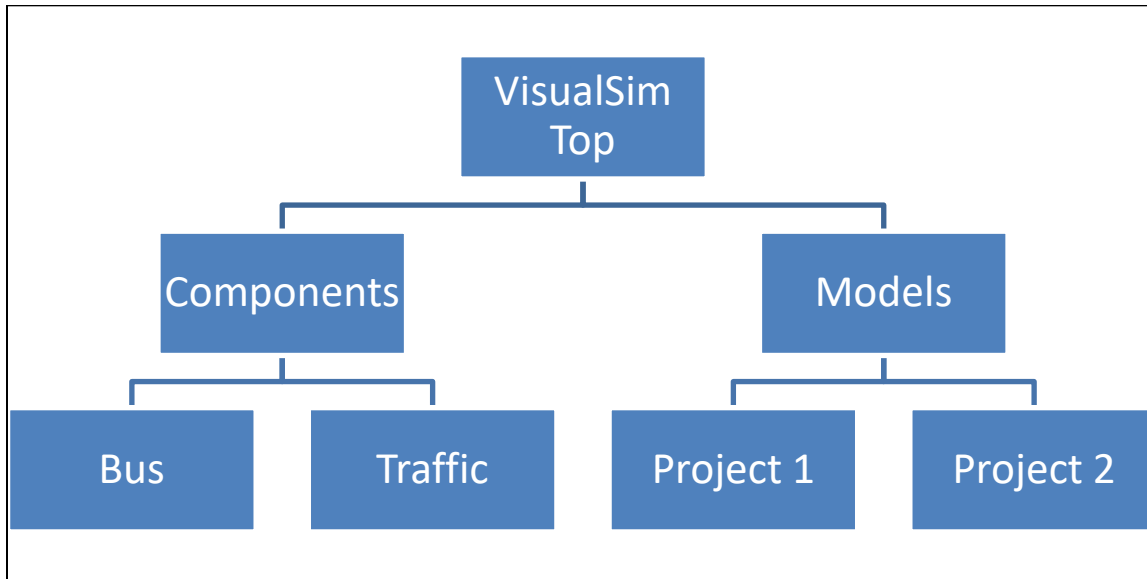


Figure 48. VisualSim Recommended Directory Structure

It is best to create a local copy of this directory for use within VisualSim. This ensures that connectivity losses do not stall creation. The top directory and the names of the directory organization with this top is identical between the central and local structure. Users can depend on version control tools to check in and check out the latest revisions of the files.

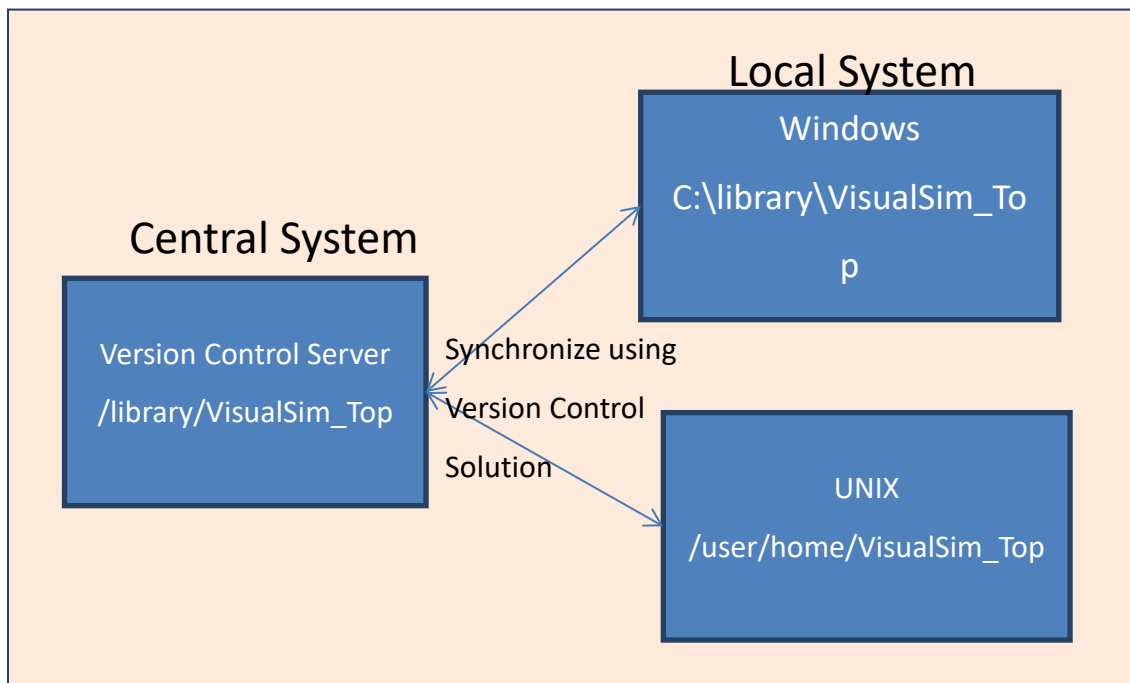


Figure 49. Library Integration between Central and Local System

10.4 User Library

Each user has a User Library, stored in `$HOME/.VisualSim/UserLibrary.xml`.

In the Block Diagram Editor, the User_Library is visible at the bottom of the actor palette on the left. After a class has been instantiated, to add it to the User Library, right click the block, and select "Save block in Library".

11 XML Details and File Parsing

11.1 Introduction

ModelBuilder stores models in ASCII files using an XML schema called Modeling Markup Language (MoML). MoML is the primary persistent file format for VisualSim models. It is also the primary mechanism for constructing models whose definition and execution is distributed over the network. This provides users the ability to directly edit and construct a MoML file. MoML is a modeling markup schema in the Extensible Markup Language (XML). It is intended for specifying interconnections of parameterized components. The filename extension can be “.xml” or “.moml” for MoML files. And the same XML file can be used in an applet2.

To get a quick start, try entering the following into a file called `test.xml`.

```
<?xml version="1.0" standalone="no"?>
<!DOCTYPE entity PUBLIC "-//Mirabilis Design//DTD MoML 1//EN"
"http://www.mirabilisdesign.com/xml/dtd/MoML_1.dtd">
<entity name="test" class="VisualSim.actor.TypedCompositeActor">
  <property name="Untimed_Digital"
    class="VisualSim.simulators.sdf.kernel.SDFDirector"/>
  <entity name="ramp" class="VisualSim.actor.lib.Ramp"/>
  <entity name="plot"
class="VisualSim.actor.lib.gui.SequencePlotter"/>
<relation name="r" class="VisualSim.actor.TypedIORelation"/>
<link port="ramp.output" relation="r"/>
<link port="plot.input" relation="r"/>
</entity>
```

This code defines a model in a top-level entity called “test”. By convention, we use the same name for the top-level model and the file in which it resides. The top-level model is an instance of the VisualSim class `VisualSim.actor.TypedCompositeActor`. It contains a simulator, two entities, a relation, and two links. The model is depicted in Figure 50. When you execute the

simulation, you get a window similar to the one in Figure 51. Enter “10” in the iterations box and click “Go” to execute the model for 10 iterations.

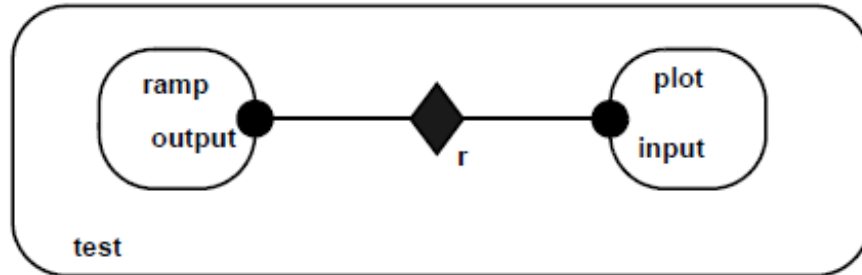


Figure 50. Simple example

The structure of the above MoML text is explained in detail in this chapter. A more interesting example is given in the \$VS/doc/Training_Material/How_to_Tasks/XML. You may wish to refer to that example as you read about the details.

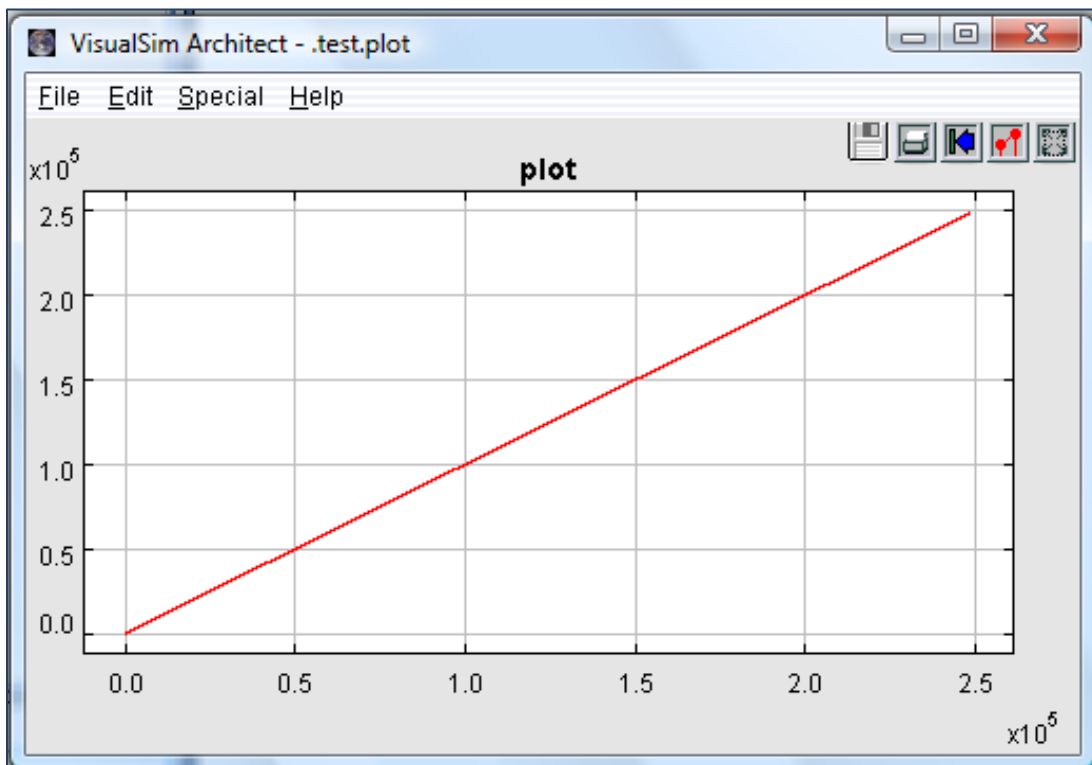


Figure 51. Simple example of a VisualSim model execution control window

MoML defines no semantics for an interconnection of components. It represents only the hierarchical containment relationships between entities with properties, their ports, and the connections between their ports. In VisualSim, the meaning of a connection (the semantics of the model) is defined by the simulator for the model, which is a property of the top-level entity. The simulator defines the semantics of the interconnection. MoML knows nothing about simulators except that they are instances of classes that can be loaded by the class loader and assigned as properties.

11.2 Topology

A model is given as a *topology*. A topology is a collection of *entities* and *relations*. Entities have *ports* and relations connect the ports. We use the term *connection* to denote the association between connected ports (or their entities), and the term *link* to denote the association between ports and relations or between relations and relations. Thus, a connection consists of one or more relations and two or more links. The visual notation is shown in Figure 52, where entities are depicted as rounded boxes, relations as diamonds, and entities as filled circles.

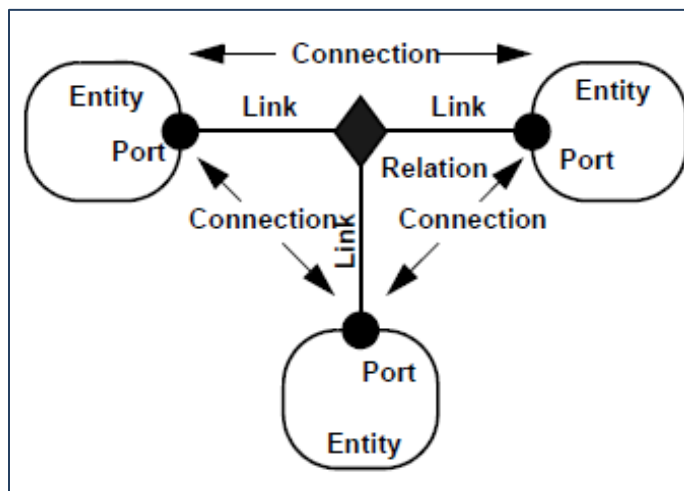


Figure 52. Visual notation and terminology

11.3 Relation Groups

Relations mediate connections between ports. For flexibility, particularly with visual syntaxes, the VisualSim abstract syntax permits any number of relations to be involved in any one connection.

Figure 53 illustrates this. Relations may be linked to other relations. Any two relations that are linked are said to be members of the same *relation group*. Specifically, a relation group is a maximal set of linked relations. Semantically, a relation group has the same meaning as a single relation. Thus, the two diagrams in Figure 53 have the same meaning.

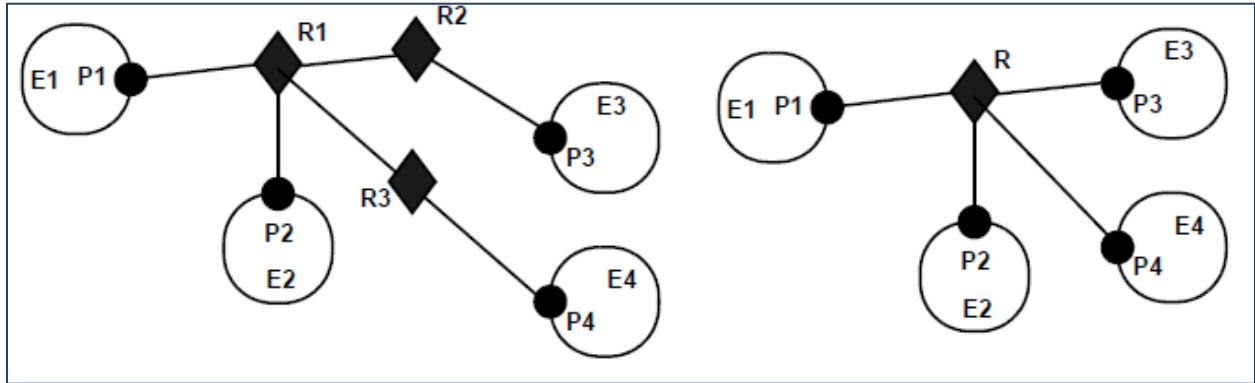


Figure 53. Relationship Groups

Relation Group A relation group is a maximal set of linked relations. At the left, R1, R2, and R3 form a relation group. A relation group is a semantically identical to a single relation, so the two diagrams above have the same meaning.

11.4 Specification of a Model

In this section, we describe the XML elements that are used to define MoML models.

11.4.1 Data Organization

As with all XML files, MoML files have two parts - one defining the MoML language and one containing the model data. The first part is called the *document type definition*, or DTD. This dual specification of content and structure is a key XML innovation. The DTD for MoML is available in VisualSim at \$VS/VisualSim/moml/MoML_DTD_1. If you are adept at reading these, it is a complete specification of the schema. However, as it is not particularly easy to read, we explain its key features here.

Every MoML file must either contain or refer to a DTD. The simplest way to do this is with the following file structure:

```
<?xml version="1.0" standalone="no"?>
<!DOCTYPE entity PUBLIC "-//Mirabilis Design//DTD MoML 1//EN"
"http://www.mirabilisdesign.com/xml/dtd/MoML_1.dtd">
<entity name="modelname" class="classname">
  model definition ...
</entity>
```

Here, “*model definition*” is a set of XML elements that specify a clustered graph. The syntax for these elements is described in subsequent sections. The first line above is required in any XML file. It asserts the version of XML that this file is based on (1.0) and states that the file includes external references (in this case, to the DTD). The second and third lines declare the document type (model) and provide references to the DTD.

The references to the DTD above refer to a “public” DTD. The name of the DTD is

```
-//Mirabilis Design//DTD MoML 1//EN
```

which follows the standard naming convention of public DTDs. The leading dash “-” indicates that this is not a DTD approved by any standards body. The first field, surrounded by double slashes, is the name of the “owner” of the DTD, “*Mirabilis Design*”.

The next field is the name of the DTD, “*DTD MoML 1*” where “1” indicates version 1 of the MoML DTD. The final field, “*EN*” indicates that the language assumed by the DTD is English. The VisualSim MoML parser requires that the public DTD be given exactly as shown, or it does not recognize the file as MoML. If a particular MoML tool does not have access to a local copy of the DTD, then it finds it at this web site.

The “entity” element may be replaced by a “class” element, as in:

```
<?xml version="1.0" standalone="no"?>
<!DOCTYPE class PUBLIC "-//Mirabilis Design//DTD MoML 1//EN"
"http://www.mirabilisdesign.com/xml/dtd/MoML_1.dtd">
<class name="modelname" class="classname">
  class definition ...
</class>
```

We say more about class definitions below.

11.5 Overview of XML

An XML document consists of the header tags “<?xml ... ?>” and “<!DOCTYPE ... >” followed by exactly one *element*. The element has the structure:

```

start tag
body
end tag

```

where the start tag has the form

```
<elementName attributes>
```

and the end tag has the form

```
</elementName>
```

The body, if present, can contain additional elements as well as arbitrary text. If the body is not present, then the element is said to be *empty* and it can optionally be written using the shorthand:

```
<elementName attributes/>
```

where the body and end tag are omitted.

The attributes are given as follows:

```
<elementName attributeName="attributeValue" .../>
```

Which attributes are legal in an element is defined by the DTD. The quotation marks delimit the value of the attributes, so if the attribute value needs to contain quotation marks, then they must be given using the special XML entity “"” as in the following example:

```
<elementName attributeName="&quot;foo&quot;"/>
```

The value of the attribute is

```
"foo" (with the quotation marks).
```

In XML “"” is called an *entity*, creating possible confusion with our use of entity in VisualSim. In XML, an entity is a named storage unit of data. Thus, “"” references an entity called “quot” that stores a double quote character.

11.6 Names and Classes

Most MoML elements have *name* and *class* attributes. The name is a handle for the object being defined or referenced by the element. In MoML, the same syntax is used to reference a pre-existing object as to create a new object. If a new object is being created, then the class attribute

(usually) must be given. If a pre-existing object is being referenced, or if the MoML reader has a built-in default class for the element, then the class attribute is optional. If the class attribute is given, then the pre-existing object must be an instance of the specified class.

A name is either absolute or relative. Absolute names begin with a period "." and consist of a series of name fields separated by periods, as in ".x.y.z". Each name field can have alphanumeric characters, spaces, or the underscore "_" character. The first field is the name of the top-level model or class object. The second field is the name of an object immediately contained by that top-level. Any name that does not begin with a period is relative to the current context, the object defined or referenced by an enclosing element. The first field of such a name refers to or defines an object immediately contained by that object.

For example, inside of an object with absolute name ".x", the name "y.z" refers to an object with absolute name ".x.y.z". A name is required to be unique within its container. That is, in any given model, the absolute names of all the objects must be unique. There can be two objects named "z", but they must not be both contained by ".x.y". Not much more is said about classes. The class names that are used in the VisualSim implementation of MoML are always fully qualified Java class names. In addition, in VisualSim, a MoML file can be referenced as a class in the same way. In MoML, any named object can also have a distinct *display name*. The display name is used to present the object to the user in visualization and editing tools. It need not be unique and can consist of arbitrary text. It is specified by the *display* XML element, as in the following example.

```
<entity name="modelName" class="classname">
    <display name="arbitrary text here"/>
</entity>
```

11.7 Top-Level Entities

A very simple MoML file looks like this:

```
<?xml version="1.0" standalone="no"?> <!DOCTYPE entity PUBLIC
"--//Mirabilis Design//DTD MoML_1//EN"
"http://www.mirabilisdesign.com/xml/dtd/moml.dtd">

<entity name="modelName" class="classname"> </entity>
```

The *entity* element has name and class attributes, and defines a VisualSim model. This value of the class attribute must be a class that is instantiable by the MoML tool. For example, in VisualSim, we can define a model with:

```
<?xml version="1.0" standalone="no"?> <!DOCTYPE entity PUBLIC "-//Mirabilis Design//DTD MoML_1//EN"
"http://www.mirabilisdesign.com/xml/dtd/moml.dtd">

<entity name="VSmodel" class="VisualSim.actor.TypedCompositeActor">
</entity>
```

Here, `VisualSim.actor.TypedCompositeActor` is a class. Most useful models are instances of `VisualSim.kernel.CompositeEntity` or a derived class. `TypedCompositeActor`, as in the above example, is derived from `CompositeEntity`.

11.8 Entity Element

A model typically contains entities, as in the following VisualSim example:

```
<?xml version="1.0" standalone="no"?>

<!DOCTYPE entity PUBLIC "-//Mirabilis Design//DTD MoML_1//EN"
"http://www.mirabilisdesign.com/xml/dtd/moml.dtd">

<entity name="VSmodel" class="VisualSim.actor.TypedCompositeActor">
  <entity name="source" class="VisualSim.actor.lib.Ramp"/>
  <entity name="sink" class="VisualSim.actor.lib.SequencePlotter"/>
</entity>
```

Notice the common XML shorthand here of writing “`<entity ... />`” rather than “`<entity ...></entity>`.” Of course, the shorthand only works if there is nothing in the body of the entity element.

An entity can contain other entities, as shown in this example:

```
<entity name="VSmodel" class="VisualSim.actor.TypedCompositeActor">
  <entity name="container" class="VisualSim.actor.TypedCompositeActor">
    <entity name="source" class="VisualSim.actor.lib.Ramp"/>
  </entity>
```

```
</entity>
```

An entity must specify a class unless the entity already exists in the containing entity or model. The name of the entity reflects the container hierarchy. Thus, in the above example, the *source* entity has the full name “.VSmodel.container.source”. The definition of an entity can be distributed in the MoML file. After it is created, it can be referred to again by name as follows:

```
<entity name="top" class="classname">
  <entity name="x" class="classname"/> ...
  <entity name="x"><property name="y">
</entity></entity>
```

MoML files support multiple containment, as in the following example:

```
<entity name="top" class="classname">
  <entity name="x" class="classname"/>
  ...
  <entity name="y" class="classname">
    <entity name=".top.x"/>
  </entity>
</entity>
```

Here, the element named “x” appears both in “top” and in “.top.y”, i.e. the same instance appears in two different places. Thus, it would have two full names, “.top.x” and “.top.y.x”. However, VisualSim does not support this, as it implements a strict container relationship, where an object can have only one container. Thus, attempting to parse the above MoML results in an exception being thrown.

11.9 Properties

Entities (and some other elements) can be parameterized. There are two mechanisms. The simplest one is to use the *property* element:

```
<entity name="source" class="VisualSim.actor.lib.Ramp">
  <property name="init" value="5" class="VisualSim.data.expr.Parameter"/>
</entity>
```

The property element has a name, at minimum (the value and class are optional). It is common for the enclosing class to already contain properties, in which case the property element is used only to set the value. For example:

```
<entity name="source" class="VisualSim.actor.lib.Ramp">
  <property name="init" value="5"/>
</entity>
```

In the above, the enclosing object (*source*, an instance of `VisualSim.actor.lib.Ramp`) must already contain a property with the name *init*. This is typically how library components are parameterized. In VisualSim, the value of a property may be an expression, as in “`PI/50`”. The expression may refer to other properties of the containing entity or of its container. Note that the expression language is not part of MoML, but is rather part of VisualSim. In MoML, a property value is simply an uninterpreted string. It is up to a MoML tool, such as VisualSim, to interpret that string.

A property can be declared without a class and without a pre-existing property if it is a *pure property*, one with only a name and no value. For example:

```
<entity name="source" class="VisualSim.actor.lib.Ramp">
  <property name="abc"/></entity>
```

A property can also contain a property, as in

```
<property name="x" value="5"> <property
  name="y" value="10"/></property>
```

A second, much more flexible mechanism is provided for parameterizing entities. The *configure* element can be used to specify a relative or absolute URL pointing to a file that configures the entity, or it can be used to include the configuration information in line. That information need not be MoML information. It need not even be XML, and can even be binary encoded data (although binary data cannot be in line; it must be in an external file). For example,

```
<entity name="sink" class="VisualSim.actor.lib.SequencePlotter">
  <configure source="url"/></entity>
```

Here, *url* can give the name of a file containing data, or a URL for a remote file. (For the SequencePlotter actor, that external data has PlotML syntax. (PlotML is another XML schema for configuring plotters.). Configure information can also be given in the body of the MoML file as follows:

```
<entity name="sink" class="VisualSim.actor.lib.SequencePlotter">
  <configure>configure information </configure></entity>
```

With the above syntax, the configure information must be textual data. It can contain XML markup with only one restriction: if the tag “`</configure>`” appears in the textual data, then it must be

preceded by a matching “ <configure>”. That is, any configure elements in the markup must have balanced start and end tags².

You can give both source attribute and in-line configuration information, as in the following:

```
<entity name="sink" class="VisualSim.actor.lib.SequencePlotter">
  <configure source="url">configure information </configure></entity>
```

In this case, the file data is passed to the application first, followed by the in-line configuration data.

In VisualSim, the configure element is supported by any class that implements the Configurable interface. That interface defines a configure() method that accepts an input stream. Both external file data and in-line data are provided to the class as a character stream by calling this method. There is a subtle limitation with using markup within the configure element. If any of the elements within the configure element match MoML elements, then the MoML DTD is applied to assign default values, if any, to their attributes. Thus, this mechanism works best if the markup within the configure element is not using an XML schema that happens to have element names that match those in MoML. Alternatively, if it does use MoML element names, then those elements are used with their MoML meaning. This limitation can be fixed using XML namespaces, something we will eventually implement.

7.3.7 Doc Element

Some elements can be documented using the *doc* element. For example,

```
<entity name="source" class="VisualSim.actor.lib.Ramp">
  <property name="init" value="5">
    <doc>Initialize the ramp above the default because...
  </doc>
  </property>
  <doc> This actor produces an increasing sequence beginning
  with 5. </doc>
</entity>
```

² XML allow markup to be included in arbitrary data as long as it appears within either a processing instruction or a CDATA body. However, for reasons that would only baffle anyone familiar with modern programming languages, processing instructions and CDATA bodies cannot be nested within one another. The MoML configure element can be nested, so it offers a much more flexible mechanism than the standard ones in XML.

formatting within the `doc` element: With the above syntax, the documentation information must be textual data. It can include markup, as in the following example, which uses XHTML³.

```
<entity name="source" class="VisualSim.actor.lib.Ramp">
<doc><H1>Using HTML</H1>Text with
<I>markup</I>.</doc></entity>
```

An alternative method is to use an XML processing instruction as follows:

```
<entity name="source" class="VisualSim.actor.lib.Ramp">
  <doc><?xhtml <H1>Using HTML</H1>Text with <I>markup</I>.<?>
  </doc>
</entity>
```

This requires that any utility that uses the documentation information be able to handle the `xhtml` processing instruction, but it makes it very clear that the contents are XHTML. However, for reasons we do not understand, XML does not allow processing instructions to be nested and so this technique has its limitations. More than one `doc` element can be included in an element. To do this, give each `doc` element a name, as follows:

```
<entity name="entityname" class="classname"> <doc
name="docname">doc contents </doc></entity>
```

The name must not conflict with any preexisting property. If a `doc` element or a property with the specified name exists, then it is removed and replaced with the property. If no name is given, then the `doc` element is assigned the name “`_doc`”.

A common convention, used in VisualSim, is to add `doc` elements with the name “`tooltip`” to define a tooltip for GUI views of the component. A tooltip is a small window with short documentation that pops up when the mouse lingers on the graphical component.

Note that the same limitation of using markup within `configure` elements also applies to `doc` elements.

7.3.8 Ports

An entity can declare a port:

```
<entity name="A" class="classname"> <port
name="out"/></entity>
```

In the above example, no class is given for the port. If a port with the specified name already exists in the class for entity `A`, then that port is the one referenced. Otherwise, a new port is created in VisualSim by calling the `newPort()` method of the container. Alternatively, we can specify a class name, as in

³ XHTML is HTML with additional constraints so that it conforms with XML syntax rules. In particular, every start tag must be matched by an end tag, something that ordinary HTML does not require (but fortunately, does allow).

```
<entity name="A" class="classname"> <port
name="out" class="classname"/></entity>
```

In this case, a port is created if one does not already exist. If it does already exist, then its class is checked for consistency with the declared class (the pre-existing port must be an instance of the declared class). In VisualSim, the typical classname for a port is

```
VisualSim.actor.TypedIOPort
```

In VisualSim, the container of a port is required to be an instance of VisualSim.kernel.Entity or a derived class.

It is often useful to declare a port to be an input, an output, or both. To do this, enclose in the port a property named "input" or "output" or both, as in the following example:

```
<port name="out" class="VisualSim.actor.IOPort">
<property name="output"/></port>
```

This is an example of a pure property. Optionally, the property can be given a boolean value, as in

```
<port name="out" class="VisualSim.actor.IOPort">
<property name="output" value="true"/></port>
```

The value can be either "true" or "false", where the latter defines the port to not be an output. A port can be defined to be both an input and an output, as follows

```
<port name="out" class="VisualSim.actor.IOPort">
<property name="output" value="true"/> <property
name="input" value="true"/></port>
```

It is also sometimes necessary to declare that a port is a multiport. To do this, enclose in the port a property named "multiport" as in the following example:

```
<port name="out" class="VisualSim.actor.IOPort">
<property name="multiport"/></port>
```

The enclosing port must be an instance of IOPort (or a derived class such as TypedIOPort), or else the property is treated as an ordinary property. As with the input and output attribute, the multiport property can be given a boolean value, as in

```
<port name="out" class="VisualSim.actor.IOPort">
<property name="multiport" value="true"/></port>
```

If a port is an instance of TypedIOPort (for library actors, most are), then you can set the type of the port in MoML as follows:

```
<port name="out" class="VisualSim.actor.IOPort">
```

```

<property name="type" value="double"
          class="VisualSim.actor.TypeAttribute"/>
</port>

```

This is occasionally useful when you need to constrain the types beyond what the built-in type system takes care of. The names of the built-in types are (currently) boolean, booleanMatrix, complex, complexMatrix, double, doubleMatrix, fix, fixMatrix, int, intMatrix, long, longMatrix, unsignedByte, unsignedByteMatrix, object, string, and general. These are defined in the class `VisualSim.data.type.BaseType`.

7.3.9 Relations and Links

To connect entities, you create relations and links. The following example describes the topology shown in Figure 54:

```

<entity name="top" class="classname">
<entity name="A" class="classname">
  <port name="out"/>
</entity>
<entity name="B" class="classname">
  <port name="out"/>
</entity>
<entity name="C" class="classname">
  <port name="in">
    <property name="multiport"/>
  </port> </entity>
<relation name="r1" class="classname"/>
<relation name="r2" class="classname"/>

<link port="A.out" relation="r1"/>
<link port="B.out" relation="r2"/>
<link port="C.in" relation="r1"/>
<link port="C.in" relation="r2"/>
</entity>

```

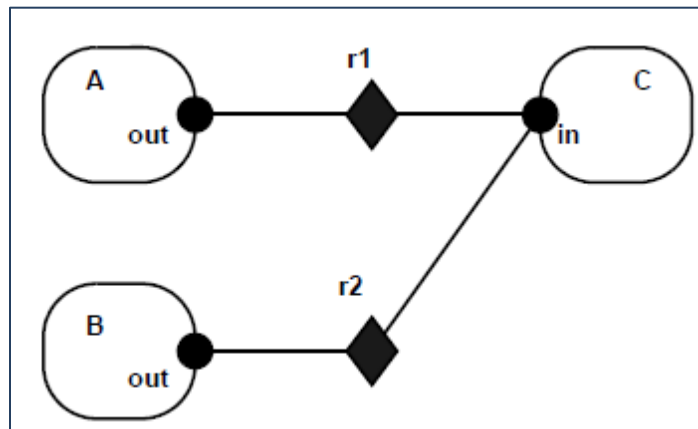


Figure 54. Example topology.

In VisualSim, the typical classname for a relation would be `VisualSim.actor.TypedIORelation`. The classname may be omitted, in which case the `newRelation()` method of the container is used to create a new relation. The container is required to be an instance of `VisualSim.kernel.CompositeEntity`, or a derived class. As usual, the class attribute may be omitted if the relation already exists in the containing entity.

The `link` elements may appear anywhere in the body of an `entity` or `class` element. They will be processed after all the contained entities, properties, and relations are created. However, the order of the link elements relative to each other does matter. Notice in this example that there are two distinct links to `C.in` from two different relations. The order of these links may be important to a MoML tool, so any MoML tool must preserve the order in which they are specified, as VisualSim does. We say that C has two links, indexed 0 and 1.

The `link` element can explicitly give the index number at which to insert the link. For example, we could have achieved the same effect above by saying

```
<link port="C.in" relation="r1" insertAt="0"/>
<link port="C.in" relation="r2" insertAt="1"/>
```

Whenever the `insertAt` option is not specified, the link is always appended to the end of the list of links.

When the `insertAt` option is specified, the link is inserted at that position, so any pre-existing links with larger indices will have their index numbers incremented. For example, if we do

```
<link port="C.in" relation="r1" insertAt="0"/>
<link port="C.in" relation="r2" insertAt="2"/>
<link port="C.in" relation="r3" insertAt="1"/>
```

then there will be a link to `r1` with index 0, a link to `r2` with index 2 (note! not 1), and a link to `r3` with index 1.

If the specified index is beyond the existing number of links, then null links (that is links to nothing) are created to fill in. So for example, if the first link we create is given by

```
<link port="C.in" relation="r2" insertAt="1"/>
```

then the port has *two* links, not one, but the first one is an empty link. If we then say

```
<link port="C.in" relation="r2"/>
```

then the port has *three* links, with the first one being empty. If we then say

```
<link port="C.in" relation="r2" insertAt="0"/>
```

then there are *four* links, with the *second* one being empty. Normally, it is not necessary in MoML to specify whether a link occurs on the inside of a port or on the outside. This can be determined automatically by identifying the relation. For example, in figure 54, port P4 is linked on the inside to relation R2 and on the outside to relations R3 and R4.

However, close examination of the DTD reveals that the relation attribute is optional. If the relation attribute is not present, then a null link is inserted. However, if you do not specify a relation, then there is no way to determine whether an inside null link or an outside null link was intended.

MoML defines the default to be an outside null link. To specify an inside null link, use the `insertInsideAt` attribute. For example, to insert a null link on the inside of P4 in Figure 54 prior to the link to R2, use:

```
<entity name="E0.E1">
  <link port="P4.in" insertInsideAt="0"/>
</entity>
```

Note that the index number is not the same thing as the channel number in VisualSim. In VisualSim, a relation may have a width greater than one, so a single link may represent more than one channel (actually, it could even represent zero channels if that relation is not linked to another ports).

There is no significance to the order in which relations are linked, unlike the order in which ports are linked to relations. Unlike links between relations and ports, there is no significance to multiple links between the same relations. Thus, in the following MoML, the second line is redundant and can be omitted with no change in meaning:

```
<link relation1="R1" relation2="R2"/> <link
relation1="R1" relation2="R2"/>
```

The same is not true of links between relations and ports. A relation group is a maximal set of linked relations. If a port links to multiple relations within the same relation group, then the meaning is exactly the same as if the port were linked to just one relation in the group. The order in which a link between ports and relations in a group is made matters, but the order in which links between relations are made does not. Thus, a relation group is semantically equivalent to a single relation where the links between ports and the single relation are made in the same order as the links between a port and relations in a relation group.

11.10 Classes

So far, entities have been instances of externally defined classes accessed via a class loader. They can also be instances of classes defined in MoML. To define a class in MoML, use the *class* element, as in the following example:

```
<?xml version="1.0" standalone="no"?> <!DOCTYPE class PUBLIC "-//
//Mirabilis Design//DTD MoML
1//EN" "http://Www.mirabilisdesign.com/xml/dtd/moml.dtd"> <class
name="Gen" extends="VisualSim.actor.TypedCompositeActor">
<entity name="ramp" class="VisualSim.actor.lib.Ramp"> <port
name="output"/> <property name="step" value="2*PI/50"/></entity>
<entity name="sine" class="VisualSim.actor.lib.TrigFunction"><port
name="input"/> <port name="output"/></entity> <port name="output"
class="VisualSim.actor.TypedIOPort"/> <relation name="r1"
class="VisualSim.actor.TypedIORelation"/> <relation name="r2"
class="VisualSim.actor.TypedIORelation"/> <link port="ramp.output"
relation="r1"/> <link port="sine.input" relation="r1"/> <link
port="sine.output" relation="r2"/> <link port="output"
relation="r2"/></class>
```

The class element may be the top-level element in a file, in which case the DOCTYPE should be declared as “class” as done above. It can also be nested within a model. The above example specifies the topology shown in figure 55. After it is defined, it can be instantiated as if it were a class loaded by the class loader:

```
<entity name="instancename" class="classname"/>
```

or

```
<entity name="instancename" class="classname" source="url"/>
```

The first form can be used if the class definition can be found from the classname. There are two ways that this could happen. First, the classname might match a class definition that is in scope; a class definition is in scope if the class is defined within the same container where the entity is being created, or within the container of that container, or the container of that container, and so on.

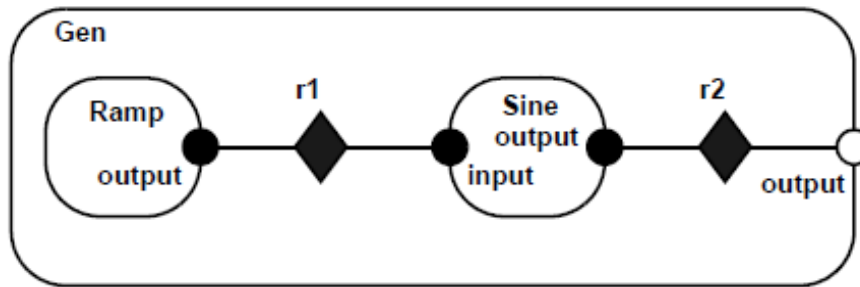


Figure 55. Sine wave generator topology.

That is once a class is defined, it can be instantiated anywhere (deeply) within the container in which is defined. Second, the *classname* might be sufficient to find the class definition in a file, much the way Java classes are found. For example, if the classname is `VisualSim.actor.lib.Sinewave` and the class is defined in the file `$PTII/VisualSim/actor/lib/Sinewave.xml`, then there is no need to use the second form to specify the URL where the class is defined. Specifically, the CLASSPATH is searched for a file matching the classname. By convention, the file defining the class has the same name as the class, with the extension “.xml” or “.moml”. An example of the first of these techniques is given below:

```

<?xml version="1.0" standalone="no"?> <!DOCTYPE entity PUBLIC "-//
//Mirabilis Design//DTD MoML
1//EN" "http://www.mirabilisdesign.com/xml/dtd/moml.dtd"> <entity
name="top" class="VisualSim.actor.TypedCompositeActor"><class
name="Gen" extends="VisualSim.actor.TypedCompositeActor"> class
definition ...
</class> <entity name="inside"
class="VisualSim.actor.TypedCompositeActor"><entity name="instance"
class="Gen"/> </entity></entity>
  
```

The ability to give a URL as the source of a class definition is very powerful. It means that a model may be build from component libraries that are defined worldwide. There is no need to localize these. Of course, referencing a URL means the usual risks that the link becomes invalid. It is our hope that reliable and trusted sources of components emerge and not allow this to happen.

The Gen class given at the beginning of this subsection generates a sine wave with a period of 50 samples. It is not all that useful without being parameterized. Let us extend it and add properties:

```

<class name="Sinegen" extends="Gen">
  <property name="samplingFrequency" value="8000.0"
  
```

```

class="VisualSim.data.expr.Parameter">
    <doc>The sampling frequency in Hertz.</doc>
</property>
<property name="frequency" value="440.0"
class="VisualSim.data.expr.Parameter">
    <doc>The frequency in Hertz.</doc>
</property>
<property name="ramp.step" value="frequency*2*PI/samplingFrequency">
    <doc>Formula for the step size.</doc>
</property>
<property name="ramp.init" value="phase"> </property>
</class>

```

This class extends Gen by adding two properties, and then sets the properties of the component entities to have values that are expressions.

11.11 Inheritance

MoML supports inheritance by permitting the user to extend existing classes. For example, consider the following MoML file:

```

<?xml version="1.0" standalone="no"?>
<!DOCTYPE entity PUBLIC "-//Mirabilis Design//DTD MoML
1//EN""http://www.mirabilisdesign.com/xml/dtd/moml.dtd">
<entity name="top" class="VisualSim.kernel.CompositeEntity">
    <class name="base" extends="VisualSim.kernel.CompositeEntity">
        <entity name="e1" class="VisualSim.kernel.ComponentEntity">
            </entity>
        </class>
    <class name="derived" extends="base">
        <entity name="e2" class="VisualSim.kernel.ComponentEntity"/>
    </class>
    <entity name="instance" class = ".top.derived"/>
</entity>

```

Here, the “derived” class extends the “base” class by adding another entity to it, and “instance” is an instance of derived class. The class “derived” can also give a source attribute, which gives a URL for the source definition.

A derived class (or subclass) can contain additional entities, relations, ports, and links. However, it cannot remove entities, relations, ports or links defined in the base class. Moreover, it cannot add links that are exclusively between ports and relations defined in the base class. New links must involve either a port or a relation that is new in the derived class.

11.12 Simulators

VisualSim requires the specification of a Simulator associated with a model, an entity, or a class. The Simulator is a property of the model. The following example gives Digital semantics to a VisualSim model:

```
<entity name="top" class="VisualSim.actor.TypedCompositeActor">
  <property name="Simulator"
    class="VisualSim.simulators.de.kernel.DEDirector">
    <property name="stopTime" value="100.0"/>
  </property>
  ...
</entity>
```

This example also sets a property of the Simulator. The name of the Simulator is not important, except that it cannot collide with the name of any other property in the model.

11.13 Input Element

It is possible to insert MoML from another file or URL into a particular point in your model. For example:

```
<entity name="top" class="...">
  <entity name="a" class="...">
    <input source="url"/>
  </entity>
</entity>
```

This takes the contents of the URL specified in the source attribute of the input element and places them inside the entity named “a”. The base of the current document (the one containing the import statement) is used to interpret a relative URL, or if the current document has no base, then the current working Simulator is used, or if that fails, the current CLASSPATH.

11.14 Annotations for Visual Rendering

The abstract syntax of MoML, clustered graphs, is amenable to visual renditions as bubble and arc diagrams or as block diagrams. To support tools that display and/or edit MoML files visually, MoML allows a relation to optionally have a *vertex* which gives it a specific physical location in a visual syntax. For example:

```
<relation name="r" class="VisualSim.actor.TypedIORelation">
  <vertex name="v1" class="classname" value="location"/>
</relation>
```

A visual rendition (such as that created by ModelBuilder) would render the relation with a located icon, rather than simply as a wire between ports. Figure 56 illustrates two links, the top one of which has a vertex, and the bottom one of which does not. The two are semantically identical, but obviously the rendition is different. A vertex is given as follows:

```
<vertex name="v1" class="VisualSim.moml.Vertex" value="{184.0, 93.0}"/>
```

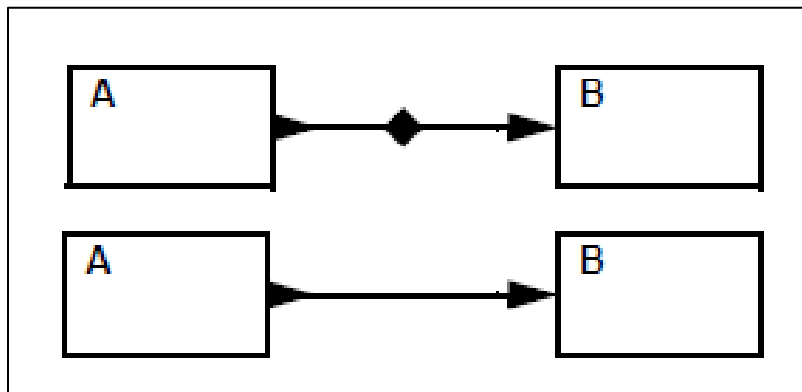


Figure 56. Vertex Example

The above is an example showing how a vertex contained by a relation results in a visual representation of the relation at a specific location (top) vs. a relation with no vertex that is rendered as a wire (bottom). The two connections have the same meaning.

This indicates that the vertex should be rendered at the location 184.0, 93.0.

VisualSim uses ordinary MoML properties to specify other visual aspects of a model. First, an entity can contain a location property, which is a hint to a visual renderer, as follows:

```
<entity name="ramp" class="VisualSim.actor.lib.Ramp">
```

```
<property name="location" class="VisualSim.moml.Location"  
value="50.0, 50.0"/>  
</entity>
```

This suggests to the visual renderer that the Ramp actor should be drawn at location 50.0, 50.0.

12 License Manager

VisualSim provides a standard License Server and FlexLM. FlexLm support is limited to Solaris only. All other platforms and node-locked licenses are supported by the Standard License Server only. Explorer only supports the Standard License Server. Both licenses enable the user to generate statistics and checkout mobile licenses.

To learn more on debugging a license issue, visit the [Installation Guide](#) document.

13 Simulation Technology

13.1 Introduction

The simulators implement various models of computation. Most of these models of computation can be viewed as a framework for component-based design, where the framework defines the interaction mechanism between the components. VisualSim consists of four major simulators-

- Digital
- Digital Untimed
- Continuous Time
- Finite State Machine
- SystemC

Except for the Finite State Machine, all the simulators implement their own scheduling between blocks and do not rely on threads. These usually results in a highly efficient execution. The FSM simulator is in a category by itself, as the components are not producers and consumers of data, but rather are states.

13.2 Models of Computation

A Model of Computation gives an interaction mechanism for components to deal with concurrency and time. The utility of a model of computation stems from the modeling properties that apply to all similar models. For many models of computation these properties are derived through formal mathematics. Depending on the model of computation, the model may be deterministic, statically schedulable, or time safe. Because of its modeling properties, a model of computation represents a style of modeling that is useful in any circumstance where those properties are desirable. In other words, models of computation form design patterns of component interaction, in the same sense that Gamma and others. describe design patterns in object oriented languages.

For a particular application, an appropriate model of computation does not impose unnecessary constraints, and at the same time is constrained enough to result in useful derived properties.

13.3 Simulators- How to select the right one?

1. What are Models of Computation: Govern interaction of components in a model. The simulators share kernel, event queue, and some libraries. The transfer of data and the exchange of timing events between simulators are transparent to the user.
2. Single Kernel vs. Co-Simulation: Synchronization has to be done externally and by each independent kernel. Having independent threads running. SDF + DE in VisualSim vs. VisualSim + VHDL are the difference.
3. Discrete-Event: Execution of synchronous events between asynchronous times. The Calendar Queue maintains sequences of events on a time line. This is similar to Hyperformix Workbench, OPNeT, BONEs, Verilog, and VHDL.
4. Finite State Machine: Case statement in a graphical form defining sequential control logic. The entities represent states and connections represent transitions between states. The execution is a strictly ordered sequence of state transitions. This is similar to Statemate, OPNeT, and Summit Visual FSM.
5. Synchronous Data Flow: Can specify *a priori* the number of input samples consumed on each input and the number of output samples produced on each output each time the block is invoked. The execution is statistical and determined prior to execution. This similar to SPW. Cossap or Synopsys System Studio is a small variation to this in the sense that Cossap evaluates a large number of inputs at every port before moving to the next port/block. This is extremely fast if the model is flow-through. This slows down if there are control elements such as loop-back.
6. Continuous Time: Simulator finds a fixed-point, i.e., a set of continuous-time functions that satisfy all the relations. This solves algebraic or differential relations between inputs and outputs. This is similar to Spice, Simulink and AMS. To determine the best variation of the Continuous Time simulator for your application, refer to Chapter 1, Section 2.4.
7. FSM Hierarchical: A FSM Hierarchical is one that switches between these simple models when the system transitions between regimes or states. A CT + FSM creates a modal model.
8. Mixed-Signal: Embedded systems frequently contain components that are best modeled using differential equations, such as MEMS and other mechanical components, analog circuits, and microwave circuits. These components, however, interact with an electronic system that may serve as a controller or a recipient of sensor data. This electronic system may be digital. Joint

modeling of a continuous subsystem with digital electronics is known as mixed signal modeling.

13.4 Simulators

In this section, we describe models of computation that are implemented in VisualSim simulators.

13.4.1.1 Continuous Time (CT)

In the CT simulator (continuous time), actors represent components that interact via continuous-time signals. Actors typically specify algebraic or differential relations between inputs and outputs. The job of the director in the simulator is to find a fixed-point, that is, a set of continuous-time functions that satisfy all the relations.

The CT simulator includes an extensible set of differential equation solvers. The simulator, therefore, is useful for modeling physical systems with linear or nonlinear algebraic/differential equation descriptions, such as analog circuits and many mechanical systems. Its model of computation is similar to that used in Simulink, Saber, and VHDL-AMS, and is closely related to that in Spice circuit simulators.

Embedded systems frequently contain components that are best modeled using differential equations, such as MEMS and other mechanical components, analog circuits, and microwave circuits. These components, however, interact with an electronic system that may serve as a controller or a recipient of sensor data. This electronic system may be digital. Joint modeling of a continuous subsystem with digital electronics is known as mixed signal modeling. The CT simulator is designed to interoperate with other VisualSim simulators, such as Digital, to achieve mixed signal modeling. To support such mixed-modeling, the CT simulator models the discrete events as Dirac delta functions. It also includes the ability to precisely detect threshold crossings to produce discrete events. Physical systems often have simple models that are only valid over a certain regime of operation. Outside that regime, another model may be appropriate. A modal model is one that switches between these simple models when the system transitions between regimes. The CT simulator interoperates with the FSM simulator to create modal models.

13.4.1.2 Digital (DE)

In the discrete-event (DE) simulator, the actors communicate via sequences of events placed in time, along a real time line. An event consists of a value and time stamp. Actors can either be processes that react to events (implemented as Java threads) or functions that fire when new events are supplied. This model of computation is popular for specifying digital hardware and for simulating telecommunications systems, and has been realized in a large number of simulation environments, simulation languages, and hardware description languages, including VHDL and Verilog.

DE models are excellent descriptions of concurrent hardware, although increasingly the globally consistent notion of time is problematic. In particular, it over-specifies (or over-models) systems where maintaining such a globally consistent notion is difficult, including large VLSI chips with high clock rates. Every event is placed precisely on a globally consistent time line.

The DE simulator implements a sophisticated discrete-event simulator. Other DE simulators in general need to maintain a global queue of pending events sorted by time stamp (this is called a priority queue). This is expensive, as inserting new events into the list requires searching for the right position at which to insert it. The VisualSim DE simulator uses a calendar queue data structure for the global event queue. A calendar queue may be thought of as a hash-table that uses quantized time as a hashing function. As such, both enqueue and dequeue operations can be done in time that is independent of the number of events in the queue.

In addition, the DE simulator gives deterministic semantics to simultaneous events, unlike most competing discrete-event simulators. This means that for any two events with the same time stamp, the order in which they are processed can be inferred from the structure of the model. This is done by analyzing the graph structure of the model for data precedence so that in the event of simultaneous time stamps, events can be sorted according to a secondary criterion given by their precedence relationships. VHDL, for example, uses delta time to accomplish the same objective.

13.4.1.3 Finite State Machine (FSM)

The finite-state machine (FSM) simulator is radically different from the other VisualSim simulators. The entities in this simulator represent not block/actor but rather state and the connections represent transitions between states. Execution is a strictly ordered sequence of state transitions.

The FSM simulator leverages the built-in Expression Language in VisualSim to evaluate guards, which determine when state transitions can be taken.

FSM models are excellent for control logic in embedded systems, particularly safety-critical systems. FSM models are amenable to in-depth formal analysis, and thus can be used to avoid surprising behavior.

FSM models have a number of key weaknesses. First, at a very fundamental level, they are not as expressive as the other models of computation described here. They are not sufficiently rich to describe all partial recursive functions. However, this weakness is acceptable in light of the formal analysis that becomes possible. Many questions about designs are decidable for FSMs and undecidable for other models of computation. A second key weakness is that the number of states can get very large even in the face of only modest complexity. This makes the models unwieldy. Both problems can often be solved by using FSMs in combination with concurrent models of computation. This was first noted by David Harel, who introduced Statechart formalism.

Statecharts combine a loose version of synchronous-reactive modeling (described below) with FSM. FSMs have also been combined with differential equations, yielding the so-called hybrid systems model of computation.

The FSM simulator in VisualSim can be hierarchically combined with other simulators. We call the resulting formalism “*charts” (pronounced “starcharts”) where the star represents a wildcard. As most other simulators represent concurrent computations, *charts model concurrent finite state machines with a variety of concurrency semantics. When combined with CT, they yield hybrid systems and modal models. When combined with SDF (described below), they yield something close to Statecharts.

13.4.1.4 Untimed Digital or Synchronous Data Flow

The synchronous dataflow (SDF) simulator handles regular computations that operate on streams. Dataflow models are popular in signal processing. Dataflow models construct processes as sequences of atomic actor firings. Synchronous dataflow (SDF) is a particularly restricted special case with the extremely useful property that deadlock and boundedness are decidable. Moreover, the schedule of firings, parallel or sequential, is computable statically, making SDF extremely useful specification formalism for embedded real-time software and for hardware.

Certain generalizations sometimes yield to similar analysis. Boolean dataflow (BDF) models sometimes yield to deadlock and boundedness analysis, although fundamentally these questions are undecidable. Dynamic dataflow (DDF) uses only run-time analysis, and thus makes no attempt to statically answer questions about deadlock and boundedness.

13.4.1.5 SystemC

SystemC is an event-driven simulator providing hardware-oriented constructs within the context of C++ as a class library implemented in standard C++. SystemC use spans design and verification from concept to implementation in hardware and software. SystemC provides an interoperable modeling platform which enables the development and exchange of very fast system-level C++ models. It also provides a stable platform for development of system-level tools.

The library provides a set of data types implementing various data representations needed for hardware modeling and certain types of software programming. These include 2-valued and 4-valued bit vectors of arbitrary width, and fixed-point representations. Also included in the core language are modules and ports for representing structure, as well as interfaces and channels that describe communication. Finally, the library includes a set of built-in primitive channels that have wide use such as signals and FIFOs.

A SystemC system consists of a set of one or more modules. Modules provide the ability to describe structure. Modules may contain processes, ports, internal data, channels, and instances of other modules. All processes are conceptually concurrent and can be used to model the functionality of the module. Ports are objects through which the module communicates with other modules. The internal data and channels provide for communication between processes and maintaining module state. Module instances provide for hierarchical structures. The interface, port, and channel structure provides for great flexibility in modeling communication and in model refinement.

13.4.1.6 Wireless Sensor networks

Modeling of wireless sensor networks requires sophisticated modeling of communication channels, sensor channels, ad-hoc networking protocols, localization strategies, media

access control protocols, energy consumption in sensor nodes, and so on. This modeling framework is designed to support a component-based construction of such models. It is intended to share models of disjoint aspects of the sensor nets problem and to build models that include sophisticated elements from several aspects.

13.4.2 Choosing Models of Computation

The rich variety of concurrent models of computation outlined in the previous section can be daunting to a designer faced with having to select them. Most designers today do not face this choice because they get exposed to only one or two.

Embedded software and digital electronics designers exclusively utilize the Discrete-Event simulator while DSP and image processing architects utilize the Synchronous Data Flow. Protocols are best done using the combination of Discrete-Event and Finite State Machine while MEMS and control systems prefer Continuous Time and Finite State Machine. A special case of combining simulators is the Continuous Time and Finite State Machine. This combination is called a Hybrid System.

There are three CT Simulators:

- CTMultiSolverSimulators - Top-level director only
- CTSimulators - Top-level or inside a composite actor
- CTEmbeddedSimulators - Contained only in a CTCompositeActor

In terms of mixing models of computation, all the directors can execute composite actors that implement other models of computation, as long as the composite actors are properly connected. Only CTMixedSignalDirector and CTEmbeddedDirector can be contained by other domains. The outside domain of a composite actor with CTMixedSignalDirector can be Discrete Event. The outside domain of a composite actor with CTEmbeddedDirector must also be CT or FSM, if the outside domain of the FSM model is CT.

An essential difference between concurrent models of computation is their modeling of time.

Some are very explicit by taking time to be a real number that advances uniformly, and placing events on a time line (Discrete-Event) or evolving continuous signals along the time line (Continuous Time). Others are abstract and take time to be discrete (Synchronous Data Flow).

A grand unified approach to modeling would seek a concurrent model of computation that serves all purposes. This could be accomplished by creating a *melange*, a mixture of all of the above, but such a mixture would be extremely complex and difficult to use. Another alternative would be to choose one concurrent model of computation, say the Continuous-Event, and show that all the others are subsumed as special cases. This is relatively easy to do, in theory. Most of these models of computation are sufficiently expressive to be able to subsume most of the others. However, this fails to acknowledge the strengths and weaknesses of each model of computation. Thus, to design interesting systems, designers need to use heterogeneous models.

The approach used in VisualSim is to provide in the infrastructure an *abstract semantics*, rather than a unifying model of computation. It is “abstract” in the sense that it is not a complete model of computation. For example, the abstract semantics of the block package asserts that blocks “fire,” but it says nothing about when they fire. This makes it possible to define blocks that can operate in several simulators (we call these *simulator polymorphic* blocks).

14 Batch Mode Simulation Execution

14.1 Introduction

VisualSim models can be executed from a script to run in a non-interactive mode. The batch mode simulation must be executed from the install directory of VisualSim. For example, if VisualSim is installed in C:\VisualSim16\VS_AR, then script must be executed from this directory. If the script is executed from any other directory, a Null Pointer Exception is generated.

The sequence to simulation model can be executed using any script language. The batch file can contain multiple lines of this script with different parameter values and model file names.

The batch mode simulation cannot handle any graphical display- text or waveforms. So, all text and waveform plots must be set to Save mode before starting the execution. No spaces are permitted in the file names and file paths. This reports an error.

In addition to the standard script format, the user must add any Java options that are used in the VisualSim.bat or VisualSim.sh file that invokes the graphical VisualSim install. This ensures the simulation speed is the same for the graphical and non-graphical editions. The common options would be “-server -Xms1024m -Xmx2048m -XX:MinHeapFreeRatio=50 -XX:MaxHeapFreeRatio=50”.

14.2 Error checking

The Batch mode simulation assumes you have checked all the parameter names, values, paths, and the file name correctly. If you have any error, the simulation simply terminates. Most of the time, it does not generate any errors.

14.3 Batch mode simulation script format

Manually:

The basic format for the Batch Run Execution is:

```
<Path to Java bin directory + java> -classpath <List of paths>
VisualSim.actor.gui.VisualSimBatchModeSimulator -resultpath <Path
to save the simulation summary> -<Parameter Name> <Parameter
Value> ..... <Model Name>
```

where

Option	Required?	Format
<Path to Java bin directory>	Yes	C:\java\jdk1.6.0_07\bin\java- Windows /usr/java/jdk1.6.0_07/bin/java- UNIX
<List of Paths>	Yes	VisualSim Install directory is required. Others fields are optional. (see below for the paths to include)
-resultsummary	Optional	This is a keyword and must not be used as a parameter name. This is used when the user saves the summary for each simulation run in a separate directory.
<Path to save the simulation summary>	Optional	Used only with – resultpath and must follow the keyword. This is the path in the standard OS path structure to save the summary for each simulation run in a separate directory.
-<Parameter Name>	Optional	-Simulation_Time (One corresponding value required) (See below for parameter support)
<Parameter Value>	Optional	1.0

Option	Required?	Format
		(One per parameter name) (See below for data value support)
<Model Name>	Yes	Path + Model Name (See below for format details)

Example:

```
D:\jdk1.6.0_24\bin\java -classpath D:/VisualSim/VS_AR
VisualSim.actor.gui.VisualSimBatchModeSimulator -resultpath C:\VisualSim\User_Library -
Input_Rate 1.0 -Execution_Time 2.5
file:/D:/VisualSim/VS_AR/doc/Training_Material/Tutorials/Part3.xml
```

14.3.1 List of Paths

The -classpath contains the VisualSim install directory. Other directories are not required but can be added as required. The format for Windows is **-classpath file_path1;file_path2...** **without the ""** and for UNIX is **-classpath file_path1:file_path2....**

Example of VisualSim install directory format:

```
C:\VisualSim\VisualSim14- Windows
/usr/VisualSim/VisualSim14- UNIX
```

14.3.2 Path to save the Batch simulation results file

The -resultpath is an optional argument for the simulation execution control. The format for Windows is **-resultpath file_path1** without any "".

Example of directory format:

```
C:\VisualSim\VisualSim14- Windows
```

/usr/VisualSim/VisualSim14- UNIX

14.3.3 Parameter Name

The script can accept top-level parameters, parameter in hierarchical block or a block parameter. The format is “**-parameter_name parameter_value -parameter_name parameter_value, -Block_name.parameter_name parameter_value ...**”. The list can contain any number of parameters. It is necessary to include only those parameters that need to be modified. Lower level parameters can be included by providing their Window Name in the order to reach the lowest hierarchical level.

1. Top-level: Simulation_Time
2. Hierarchical Block: Hierarchical Block Name.Parameter Name (Eg: Processor_Block.CPU_Speed)
3. Block Parameter: Digital.startTime

14.3.4 Parameter Value

All standard data types are supported here. The format must match whatever the default value used in model when initializing the parameters. Parameters listed in the parameter set are also supported here. The only restriction is that strings used inside a array or otherwise must be enclosed in \”. For example, “DRAM1” must be written as “\”DRAM1\”.

Data types supported:

Basic: string, integer, double, long, boolean,

Complex: data structures (all types), matrix (all types), arrays (all types)

If the script contains a variable that is set first and then used as a value in the simulation line, make sure there are no spaces after the “=” or extra spaces on Linux side.

For example,

this line is correct:

```
set num=5
```



```
java -classpath C:/VS VisualSim.actor.gui.VisualSimBatchModeSimulator -Param %num%
file:/C:/VS /Model.xml
```

while, this line is incorrect:

```
set num= 5 (Space is not permitted)
```

```
java -classpath C:/VS VisualSim.actor.gui.VisualSimBatchModeSimulator -Param %num%
file:/C:/VS /Model.xml
```

14.3.5 Model Name

The last item in the line is the file name. The preferred format is to use the URL technique. This would be “file:/D:/VisualSim/Model_Example.xml” on Windows and “file://VisualSim/Model_Example.xml” on Linux.

If the model file is within the VisualSim install, the format for Windows is “User_Library/Model/Command_Line_Modeling.xml” and for UNIX is “. /User_Library/Model/Command_Line_Modeling.xml “.

An alternate option is to use “\$VS/User_Library/Model/Command_Line_Modeling.xml”.

To get the URL format, open the file in VisualSim Architect or in a Web Browser, and copy the URL address shown.

14.3.6 Using Post Processor to create the batch file .

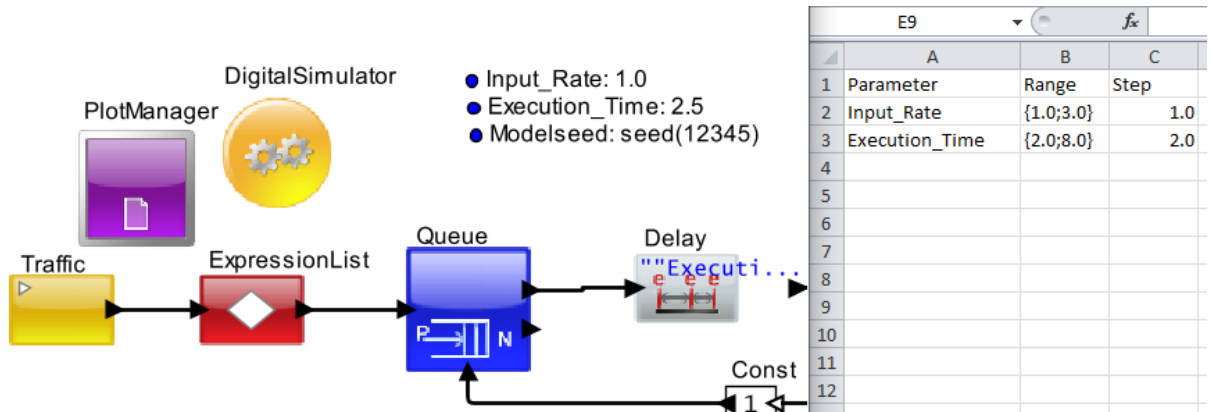
1. Create the csv file and save the file where the model file(.xml) is saved.
2. Give the parameter name and values in (Range column)in the csv file as shown

	A	B	C
1	Parameter	Range	Step
2	Input_Rate	{1;3}	1
3	Execution_Time	{2;8}	2

3. The parameter name should match with the model parameter name.

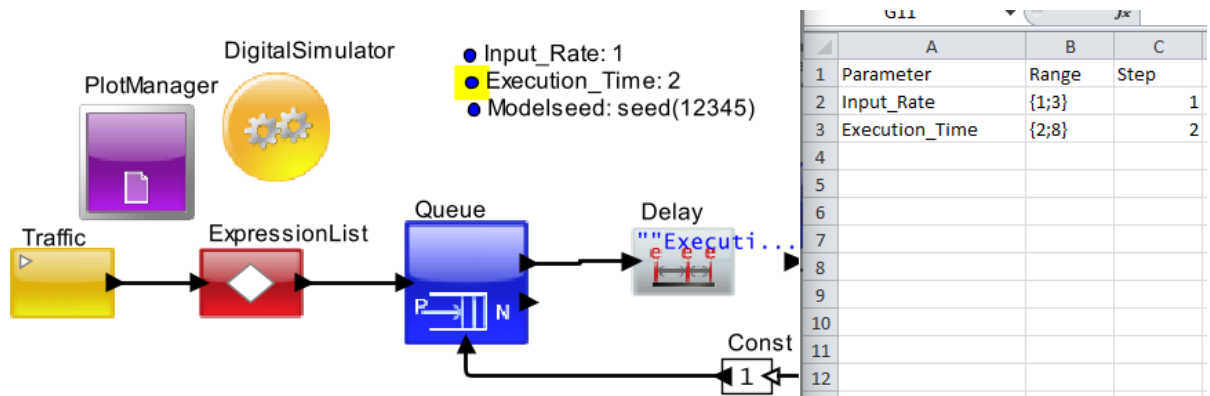
4. If the values in the model paramter are in decimal, provide the decimal values in the csv column – Range and Step.

5. Refer to the image –



6. If the values in the model paramter are in integer, provide the integer values in the csv column – Range and Step.

7. Refer to the image –



8. Configure the model using postprocessor. (Activity -> Configure Model)

9. ModelName_index.xml file will be generated.

10. Run PostProcessor -> Batch Generator -> Generate batch/ shell file

11. Go to the folder where the csv file and model is saved, first select csv file , then select model.

12. Sim_Batch_Run.bat / Sim_Batch_Run.sh will be created, in the same folder where the model is saved.

13. To run the batch file on different CPU core –

1. Go to VS_AR folder.
2. Run the ThreadSimCore.bat / ThreadSimCore.sh file .
3. Enter the location of the file Sim_Batch_Run.bat / Sim_Batch_Run.sh. for example:

```
C:\VisualSim\VisualSim2030_64_beta\VS_AR\lib\mohini\simulation\part_index_model\Sim_Batch_Run.bat
```

14.4 Viewers, Ploters and Text Displays

Models run in batch mode must not contain any graphical viewers or interactive windows. All plots, results and statistics must be written to file. If you have ViewPlot or ViewText enabled in any display, you get the following error:

```
----- Exception Reported -----
VisualSim.kernel.util.IllegalActionException: Cannot find effigy for top level: .Model1
in .Model1.Hblock1.HHBlock1.Display_Plotter
-----
```

The paths in any file write is relative to the <VisualSim install directory> from where the batch file is being executed. If the VisualSim_batch_mode_run.bat(.sh) is executed from C:/VisualSim/VS (/VisualSim/VS), then the file paths for all the writes are relative to this position. You get the following error if the directory does not exist.

```
----- Exception Reported -----
```

VisualSim.kernel.util.IllegalActionException: Exception, writeFile, File Path:
Stats_of_Controller.txt

Exception Reported: java.lang.IllegalArgumentException: URI is not absolute

The best file name options are:

1. Filename.txt
2. Results/Filename.txt (Saved in \$VS/Results folder)
3. C:/VisualSim/Models/Filename.txt

14.5 Output

14.5.1 Model statistics

All statistics, plots and files are saved in the directories specified by the respective block parameters.

14.5.2 Summary

The success or failures of the simulation runs are reported on the terminal windows executing the script and in the "**Batch_Mode_Results_Summary.txt**". This file is saved in the VisualSim install directory or in the path provided by `-resultpath` parameter.

If the file does not exist, a new file is created. The file format is as follows:

```
Start t      12345678100      Model: MyModel_1
End   t      12345678200      Model: MyModel_1
Start t      12345678200      Model: MyModel_2
```

```
----- Exception Reported -----
"Exception message"
```

End t 12345678250 Model: MyModel_2

14.5.3 Saving text and Plots

The saving folder must exist. The following formats work correctly in the Command-Line version:

\$VS/User_Library/Folder/results

\$CLASSPATH/User_Library/Folder/results

FileName

If you use any other format, you get the following error message:

15 Pause and Resume function with Debugging facility

VisualSim Architect has a debugging and step simulation facility that allows users to specify time stamps to pause simulation and enables the user to save the simulation data and restart from that time stamp even after closing the tool. This feature enables the user to save the simulation data every day or every time they close the software when they have to run large simulation models for days. This eliminates the requirement of running simulation continuously till the simulation end point is reached.

The pause and resume functions can also be used for debugging facility as well. User can pause for a given timestamp and analyze the system response and continue simulation step by step.

The system can be analyzed for required functionality and also helps the designer to identify if the crucial tasks are being executed in the given timing deadlines.

15.1 How to Use Pause and Resume Function

Current version supports models with SystemResource, Servers, Queues, and Script.

Make sure you have the file PauseSimulationAt.txt in the same directory. This file has the timestamps for pausing simulation.

15.2 Steps:

1. Run Simulation by clicking the green arrow button in tool bar or press CTRL+R.
2. Pause Simulation by clicking the Pause button in tool bar
3. Click on Save As.
4. Select the check box "Save Simulation Data".
5. Give Name for the model with .xml extension.
6. Click on Ok.
7. .bin file is created in the same directory and this file has the Simulation data.
8. Close VisualSim Architect.
9. Start VisualSim Architect.
10. Open the .xml file saved in the previous step.
11. Model starts running from the time stamp where it was stopped. The Model runs till it reaches the next time stamp for pause.

16 Auto-Save

VisualSim provides the ability for the user to continuously save the currently open model, if they are modified. The interval between the saves is set in the VSconfig.properties. The format is:

```
Auto_Save_Time=2
```

Where the number on the RHS is the time interval between saves.

The intermediate xml files are saved in the <User Home>/VisualSim directory. The format is as follows:

```
Scheduler_SW_FCFS_Preempt_20151127_143903.xml
```

Where

File Name: Scheduler_SW_FCFS_Preempt

Date: 20151127- Here is it 2017 February 02

Time: 143903 is 2:39:03 PM

Note: The intermediate files are not deleted when the model is saved or VisualSim is closed.

17 Data Types

17.1 Scalar and Numerical Values

- Numerical values without decimal points, such as "10" or "-3" are integers of type *int*.
- Numerical values with decimal points, such as "10.0" or "3.14159" are of type *double*.
- Numerical values without decimal points followed by the character "l" (el) or "L" are of type *long*.
- Unsigned integers followed by "µb" or "UB" are of type *unsignedByte*, as in "5µb". An *unsignedByte* has a value between 0 and 255.
- Numbers of type *int*, *long*, or *unsignedByte* can be specified in decimal, octal or hexadecimal. Numbers beginning with a leading "0" are octal numbers. Numbers beginning with a leading "0x" is hexadecimal numbers. For example, "012" and "0xA" are both equal to the integer 10.
- A *complex* is defined by appending an "i" or a "j" to a double for the imaginary part. This gives a purely imaginary complex number which can then leverage the polymorphic operations in the Token classes to create a general complex number. Thus "2 + 3i" results in the expected complex number. You can optionally write this as "2 + 3*i".

Scalar values use a 64 bit with 54 bits mantissa, 1 bit mantissa sign, 8 bits exponent and 1 bit exp sign. All numerical values are stored as tokens which contain the values, in the above format, and the type. All math operations are done with full resolution. Basic math functions are built into the token for simulation speed. For all other basic functions, Java math and Java extended math are used. All other functions are custom built in the RegEx language.

17.2 String Constants

Anything between double quotes, "...", is interpreted as a string constant. The built-in string-valued constants are shown in the RegEx section of this document.

17.3 Arrays

Arrays are specified with curly brackets, for example, "{1, 2, 3}" is an array of *integer*, while {"x", "y", "z"} is an array of *string*. The types are denoted "{int}" and "{string}" respectively. "{1, 2, 3}" is a single-dimension array while "{{1, 2, 3},{4,5,6}}" is a multi-dimension array. An array is an ordered list of tokens of any type, with the only constraint being that the elements all have the same type. If an array is given with mixed types, the expression evaluator attempts to losslessly convert the elements to a common type. Thus, for example,

```
{1, 2.3}
```

has value

```
{1.0, 2.3}
```

Its type is {double}. The elements of the array can be given by expressions, as in the example "{2*pi, 3*pi}". The elements of an array can be accessed as follows:

```
>> {1.0, 2.3} (1)
```

```
2.3
```

which yields 2.3.



Note

Note that indexing begins at 0. All array operations are listed in the RegEx section.

An array can be accessed by the name and index as follows:

Single-dimension:

```
>> x = {1.0, 2.3}
```

```
{1.0, 2.3}
```

```
>> x(0)
```

```
1.0
```

Multi-dimension:

```
>> a = {{1,2,3},{4,5,6}}
```

```
{{1, 2, 3}
```

```
, {4, 5, 6}
```

```
}
```

```
>> a(0)(0)
```

```
1
```

Arithmetic operations on arrays are carried out element-by-element, as shown by the following examples:

```
>> {1, 2} * {2, 2}
```

```
{2, 4}
```

```
>> {1, 2} + {2, 2}
```

```
{3, 4}
```

```
>> {1, 2} - {2, 2}
```

```
{-1, 0}
```

```
>> {1, 2} ^ 2
```

```
{1, 4}
```

```
>> {1, 2} % {2, 2}
```

```
{1, 0}
```

An array can be checked for equality with another array as follows:

```
>> {1, 2} == {2, 2}
```

```
false
```

```
>> {1, 2}!={2, 2}
```

```
true
```

For other comparisons of arrays, use `compare()` function. As with scalars, testing for equality using the `==` or `!=` operators tests the values, independent of type. For example,

```
>> {1, 2}=={1.0, 2.0}
```

```
true
```

You can extract a subarray by invoking `subarray()` method as follows:

```
>> {1, 2, 3, 4}.subarray(2, 2)
```

```
3, 4}
```

The first argument is the starting index of the subarray and the second argument is the length.

You can also extract non-contiguous elements from an array using `extract()` method. This method has two forms:

1. The first form takes a boolean array of the same length as the original array which indicates which elements to extract, as in the following example:

```
>> {"red", "green", "blue"}.extract({true, false, true})
```

```
{"red", "blue"}
```

2. The second form takes an array of integers giving the indices to extract, as in the following example:

```
>> {"red", "green", "blue"}.extract({2, 0, 1, 1})
```

```
{"blue", "red", "green", "green"}
```

To add an additional item to the array, you use the `append` function. There are a few variations also available.

Single Array

```
>> a = {1, 2, 3}
```

```
{1, 2, 3}
```

```
>> a = a.append(4)
```

```
{1, 2, 3, 4}
```

Multi-dimension Array

```
>> a = {{1,2,3},{4,5,6}}
```

```
{{1, 2, 3}
```

```
, {4, 5, 6}
```

```
}
```

```
>> a = append(a,7)
```

```
{{1, 2, 3, 7}
```

```
, {4, 5, 6, 7}
```

```
}
```

```
>> a = a.append({7,8,9,10})
```

```
{{1, 2, 3, 7}
```

```
, {4, 5, 6, 7}
```

```
, {7, 8, 9, 10}
```

```
}
```

To search the array, you can use the `find` (returns an index) or `search` (list of values).

```
>> a = {true,false,false}
```

```
{true, false, false}
```

```
>> b = find(a)
```

```
{0}
```

```
>> a = {1,2,3,4}
```

```
{1, 2, 3, 4}
>> x = find(a,2)
{1}
>> b = {{1,2,3},{4,5,6}}
{{1, 2, 3}
, {4, 5, 6}
}
>> x = find(b(1),4)
{0}
>> a
{1, 2, 3, 4}
>> X=search(a, 3,1)
2
```

17.4 Matrices

In VisualSim, arrays are ordered as sets of tokens. VisualSim also supports matrices, which are more specialized than arrays. They contain only certain primitive types, currently Boolean, complex, double, fixedpoint, int, and long. UnsignedByte matrices are not supported. Matrices cannot contain arbitrary tokens, so they cannot, for example, contain matrices. They are intended for data intensive computations.

Matrices are specified with square brackets, using commas to separate row elements and semicolons to separate rows. For example, "[1, 2, 3; 4, 5, 5+1]" gives a two by three integer matrix (2 rows and 3 columns). Note that an array or matrix element can be given by an expression. A row vector can be given as "[1, 2, 3]" and a column vector as "[1; 2; 3]". Some MATLAB-style array constructors are supported. For example, "[1:2:9]" gives an array of odd numbers from 1 to 9, and is equivalent to "[1, 3, 5, 7, 9]". Similarly, "[1:2:9; 2:2:10]" is equivalent to "[1, 3, 5, 7, 9; 2, 4, 6, 8, 10]". In the syntax "[p:q:r]", p is the first element, q is the

step between elements, and *r* is an upper bound on the last element. That is, the matrix does not contain an element larger than *r*. If a matrix with mixed types is specified, then the elements are converted to a common type, if possible. Thus, for example, "[1.0, 1]" is equivalent to "[1.0, 1.0]," but "[1.0, 1L]" is illegal (because there is no common type to which both elements can be converted losslessly).

Reference to elements of matrices have the form "matrix(*n*, *m*)" or "name(*n*, *m*)" where name is the name of a matrix variable in scope, *n* is the row index, and *m* is the column index. Index numbers start with zero, as in Java, not 1, as in MATLAB. For example,

```
>> [1, 2; 3, 4](0,0)
1
>> a = [1, 2; 3, 4]
[1, 2; 3, 4]
>> a(1,1)
4
```

Matrix multiplication works as expected. For example, (as seen in the expression evaluator)

```
>> [1, 2; 3, 4]*[2, 2; 2, 2]
[6, 6; 14, 14]
```

Of course, if the dimensions of the matrix do not match, then you get an error message. To do element wise multiplication, use the `multiplyElements()` function. Matrix addition and subtraction are element wise, as expected, but the division operator is not supported. Element wise division can be accomplished with the `divideElements()` function, and multiplication by a matrix inverse can be accomplished using the `inverse()` function. A matrix can be raised to an int or unsignedByte power, which is equivalent to multiplying it by itself some number of times. For instance,

```
>> [3, 0; 0, 3]^3
[27, 0; 0, 27]
```

A matrix can also be multiplied or divided by a scalar, as follows:

```
>> [3, 0; 0, 3]*3  
[9, 0; 0, 9]
```

A matrix can be added to a scalar. It can also be subtracted from a scalar, or have a scalar subtracted from it. For instance,

```
>> 1-[3, 0; 0, 3]  
[-2, 1; 1, -2]
```

A matrix can be checked for equality with another matrix as follows:

```
>> [3, 0; 0, 3]!= [3, 0; 0, 6]  
true  
  
>> [3, 0; 0, 3]== [3, 0; 0, 3]  
true
```

For other comparisons of matrices, use the `compare()` function. As with scalars, testing for equality using the `==` or `!=` operators tests the values, independent of type. For example,

```
>> [1, 2]==[1.0, 2.0]  
true
```

To get type-specific equality tests, use the `equals()` method, as in the following examples:

```
>> [1, 2].equals([1.0, 2.0])  
false  
  
>> [1.0, 2.0].equals([1.0, 2.0])  
true  
  
>>
```



ExpressionList and Script blocks do not support the assignment of values to a matrix. You cannot have an existing matrix on the LHS of an expression.

Caution

17.5 Data Structure or Transaction or Record Token

A Data Structure is a class type containing named fields and associated value. The value of each field can have a distinct type. Data Structures are delimited by curly braces, with each field given a name. For example, "{a=1, b="foo"}" is a data structure with two fields, named "a" and "b", with values 1 (an integer) and "foo" (a string), respectively. The value of a field can be an arbitrary expression, and data structures can be nested (a field of A data structure may be A data structure).

Fields may be accessed using the period operator. For example,

```
{a=1,b=2}.a
```

yields 1. You can optionally write this as if it were a method call:

```
{a=1,b=2}.a()
```

The arithmetic operators +, -, *, /, and % can be applied to data structures. If the data structures do not have identical fields, then the operator is applied only to the fields that match, and the result contains only the fields that match. Thus, for example,

```
{foodCost=40, hotelCost=100} + {foodCost=20, taxiCost=20}
```

yields the result

```
{foodCost=60}
```

You can think of an operation as a set intersection, where the operation specifies how to merge the values of the intersecting fields. You can also form an intersection without applying an operation. In this case, using the intersect() function, you form a data structure that has only the common fields of two specified data structures, with the values taken from the first data structure. For example,

```
>> intersect({a=1, c=2}, {a=3, b=4})
```



```
{a=1}
```

Data structures can be joined (think of a set union) without any operation being applied by using the `merge()` function. This function takes two arguments, both of which are data structures. If the two data structures have common fields, then the field value from the first data structure is used. For example,

```
merge({a=1, b=2}, {a=3, c=3})
```

yields the result `{a=1, b=2, c=3}`.

Data structures can be compared, as in the following examples:

```
>> {a=1, b=2}!={a=1, b=2}
```

```
false
```

```
>> {a=1, b=2}!={a=1, c=2}
```

```
true
```

Note that two data structures are equal only if they have the same field labels and the values match. As with scalars, the values match irrespective of type. For example:

```
>> {a=1, b=2}=={a=1.0, b=2.0+0.0i}
```

```
true
```

The order of the fields is irrelevant. Hence

```
>> {a=1, b=2}=={b=2, a=1}
```

```
true
```

Moreover, data structure fields are reported in alphabetical order, irrespective of the order in which they are defined. For example,

```
>> {b=2, a=1}
```

```
{a=1, b=2}
```

To get type-specific equality tests, use the `equals()` method, as in the following examples:

```
>> {a=1, b=2}.equals({a=1.0, b=2.0+0.0i})
```

```
false
>> {a=1, b=2}.equals({b=2, a=1})
true
>>
```

17.6 Invoking Methods

Every element and sub-expression in an expression represents an instance of the `Token` class in `VisualSim` (or more likely, a class derived from `Token`). The expression language supports invocation of any method of a given token, as long as the arguments of the method are of type **Token** and the return type is **Token** (or a class derived from `Token`, or something that the expression parser can easily convert to a token, such as a string, double, int, and so on.). The syntax for this is `(token).methodName(args)`, where `methodName` is the name of the method and `args` is a comma-separated set of arguments. Each argument can itself be an expression. Note that the parentheses around the token are not required, but might be useful for clarity. As an example, the `Array Token` and `Data Structure` classes have a `length()` method, illustrated by the following examples:

```
{1, 2, 3}.length()
{a=1, b=2, c=3}.length()
```

each of which returns the integer 3.

The `MatrixToken` classes have three particularly useful methods, illustrated in the following examples:

```
[1, 2; 3, 4; 5, 6].getRowCount()
```

which returns 3, and

```
[1, 2; 3, 4; 5, 6].getColumnCount()
```

which returns 2, and

```
[1, 2; 3, 4; 5, 6].toArray()
```

which returns {1, 2, 3, 4, 5, 6}. The latter function can be particularly useful for creating arrays using MATLAB-style syntax. For example, to obtain an array with the integers from 1 to 100, you can enter:

```
[1:1:5].toArray()
>>{1,2,3,4,5}

[1:2:5].toArray()
>> {1, 3, 5}
```

17.7 Defining Functions

The expression language supports definition of functions. The syntax is:

```
function(arg1:Type, arg2:Type...)
    function body
```

where "function" is the keyword for defining a function. The type of an argument can be left unspecified, in which case the expression language attempts to infer it. The function body gives an expression that defines the return value of the function. The return type is always inferred based on the argument type and the expression. For example:

```
function(x:double) x*5.0
```

defines a function that takes a double argument, multiplies it by 5.0, and returns a double. The return value of the above expression is the function itself. Thus, for example, the expression evaluator yields:

```
>> function(x:double) x*5.0
(function(x:double) (x*5.0))
>>
```

To apply the function to an argument, simply do

```
>> (function(x:double) x*5.0) (10.0)

50.0

>>
```

Alternatively, in the expression evaluator, you can assign the function to a variable, and then use the variable name to apply the function. For example,

```
>> f = function(x:double) x*5.0
      (function(x:double) (x*5.0))
>> f(10)
50.0
>>
```

Functions can be passed as arguments to certain "higher-order functions" that have been defined. For example, the `iterate()` function takes three arguments, a function, an integer, and an initial value to apply the function. It applies the function first to the initial value, then to the result of the application, and finally to that result, collecting the results into an array whose length is given by the second argument. For example, to get an array whose values are multiples of 3, try

```
>> iterate(function(x:int) x+3, 5, 0)
{0, 3, 6, 9, 12}
```

The function given as an argument simply adds three to its argument. The result is the specified initial value (0) followed by the result of applying the function once to that initial value, then twice, then three times, and so on.

Another useful higher-order function is the `map()` function. This one takes a function and an array as arguments, and simply applies the function to each element of the array to construct a result array. For example,

```
>> map(function(x:int) x+3, {0, 2, 3})
{3, 5, 6}
```

A typical use of functions in a VisualSim model is to define a parameter in a model whose value is a function. Suppose that the parameter named "f" has value "function(x:double) x*5.0". Then within the scope of that parameter, the expression "f(10.0)" yields the result 50.0.

Functions can also be passed along connections in a VisualSim model. Consider the model shown in figure.

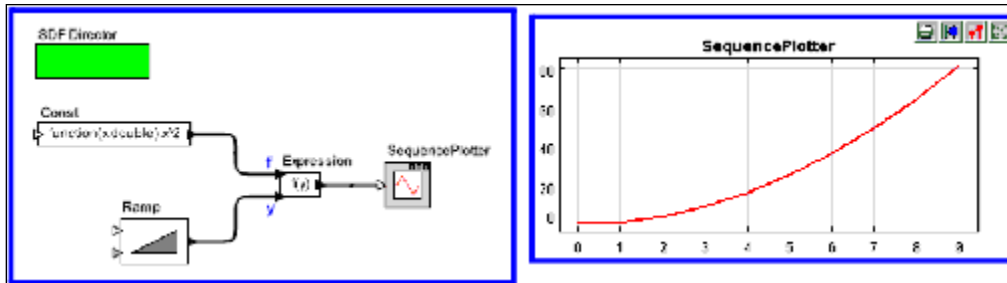


Figure 57. Example of a function being passed from one actor to another

The Const actor defines a function that simply squares the argument. Its output, therefore, is a token with type function. That token is fed to the "f" input of the Expression actor. The expression uses this function by applying it to the token provided on the "y" input. That token, in turn, is supplied by the Ramp block, so the result is the curve shown in the plot on the right.

A more elaborate use is shown in the following figure:

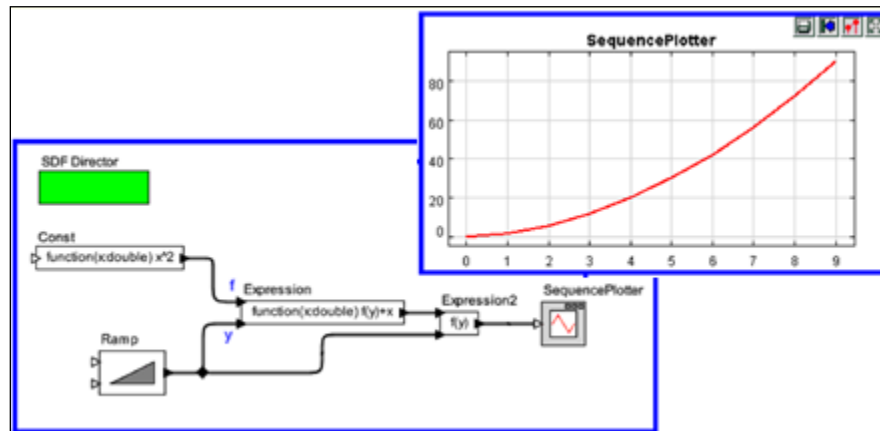


Figure 58. Elaborate use

The Const actor produces a function, which is then used by the Expression actor to create new function, which is finally used by Expression2 to perform a calculation. The calculation performed here adds the output of the Ramp to the square of the output of the Ramp.

Functions can be recursive, as illustrated by the following (rather arcane) example:

```
>> fact = function(x:int,f:(function(x,f) int)) (x<1?1:x*f(x-1,f))
```

```

(function(x:int, f:function(a0:general, a1:general) int)
(x<1)?1:(x*f((x-1), f)))

>> factorial = function(x:int) fact(x,fact)

(function(x:int) (function(x:int, f:function(a0:general,
a1:general) int) (x<1)?1:(x*f((x-1), f)))(x, (function(x:int,
f:function(a0:general, a1:general) int) (x<1)?1:(x*f((x-1), f)))))

>> map(factorial, [1:1:5].toArray())

{1, 2, 6, 24, 120}

>>

```

The first expression defines a function named "fact" that takes a function as an argument, and if the argument is greater than or equal to 1, uses that function recursively. The second expression defines a new function "factorial" using "fact." The final command applies the factorial function to an array to compute factorials.

17.8 Fixed Point Numbers

VisualSim includes a preliminary fixed point data type. We represent a fixed point value in the expression language using the following format:

```
fix(value, totalBits, integerBits)
```

Thus, a fixed point value of 5.375 that uses 8 bit precision of which 4 bits are used to represent the (signed) integer part can be represented as:

```
fix(5.375, 8, 4)
```

The value can also be a matrix of doubles. The values are rounded, yielding the nearest value representable with the specified precision. If the value to represent is out of range, then it is saturated, meaning that the maximum or minimum fixed point value is returned, depending on the sign of the specified value. For example,

```
fix(5.375, 8, 3)
```

yields 3.968758, the maximum value possible with (8/3) precision.

In addition to the `fix()` function, the expression language offers a `quantize()` function. The arguments are the same as those of the `fix()` function, but the return type is a `DoubleToken` or `DoubleMatrixToken` instead of a `FixToken` or `FixMatrixToken`. This function can therefore be used to quantize double-precision values without ever explicitly working with the fixed-point representation.

To make the `FixToken` accessible within the expression language, the following functions are available:

To create a single `FixPoint Token` using the expression language:

```
fix(5.34, 10, 4)
```

This creates a `FixToken`. In this case, we try to fit the number 5.34 into a 10 bit representation with 4 bits used in the integer part. This may lead to quantization errors. By default the round quantizer is used.

To create a `Matrix with FixPoint values` using the expression language:

```
fix([ -.040609, -.001628, .17853 ], 10, 2)
```

This creates a `FixMatrixToken` with 1 row and 3 columns, in which each element is a `FixPoint value` with precision (10/2). The resulting `FixMatrixToken` tries to fit each element of the given double matrix into a 10 bit representation with 2 bits used for the integer part. By default, the round quantizer is used.

To create a single `DoubleToken`, which is the quantized version of the double value given, use the expression language:

```
quantize(5.34, 10, 4)
```

This creates a `DoubleToken`. The resulting `DoubleToken` contains the double value obtained by fitting the number 5.34 into a 10 bit representation with 4 bits used in the integer part. This may lead to quantization errors. By default the round quantizer is used.

To create a `Matrix with doubles quantized to a particular precision` using the expression language:

```
quantize([ -.040609, -.001628, .17853 ], 10, 2)
```

This creates a DoubleMatrixToken with 1 row and 3 columns. The elements of the token are obtained by fitting the given matrix elements into a 10 bit representation with 2 bits used for the integer part. Instead of being a fixed point value, the values are converted back to their double representation and by default the round quantizer is used.

17.9 Special Functions

Few functions have sufficiently subtle properties that require further explanation. That explanation is here.

```
eval()
```

The built-in function `eval()` evaluates a string as an expression in the expression language. For example,

```
eval("[1.0, 2.0; 3.0, 4.0]")
```

returns a matrix of doubles. The following combination can be used to read parameters from a file:

```
eval(readFile("filename"))
```

where the filename can be relative to the current working directory (where VisualSim was started, as reported by the property `user.dir`). The user's home directory (as reported by the property `user.home`), or the classpath, includes the directory tree in which VisualSim is installed.



Note

If `eval()` is used in an expression, it is impossible for the type system to infer any more specific output type than general. If you need the output type to be more specific, then you need to cast the result of `eval()`.

Note that if `eval()` is used in an expression, it is impossible for the type system to infer any more specific output type than general. If you need the output type to be more specific, then you need to cast the result of `eval()`. For example, to force it to type double:

```
>> cast(double, eval("pi/2"))
```




```
1.5707963267949
```

```
traceEvaluation()
```

The `traceEvaluation()` function evaluates an expression given as a string, much like `eval()`, but instead of reporting the result, reports exactly how the expression was evaluated. This can be used to debug expressions, particularly when the expression language is extended by users.

17.10 Distributions

VisualSim provides a large number of distributions as blocks and in the RegEx. The random numbers generated can be arrays or single values. There are two types of RegEx random distributions - Random and Gaussian.

 Seed	To see the distribution seed, the user must have a top-level parameter called <code>model_seed</code> with value of <code>seed(integer value)</code> . The Traffic block and the Basic Processing blocks have the model seed as the parameter of each block. These blocks do not use the <code>model_seed</code> parameter.
--	---

The RegEx distribution functions use a different seed for each run. To make each simulation run have the same seed, the user must have a top-level parameter called `model_seed`. The parameter value is `seed (integer value)`. The Traffic and the Basic Processing blocks have the model seed as the parameter of each block. These blocks do not use the `model_seed` parameter.

The functions `random()` and `gaussian()` return one or more random numbers. With minimum number of arguments (zero or two, respectively), they return a single number. With one additional argument, they return an array of the specified length. With a second additional argument, they return a matrix with the specified number of rows and columns.

The `irand` and `rand` have two arguments and return an integer and double value respectively. There is also a random distribution associated with the integer token which can be used to speed up the random number generation.

There is a key subtlety when using these functions in VisualSim. In particular; they are evaluated only when the expression within which they appear is evaluated. For example, if the value parameter of the Const block is set to "random()", then its output is a random constant, that is, it does not change on each firing. The same is true for parameter also. If the model seed is not set, the output changes on successive runs of the model. In contrast, if this is used in an ExpressionList or Script block, then each firing triggers an evaluation of the expression, and consequently results in a new random number.

17.11 `property()`

The `property()` function accesses system properties by name. Some possibly useful system properties are:

- **VisualSim.VS.dir**: The directory in which VisualSim is installed.
- **VisualSim.VS.dirAsURL**: The directory in which VisualSim is installed, but represented as an URL.
- **user.dir**: The current working directory, which is usually the directory in which the current executable was started.

17.12 `remainder()`

This function computes the remainder operation on two arguments as prescribed by the IEEE 754 standard, which is not the same as the modulo operation computed by the `%` operator. The result of `remainder(x, y)` is $(x-yn)$, where n is the integer closest to the exact value of x/y . If two integers are equally close, then n is the integer that is even. This yields results that may be surprising, as indicated by the following examples:

```
>> remainder(1,2)
1.0
```

```
>> remainder(3,2)
-1.0
Compare this to
>> 3%2
1
```

which is different in two ways. The result numerically different and is of type int, whereas remainder() always yields a result of type double.

If either argument is NaN, or the first argument is infinite, or the second argument is positive zero or negative zero, then the result is NaN.


If the first argument is finite and the second argument is infinite, then the result is the same as the first argument.

17.13 Power and Modulo

The ^ operator computes "to the power of" or exponentiation where the exponent can only be an *int* or an *unsignedByte*.

The *unsignedByte*, *int* and *long* types can only represent integer numbers. Operations on these types are integer operations, which can sometimes lead to unexpected results. For instance, 1/2 yields 0 if 1 and 2 are integers, whereas 1.0/2.0 yields 0.5. The exponentiation operator '^' when used with negative exponents can similarly yield unexpected results. For example, 2^-1 is 0 because the result is computed as 1/(2^1).

The % operation is a **Modulo** or **Remainder Operation**. The result is the remainder after division. The sign of the result is the same as that of the dividend (the left argument).

 <p>Example</p>	<pre>>> 3.0 % 2.0 1.0 >> -3.0 % 2.0 -1.0 >> -3.0 % -2.0</pre>
---	---

	-1.0
	>> 3.0 % -2.0
	1.0

The magnitude of the result is always less than the magnitude of the divisor (the right argument). Note that when this operator is used on doubles, the result is not the same as that produced by the remainder() function. For instance,

```
>> remainder(-3.0, 2.0)
```

```
1.0
```

The remainder() function calculates the IEEE 754 standard remainder operation. It uses a rounding division rather than a truncating division, and hence the sign can be **positive** or **negative**, depending on complicated rules. For example, counter intuitively,

```
>> remainder(3.0, 2.0)
```

```
-1.0
```

18 Data Structures

18.1 Introduction

Data Structures are the signals or transactions that propagate from block to block along the wires between ports. Data Structures are the equivalent to a packet on a network or a collection of wires/pins on a chip or a message between methods in software. The Data Structure contains a number of fields with unique names.

Every block in a model operates and makes decisions on the content of the Data Structures. For example a Traffic Generator would create a Data Structure with certain content, at a certain time and transfer it to the next block, which could be a queue. The queue block could reorder the queue storage based on the field of this data structure called "Priority".

Data Structure fields can be manipulated by the **ExpressionList**, **Script**, and **Custom-coded** blocks. All other blocks use the field values to make decisions such as routing, execute, Read or Write operations and implement delays.

18.2 Layout

A data structure contains a number of rows and each row contains a Field name and a Value. A Data Structure in VisualSim looks like this:

Field Name	Field Value
{BLOCK	"Traffic"
DELTA	0.0
DS_NAME	"DS_Traffic"
Field1	1.0
Field2	"str"
Field3	True
ID	1
INDEX	0
TIME	1.0E-10}

All data structures comprise six (6) header rows. These are:

Field Name	Field Description	Type
BLOCK	Name of Source Block	String
DS_NAME	Name of Data Structure Template	String
DELTA	User Settable Field. This field can be used to store intermediate values that might be needed for a calculation elsewhere in the model.	Double
TIME	Simulation time when DS was created. This is a time stamp that can be used to compute the latency and/or to determine deadline triggers.	Double
INDEX	User Settable Field. This field can be used to store intermediate values that might be needed for a calculation elsewhere in the model.	Integer
ID	Unique ID of each Data Structure from each source. This is a increasing sequence number.	Integer

The remaining are user-defined fields. There can be any number of user-defined fields. The types of the user-defined fields are inferred from the initial value. The three user-defined fields from the above example are:

Data Structure Field Name	Field Type	Field Value
Field1	Double	1.0
Field2	String	str
Field3	Boolean	true

18.3 Supported Data Types

The fields of the data structure support the following data types:

Data Type	Example
Integer	20
Long	2L
Double	1.0
String	"L2_Cache"
Boolean	true or false
Data Structure	{FldA=1, Fld2=3}
Binary String (Available only in the Data Structure blocks and is being deprecated.)	4'b100 (string for the Verilog format)
Array	{1.0, 2.0} or {{1.0,2.0},{3.0,4.0}}
Matrix	[1, 2; 3, 4]
Complex	4 + 2j
Fixed Point	fix(.37665, 6, 2)
Embedded Data Structure	Data_Structure "Processor_DS" or Data_Struct "C:.VisualSim.VS_AR.VisualSim.data.Processor_DS"


18.4 Port Typing

The “**Type System**” in VisualSim follows a hierarchical pattern that determines the automatic casting in an expression. All block ports are polymorphic, meaning that their type is defined at run-time based on the arriving data token. The default polymorphic setting for the port is 'unknown' or 'general'.

Some blocks have preset port types for the input and output ports. These types cannot be modified by the user. The ports connected to these ports must be modified. The data type of the ports connected to these preset port must match the preset type. To change the port data type, right-click on the block and select “**Configure Ports**” in the context menu of the block. Common ports requiring this modification includes the “**priority**” ports of the **TimedQueue** and the “**input**” ports of the **TimeDataPlotter** blocks.

18.5 Data Structure Template Location

Text-based Data Structure can be located anywhere in the File System that can be accessed by VisualSim. If the txt file is located in **<VS Home>/VisualSim/data**, else the path must be provided. Java class definition of Data Structure must always be located in the **<VS Home>/VisualSim/data** directory.

 Note	<p>The data structures shipped with VisualSim are either located in the <VS Home>/VisualSim/data directory or in the directory containing the model.</p>
--	---

18.6 Data Structure Definitions and Example

There are three ways of constructing a Data Structure definition:

- Text or CSV format file Used for all model construction
- Traffic Block Window
- Java class file Used only when the model needs to be embedded in a document and displayed using VisualSim Explorer

18.6.1 Text Example

File Name: Stop_n_Wait.txt

Rules: Each row is a field. Spaces are required between columns. The line must end with a semi-colon. The advantage of the text version of the Data Structure is that it can be dynamically modified and used without recompiling.

// Name	Type	Value	Comment
Uniform_Rand_Length	int	1 ;	/* Field Comment */
Uniform_Rand_Noise	int	2 ;	/* Field Comment */
Channel	int	3 ;	/* Field Comment */
Packet_Bytes	int	4 ;	/* Field Comment */
Time_Stamp	double	5.0 ;	/* Field Comment */
Packet	Data_Struct	"Processor_DS" ;	/* Field Comment */

18.6.2 Java Example

File: Stop_n_Wait.java-

Rule: Data Structure fields are concatenated like a string.

//	Type	Name	Value	Comment
private String		Transaction_Name	= "App_0" ;	/** Transaction Name (IORead, etc.) */
private int		Transaction_Bytes	= 0 ;	/** Transaction Size in Bytes */
private String		Source_Name	= "P0" ;	/** Source Name, used in routing */
private int		Source_ID	= 1 ;	/** corresponds to Processor ID */
private String		Destination_Name	= "Bus" ;	/* Destination Name, used in routing */
private int		Destination_ID	= 1 ;	/* Destination Processor ID */
private String		DMA_Channel_Name	= "DMA_Channel" ;	/* DMA Channel Name */
private int		DMA_Channel_ID	= 1 ;	/* DMA Channel ID */

**Note**

The last line must end with a ";" outside the "", as this indicates the end of the string.

Save this file in the \$VS/VisualSim/data directory only.

To compile, use javac in the Java JDK bin folder

18.6.3 Finding the Data Structure Template

The blocks first look for a class definition in the VisualSim/data directory and then a text file version of the Data Structure. It accepts the first file with the matching name of the Data Structure that it finds in the CLASSPATH. The CLASSPATH is defined in the VisualSim.bat/sh file.

18.7 Path Definition

There are three ways to define the path to the Data Structure definition.

1. **Data_Structure_FileName** (Definition is in VisualSim/data directory of the install)
2. **User_Library.Data_Structure_FileName** (Definition is in <VS Home>)
3. **C:.\VisualSim.Data_Structure_FileName** (External to VisualSim- Windows)

or

User.VisualSim.Data_Structure_FileName (External to VisualSim- UNIX)

The Data Structure definition location is required for the following blocks:

- Traffic
- TriggeredTraffic
- VariableList- Initial Value
- Script Block
- ExpressionList

- RegEx function- newToken

18.8 Construction

The Data Structures are generated by the **Source** blocks (**Traffic**, **TriggeredTraffic**, **Transaction_Sequence**, and **Script**).



Note

It is recommend to define all the data structures in a single location. New fields can be created in the ExpressionList and Script blocks.

The sequence of events is as follows:

1. Create a Data Structure template as a txt or a Java file.
2. Enter the name and, optional path, in the traffic generator block.
3. Customize field values to create scenarios.
4. Use the values to make decisions or conduct operations in the model.

18.8.1 Compiling Java Data Structure

To compile the java file, run "javac VisualSim\data\MyDS.java" from the root of the VisualSim install. If javac is not recognized, make sure that the jdk/bin directory is included in the PATH.

19 Processor_DS

19.1 Introduction

The Processor_DS is the Data Structure Template used by the Hardware Modeling blocks. The following are the fields.

Field Name	Type	Value	Comment
A_Address_Min	int	1	Can store Address. This is not being used by any IP block.
A_Address_Max	int	100	Can store Address. Used in the Memory Controller for the Bank Number.
A_Addr_Ctrl_Flag	Boolean	true	Address or Control Flag; Used to distinguish between Read and Write in the Memory Controller. True is read.
A_Branch	Boolean	false	Instruction Branch; Used in the processor block to determine whether the branch has been taken or not.
A_Bytes	int	8	Data size in Bytes. This is the total size of the transaction. Used in all the IP blocks for the size of the transaction.
A_Bytes_Remaining	int	4	Remaining data in Bytes when transaction is fragmented.
A_Bytes_Sent	int	4	Transaction data size in Bytes for this fragment.
A_Command	String	Read	Commands are typically Read, Write,

Field Name	Type	Value	Comment
			Prefetch, and so on. The user can put any value in it as described for the customer blocks.
A_Data	String	MyData	User Data. This is not being used by Ip block currently.
A_First_Word	boolean	true	First word for a transaction. This is used internally in bus and memory blocks. The Bus sets this flag for the first word when it sends it to the Cache/DRAM blocks. It is used in the HW_DRAM to determine whether the word is the first or not.
A_Instruction	array	{"ADD","ADD"}	Instructions. This is the list of instructions for the Processor to execute. It is also the instruction used to identify the matching task in the DMA Database.
A_Instruction_Reorder	array	{1,1}	Enable or disable out-of-order execution. This determines how many newer instructions can execute before the current one must execute. The possible values are 0 and 1 where 1 means everything must execute in order and 0 means that anyone can go ahead. There must be a one-to-one correspondence between this and the A_Instruction. Additional values of 23... are possible. 2 indicates that next two instructions can

Field Name	Type	Value	Comment
			execute before the Processor has to wait for the current instruction to execute.
A_Interrupt	Boolean	false	Interrupt flag for DMA requests and Prefetch. Set by Processor or cache block; Decision made on what to return at the cache and DRAM blocks; Sets it to true when we need to get only one word back.
A_Prefetch	boolean	false	Prefetch Flag. Same as A_Interrupt but the request is for a whole line as opposed to a word. Used between the processor and cache; and cache and DRAM.
A_IDX	int	0	Index number of the current Instruction in the A_Instruction array.
A_IDY	int	0	Last index of a multi-instruction access.
A_Priority	int	0	Transaction Priority
A_Proc_Return	int	-1	Processor Return ID and used internally for decisions
A_Return	int	-1	Return ID
A_Protocol_State	String	MyState	Protocol State -- FSM Map. Not used.
A_Task_Flag	Boolean	false	Indicates a required return for a Write transaction

Field Name	Type	Value	Comment
A_Task_Name	String	Name	Unique Task Name
A_Task_ID	long	0	Unique Task ID
A_Task_Address	int	1	Unique Task Address
A_Task_Source	String	Src	Transaction Source
A_Source	String	Src	Transaction Source
A_Hop	String	Hop	Next Intermediate Device name
A_Status	String	Status	Routing Status
A_Destination	String	Dest	Transaction Destination
A_Time	Double	0.0	Internal Timestamp
A_Variables	Int	16	Number of Software Variables

19.2 Usage of Data Structure fields in the Model

A_Address_Min – It holds the starting bus or memory address.

A_Address_Max – It holds the ending bus or memory address.

A_Address_Control_Flag - Used internally by the Linear, PCI, and AHB buses.

A_Branch - Instruction Branch, used internally by the processor when an instruction arrives and the branch needs to be taken. If "true", the processor pipeline is flushed.

A_Bytes - Total Number of Bytes in a transaction. This is typically the number of bytes requested from the Slave.

A_Bytes_Remaining - When partial transfers are made, the bytes remaining to be transferred are maintained in this field. This is used by the Bus to know if all the transfers are

complete for a Write/Read. The Slave looks for the **A_Bytes_Remaining=0** to know that the transfer is complete.

A_Bytes_Sent - Actual number of bytes transferred in the current transaction. This is used for partial data transfer. For a Bus, this is equal to the burst size.

A_Command – It holds the Request type. The standard ones are Read, Write, Prefetch, and Erase. Others can be added by the user as required. Read, Write, and Prefetch are special keywords that are understood by the Bus and Memory for processing.

A_Data - Contains the user data.

A_First_Word - This is enabled or true for the first transaction in a multi-transfer sequence. All other transfers in this sequence have false.

A_Instruction - An array of instructions that need to be executed on the Processor. The instruction names in this field must match the list in the Instruction Set of the target processor. The Load/Store instruction does not contain the “#” in this field. The # is annotated on the Instruction_Set lookup.

A_Instruction_Reorder - An array corresponding to the list of instructions. The default of all "1"s means that all the instructions are executed sequentially. All "0" allows complete out-of-order execution. When an instruction completes, it sets the corresponding value to "0". If the value is "2", it means that two instructions before must have completed before this current one can execute. You can have any combinations of 0, 1,2,.....

A_Interrupt - This is linked to the A_Prefetch. If A_Prefetch is set to "true" and A_Interrupt" is set to false, this is the very first prefetch for this task. If A_Prefetch and A_Interrupt are true, it is an ongoing prefetch. For the DMA, this operates without the A_Prefetch flag. It is a good practice not to change these fields.

A_Prefetch - If A_Prefetch is set to "true" and A_Interrupt" is set to false, then it is the very first prefetch for this task. If A_Prefetch and A_Interrupt are true, it is an ongoing prefetch. It is a good practice not to change these fields. This is set to false for cache misses and retrieving one word.

A_IDX - Current instruction index in the A_Instruction array.

A_IDY – This is used for managing multiple instruction dispatch per cycle. Specifies the last instruction index is the set that has been dispatched for the current cycle.

A_Priority - Priority of the current transaction. It is used for queue reordering and bus preemption.

A_Proc_Return - This specifies a return ID when the processor sends the request to a bus, DMA, slave or any other device. When the user goes to a “task”, this specifies where to return it. This is used by the Processor and DMA block.

A_Return - This is an index to the Pipeline on return. This tells which stage of the pipeline this task is returning too. The user should not modify this. A positive number indicates it is waiting and a negative number means it is ignored.

A_Protocol_State - This is used for the pipeline and is used internally by the processor and Linear Bus.

A_Task_Flag - This is used for the pipeline and is used internally by the processor and Linear Bus.

A_Task_Address - This is used for the pipeline and is used internally by the processor and Linear Bus.

A_Task_Source - This is used by the Bus to keep track of intermediate information. Do not change.

A_Task_Name - Unique Processor Task Name. This is an identifier at the Processor on which task is executing. This is used by the DMA to determine the sequence of operations to be performed based on a match of the Task Name and the instruction Name.

A_Task_ID - Unique Processor Task ID and each task coming into the processor should have a unique number for multiple task execution on the processor.

A_Source - Transmitting block name. If the processing is sending a read request to the Slave, the Processor name is the Source. On the return, the Slave name is the Source. Used for routing on the Bus

A_Hop - Used for routing across the Bus. This is used to determine what the intermediate node is in the transfer between devices.

A_Status - Routing Status and is maintained with the Bus Arbiter. This is not a user-editable field

A_Destination – This is used to determine where to send this data structure next. It could be Processor, bus, dma, memory or any other hardware device Used for Routing, destination where the request has to be sent.

A_Time - Internal Timestamp

A_Variables - Number of Software Variables. This determines the hit or miss at the Registers and D_Cache.

19.3 Processor_DS Example

```

OUTPUT AT TIME          ----- 0.10 ns -----
{A_Addr_Ctrl_Flag      = true,
A_Address_Max          = 100,
A_Address_Min          = 1,
A_Branch               = false,
A_Bytes                = 8,
A_Bytes_Remaining      = 4,
A_Bytes_Sent           = 4,
A_Command              = "Read",
A_Data                 = "MyData",
A_Destination          = "Dest",
A_First_Word           = true,
A_Hop                  = "Hop",

```


```
A_IDX          = 0,
A_IDY          = 0,
A_Instruction  = {"ADD", "ADD"},
A_Instruction_Reorder= {1},
A_Interrupt    = false,
A_Prefetch     = false,
A_Priority     = 0,
A_Proc_Return  = -1,
A_Protocol_State = "MyState",
A_Return       = -1,
A_Source       = "Src",
A_Status       = "Status",
A_Task_Address = 1,
A_Task_Flag    = false,
A_Task_ID      = 0L,
A_Task_Name    = "Name",
A_Task_Source  = "Src",
A_Time         = 0.0,
A_Variables    = 16,
BLOCK          = "Trans_Src",
DELTA          = 0.0,
DS_NAME        = "Processor_DS",
ID             = 1,
```

INDEX = 0,
TIME = 1.0E-10}

20 Parameters


20.1 Introduction

Parameters are constants defined in the model window or a block. Parameters are constants and do not change during a simulation. Parameters are evaluated at the start of an execution and the value is maintained until the end of the simulation. Each block has a defined set of parameters that are associated with the operation of the block. The users can add parameters to both model windows and blocks. Parameters define attributes such as the processor speed, queue depth or simulation time, or run-time conditions such as Traffic_ON.

 Seed	Parameters are used to specify attributes such as the processor speed, queue depth or simulation time, or run-time conditions such Traffic_ON.
--	--

20.2 Parameter Values

The values of the parameters can be scalar, strings, file names, colors, expressions, and functions. All data types are supported in the parameters.

 Types	Strings must be enclosed in "Quote" marks. Integers should not have decimal points. Doubles should have decimal points. Longs should have "L" appended at end of the number. Booleans should be lowercase 'true' or 'false'.
---	--

Expression in parameters can be an arithmetic or logical operation. The parameter expressions can contain values from other parameters.

Type	Example
String	"Queue1" "file://C:/VisualSim/filename.txt"

Type	Example
Integer	1
Double	1.0
Long	123L
Boolean	True
Array	{1,2,3}
Matrix	[1,2;3,4] Note: Can contain any data type
Expression	(Parameter1==4)?Parameter2:Parameter4
Data Structure	{first=1,second="name"}

20.3 Creation

To add a new model parameter:

1. Drag-n-Drop the block from the Library Folder **Model Setup >Parameter** ('parameter=') into an open Block Diagram Editor window.
2. Right-click to select **Customize Name** of the parameter and enter a name. A new parameter name must be unique, else the BDE will generate an exception.
3. Double click the new parameter name to set the value of the parameter.

For a block, double click on the block and select **Add**. Enter the parameter name and value.

20.4 Using Parameters

Parameters can be on the Right-Hand Side of an expression and as a block parameter value.

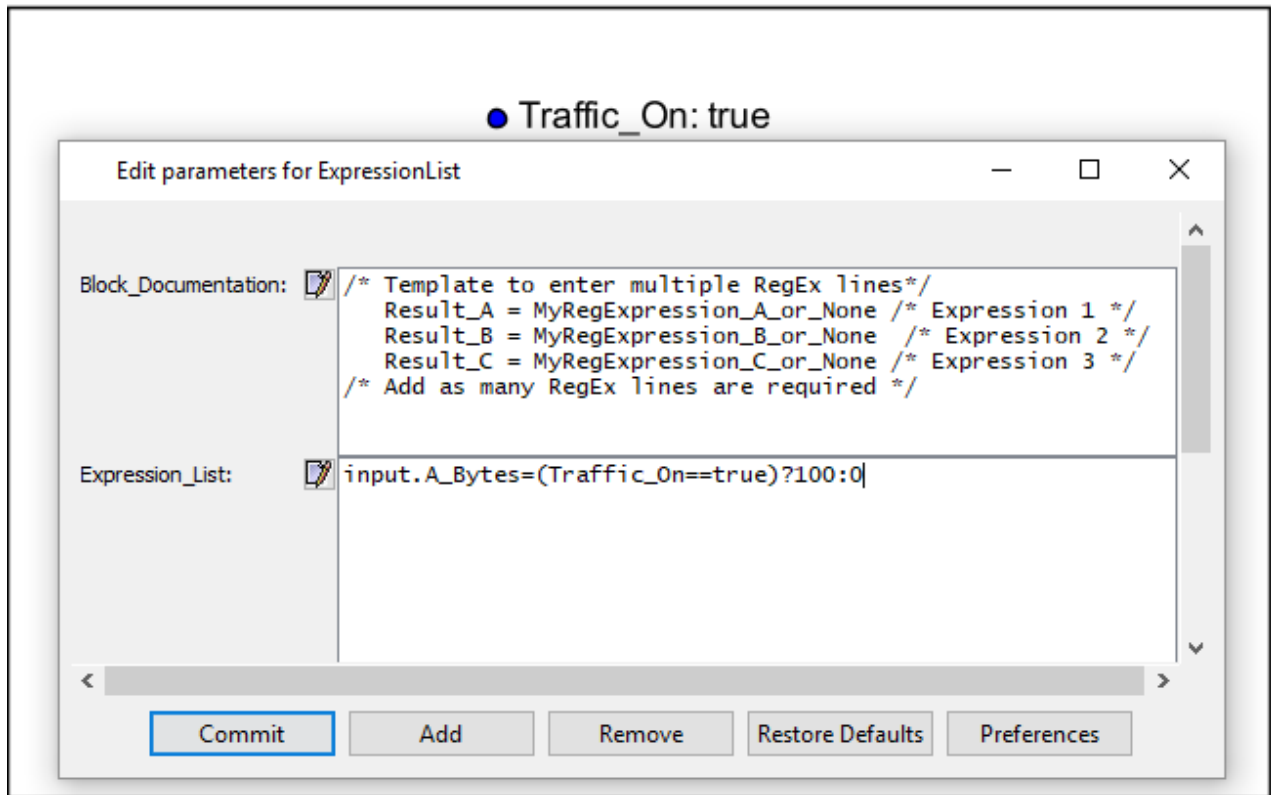


Figure 59. Using Parameters in Expressions

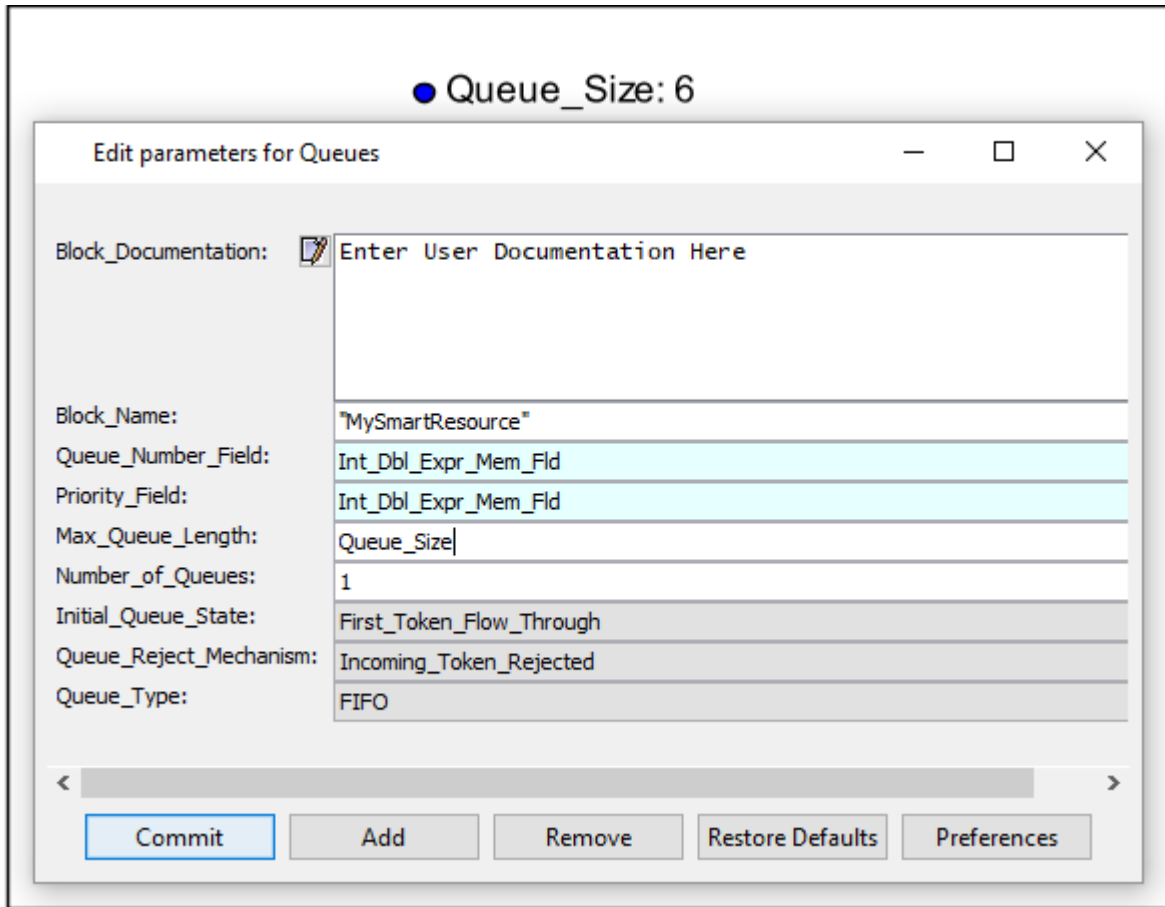


Figure 60. Using Parameters to set Block attributes

Parameters can be concatenated with strings to form the Destination Name for Virtual Connections and the file names for file access blocks.

Parameters of a block at the top-level of the model, parameters of a hierarchical block or parameters of a block within a hierarchical block can be accessed from any other block or parameter. The format is as follows:

MyBlock::MyBlock_Param

Example: Server::Number_of_Queues


Where Server is the block name and Number_of_Queues is the parameter name. Now, if you have to access a parameter from a Hierarchical block, you provide the complete path containing all the intermediate Hierarchical block starting from the top-level.

My_HBlock::My_HBlock2::BlockName::Low_Level_Param

The BlockName will be the name appearing above the block. Parameters in a hierarchical block that are not linked to top-level parameters and parameters of a block cannot be accessed from another hierarchical level. The value of the parameter in hierarchy or parameter of a block can be accessed from the batch-mode simulation using the following format:


Hierarchical block: <window1_name.window2_name.Parameter_name>

Block: <Window1_name.block_name.Parameter_name>

 Batch-Mode	<p>When defining parameter values for the batch-mode simulation, the “ of a string value must be followed by a \”. For example, a value of “MyName” must be defined as “\”MyName\”.</p>
--	---

20.5 Linking Parameters Up/ Down the Model Hierarchy

The value of a parameter can be set in the parameter or can reference a parameter name in the block that this parameter is contained. This can be block parameter that refers to a parameter in the window or a parameter window reference a parameter in the window that contains this block.

 Value Flow	<p>Values of parameters flow top-down and never bottom-up.</p>
--	--

Blocks can link to top level system model parameters by entering the name of the top level parameter in the Block parameters. In the case below, the top level parameter Processor_Speed' is passed to 'Hierarchical_Block' ARM_Speed' (Value 133.0).

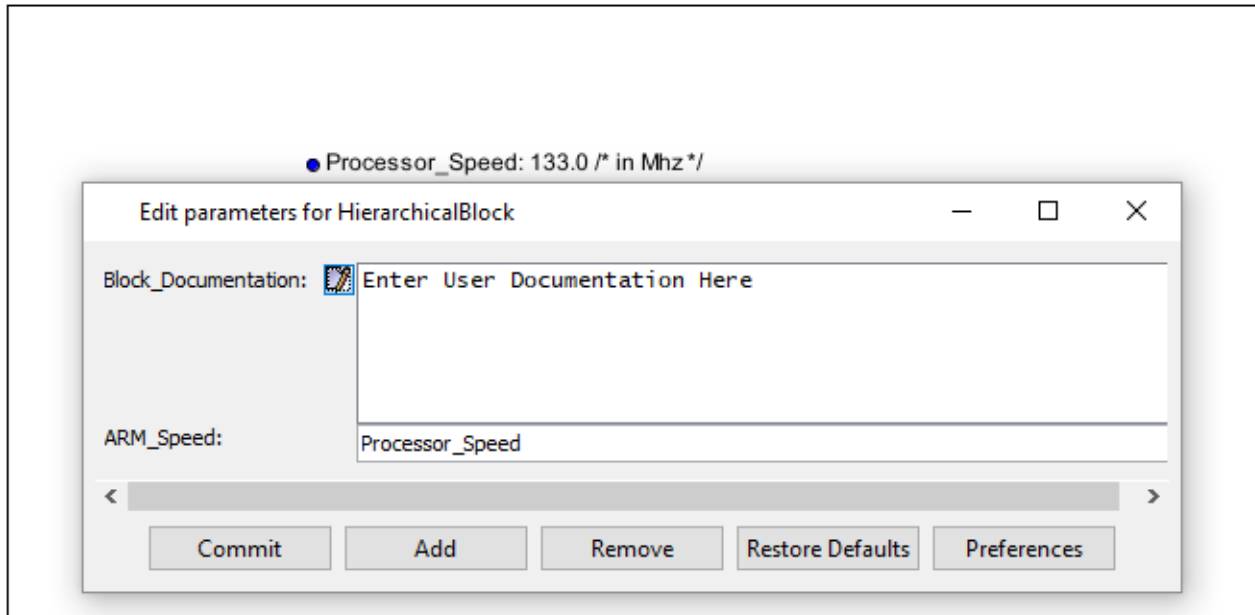


Figure 61. Linking Parameters

20.6 Parameters as Variables

Parameters are constants and, as such, are evaluated at the start of the execution and remain the same until the end of the simulation. SetVariable block and PortParameter can modify the value of a parameter during the simulation. The modified value is recognized by the algorithmic blocks, Expression and, interactive display block. Traffic, Resources, Hardware, and Behavior blocks do not recognize the modified value.

20.7 Shared Parameters

Parameters can be defined at one-level of the hierarchy and reused many levels below in the hierarchy. A parameter at a lower-hierarchy can link to the top-level parameter and get the top-level, provided there is no other parameter that matches the name in the hierarchy between the two-levels. A special case of the shared parameter is the stopTime of the Digital simulator. The user can set value at the top-level and all Digital simulators in the model adopt this value. There is also a standard parameter in the folder called SharedParameter.

20.8 Special Parameters

The “Parameter=” is the most-commonly used parameter. There are other parameter types such as FileParameter (with a browse button), StringParameter (no double-quotes required), and ColorParameter. The PortParameter creates a port and a parameter with the same name. When a new value arrives at the port, the parameter takes on this value.

20.9 Parameter Value on the Icon

The Appearance > Edit Custom Icon has ParameterValue to display the value of a parameter on the block icon. The ParameterExpression can be used to combine values of multiple Parameters in an expression and the resulting value is displayed.

It is also possible to modify the color of the icon dynamically during the simulation. The fillColor parameter of the icon building attributes can be a transitional-if statement ($x==y?red:(x==z)?blue:black$). When the SetVariable block modifies the parameter value of x, the icon color is modified.

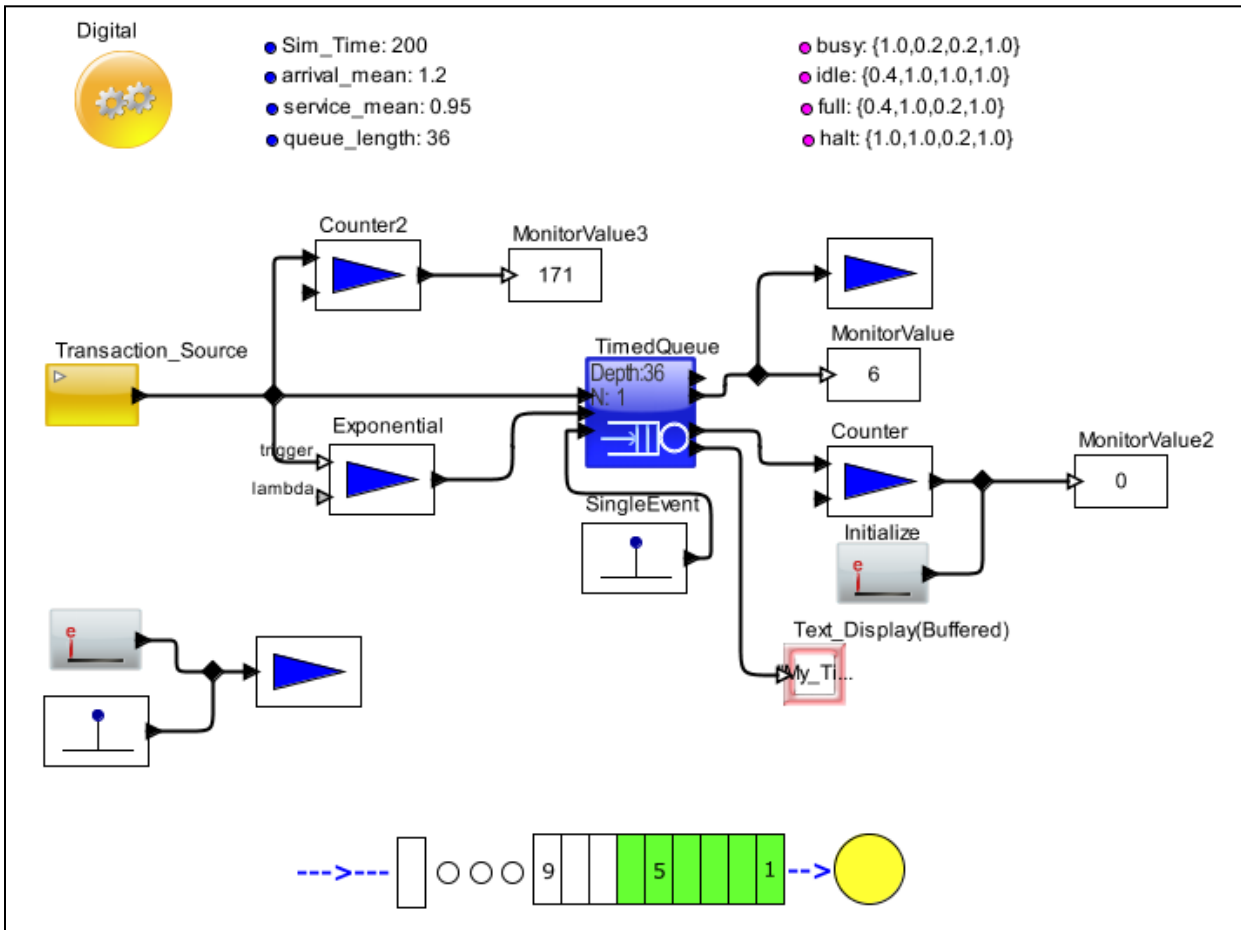


Figure 62. Using Parameters to set the Icon color

In the example, the colors are identified by a type - idle, busy, full or halt. As the queue size changes, the icons on the lower part of the screen change color based on the new value of the Queue length.

21 Configuring Ports and Making Connections

21.1 Introduction

The Configure Ports dialog supports adding, removing, and changing key properties of ports of an entity. It displays the ports of an actor in tabular form with each row representing a port and each column a particular property of a port. An example is shown below:

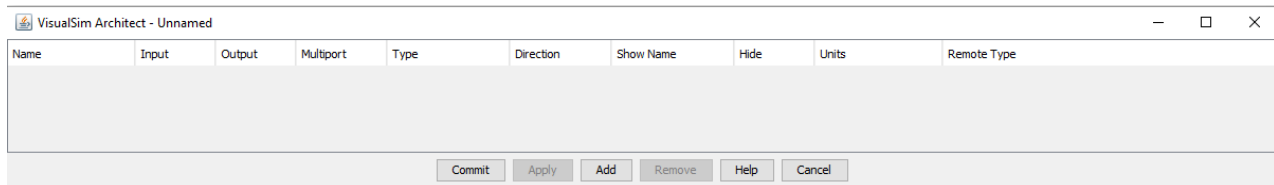


Figure 63. Configure ports for the block

To configure the ports, right click the block and select **Customize > Ports**. Editing a cell does not immediately cause the corresponding port property to be changed. Click the **Apply** button to modify the port properties. Click **Commit** to dismiss after any table modifications are applied. Clicking **Cancel** causes any pending table modifications to be discarded and the dialog dismissed.

21.2 Editing

For the most part, editing the port properties is straight forward. Just click in the cell to be edited and an obvious interaction ensues. Some properties may not be editable because they are part of a class definition, so immutable. These cells have a red background and ignore any attempts at editing as shown below.

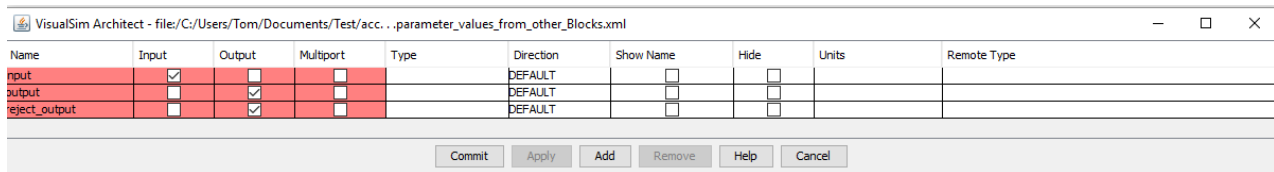


Figure 64. Ports that cannot be edited

Name - Names must not contain a period, must not be blank, and must be unique.

Input, Output, Multiport - Checkboxes that determines if a port is input, output, or both.

Type - The type can be given by any expression that can be evaluated (this expression is called a "prototype"). For example, you can specify the type to be double by giving the string "0.0" (or any other number with a decimal point). However, this does not look very good as a designator for a type. The VisualSim expression language defines the constant "double" to equal "0.0". Thus, the preferred way to specify that a port has type double is to give its type as "double".

The primitive types include:

- Data Structure
- boolean
- complex
- double
- fixedpoint
- general
- int
- long
- matrix
- object
- scalar

- string
- unknown

The constant "unknown" has a rather special behavior, in that it sets the type of the port to be unknown, allowing type resolution to infer it. The constant "matrix" designates a matrix without specifying an element type, in contrast to, for example, "[double]", which specifies a double matrix (see below). Similarly, the constant "scalar" designates a scalar of any type (double, int, long, and so on.). The constant "general" designates any type.

As the type is given by a "prototype", any data type that can be given in an expression can be specified as a type. For structured types, follow the same syntax as in expressions. For example:

```
{double} - double array
[int]     - int matrix
{field1 = string, field2 = int} - For Data Structure
```

Direction - The Cardinal Direction determines which side of the icon the port is located on. Clicking in this cell brings up a menu that provides the means to select a specific side, that is NORTH, EAST, SOUTH, and WEST. DEFAULT can also be selected. Below are the defaults:

- Input ports are usually on the West side.
- Output ports are usually on the East side.
- Ports that are both an input and an output are located on the South side.

Show Name – Enabling this option causes the name of the port to be displayed. Disabling removes the name from the display.

Hide - Enabling this option causes the port name to be hidden.

Units - The units specification for the port. This column is not currently being used.

Remote Types- This column is used to define the data types on the remote system or application. This is used to define the data types for the Verilog and SystemC_Cosim only.

This is a string field and must be fully contained within “”. The content in this column text depends on the type of block and the interface.

21.3 Adding a port

To add a port, click **Add** in Figure 6364. This adds a new row with either default, or unspecified cells. Edit the cells as required for the new port.

21.4 Removing ports

Select the row that contains the port to be removed. On a Windows platform, selecting a row is accomplished with a right-mouse click in the row. On a Mac platform, selecting a row is accomplished with a command-click in the row. When a row is selected, the name of the port is displayed in the Remove button. Click Remove to remove the port from the table.

21.5 Polymorphic Port Types

Most VisualSim blocks can accept several token types on an input port to trigger normal operation. Blocks have polymorphic input and output ports to allow the user more flexibility in implementing their design. While most of the time the queue data tokens are Data Structures, there may be instances where Int Token(s), or Double Token(s) are more appropriate. For example, the Switch_Trigger Block can accept any data token on the input, output, or 'control' port.

The 'control' port does not care what data token enters. It is just used to control the flow of tokens from the input to output, based on the Switch_Trigger menu attribute setting (See Processing/Switching folder):

`Input_First_Next_Control`

`Control_First_Next_Input`

`Input_or_Control_First`

Polymorphic port types reduce the number of library blocks needed by approximately fifty to sixty percent, while maintaining the same functionality, and a high level of simulation performance.

To understand the polymorphism system, run the model on the Type System Usage Page.

21.6 Ports

There are six different types of ports. For more details on Ports, refer to the section on Configuring Ports later in this Chapter.

- ⇒ The six ports are Input, Output, Multiport Input, Multiport Output, Input/Output, and Multiport Input/Output.
- ⇒ Single Input and Output ports can be selected from the toolbar. The remaining must be selected from the Menu.
- ⇒ Single ports are solid and Multiports are hollow.
- ⇒ View details below on Configuring Ports.
- ⇒ Configure external ports from Background Context Menu > Configure Ports.


21.7 Relation and Link

Links are the wires between various blocks in the diagram. The relation is the Blue Diamond that enables broadcast from a single port. The links simply transfer data structures and objects from one port to another. There are no attributes and parameters associated with links and relations.

- ⇒ External ports and relations can be created from the toolbar. View details below on Configuring Ports.
- ⇒ Control-click to create new relations. The relation provides the ability to connect multiple links to a single input. Alternatively you can click the Black Diamond in the standard toolbar.

- ⇒ Drag connections from one port to another. Control-drag to create a connection starting at a relation or an external port.
- ⇒ To broadcast a value from a single port, connect to a diamond relation.

21.8 Point-to-Point Block Connections

After drag-n-dropping several Blocks into the Block Diagram Editor, including hierarchical Blocks, it is easy to inter-connect the Blocks together. For a simple output port to single input port connections, one just drags from either the input, or output port, to the other port. If an output port must go to more than one input port, then one must add a "Relation" connection into the Block Diagram Editor by pushing the black diamond ICON  in the top menu bar, and the BDE will add a new relation in the middle of the open window. You then connect each input and output port(s) to the added "Relation". You can also make a connection from a "Relation" to an input or output port, simply by holding-down the "CTRL" key before dragging to the input or output port.

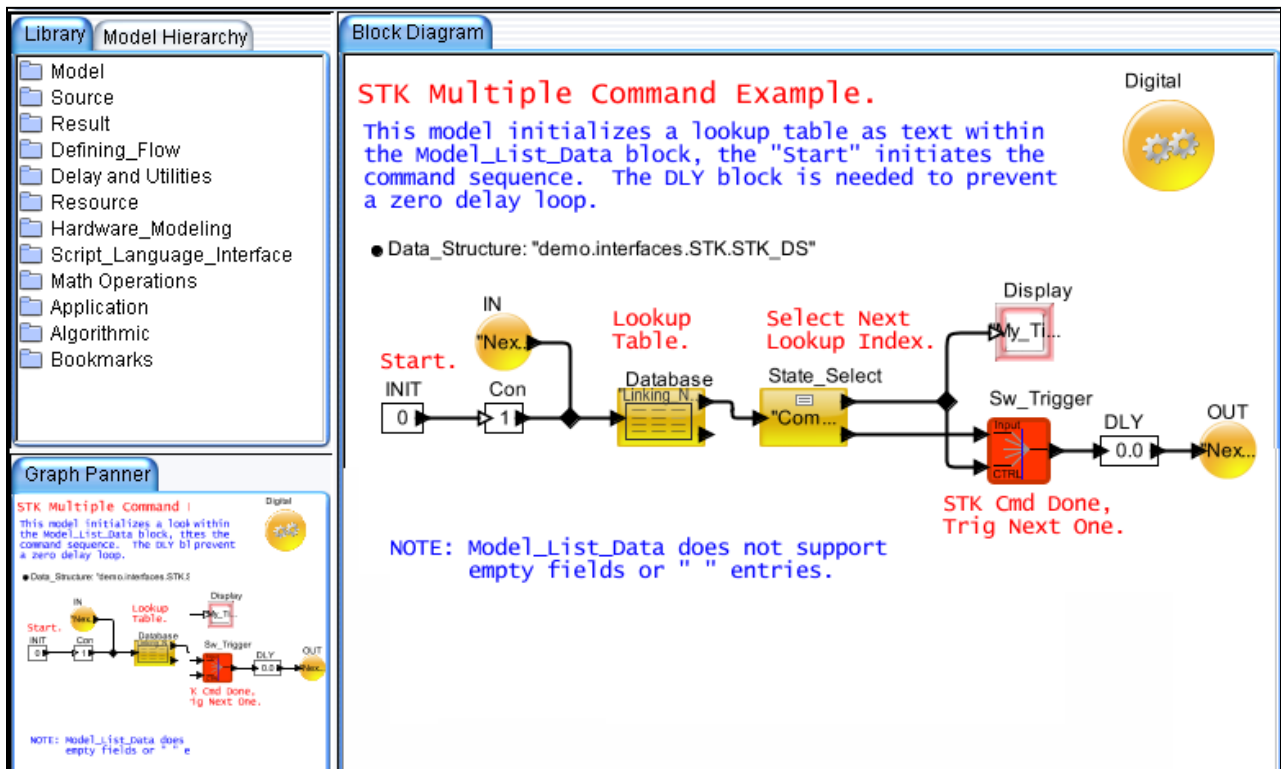


Figure 65. Block-to-block Connections

In terms of Hierarchical blocks, one must first add the input and output ports by right-mouse click "**Open Block**" and then return to the top level to connect the ports. Finally, one can leave non-mandatory input and any output ports "open" and the simulation runs fine.

21.9 Making Connections

To connect the input (black) port to an output (black) port, select the input, hold down the left-button and drag over the output port.

To connect multiple wires, between multiple sets of input and output that meet at a point, a relation (blue diamond) must be used. Connect each input and output port to the relation. It is not sufficient to have the wire go over the Relation. The wires must be connected to the relation.

In a Hierarchical block, you can connect a BDE port to a block port by holding the CTRL button and drawing the wire. Alternately, you can use the normal approach to connect the input/output port of a block to the BDE port.

When you connect a multi-port (white) of a Hierarchical block to another block, you must always connect the output port to the multi-port and then the input port to the multi-port. If this process is not followed, data may not go across the interface.

21.10 Virtual Connections

A unique connection in VisualSim is the ability to communicate between two points in the model without the use of wires. The communication can be between a Script and a IN block or an OUT to an IN block. This communication is done using destination name matching. The destination types can be local (same window) and global (full model).

21.11 Adding Parameters to Links and Ports

An annotated display and tooltip of the ports can be defined by adding a variable called `_showInfo` and `_explanation` respectively to the port. The color and tooltip of the link can be

modified by using `_color` and `_explanation` respectively. To add a parameter, right-click to “Configure”. Click Add to create a parameter.

An explanation of the three parameters is given below.

- ⇒ (Block, Port and Link) The tooltip is done by adding a parameter name `_explanation`, value as a string without “” and the class `VisualSim.kernel.util.StringAttribute`.
- ⇒ (Link only) For the color, you add `_color` giving a color name for the value (string without “”) and then making the class to be `VisualSim.kernel.util.StringAttribute`. The following is the list of color values: black, blue, cyan, darkgray, darkgrey, gray, grey, green, lightgray, lightgrey, magenta, orange, pink, red, white and yellow.
- ⇒ (Port only) A annotation can be displayed on a port by adding a parameter `_showInfo`, value as any data type and the default Class `VisualSim.data.expr.Parameter`.

21.12 Creating Generic Port Icon

Port icons are dynamically created in VisualSim during the block instantiation on the Block Diagram Editor. The icon and color for Input, Output, Input/Output, and none port types are fixed and cannot be modified by the user. For a number of reasons, the user might want to keep the look of the port different from the standard view. A generic icon of rectangular shape and green fill is provided. The port icon looks the same for input, Output, and input/output. Users can modify their port icon to this generic type by doing the following:

1. Drag a block into the BDE.
2. Right-click on the port and select “Configure”.
3. Now click Add.
4. Enter the following information
 - a. Name: `_icon` ; Value: `true`; Class: `VisualSim.kernel.util.StringAttribute`
5. Click OK.
6. Click OK.
7. Now, you see that the port icon has changed to a green rectangle.

You can do the above graphical function by updating the xml file:

```
<port name="input" class="VisualSim.actor.TypedIOPort">  
  <property name="input"/>  
  <property name="_icon" class="VisualSim.kernel.util.StringAttribute" value="true">  
  </property>  
</port>
```

You need to add the property name `_icon` with the associated class and value to each port that needs to be converted to this generic icon.

22 Model Variable

22.1 Introduction

Memories in VisualSim are programming variables or hardware registers or lookup tables. They can contain any data type. Memories can be accessed using Variable blocks, Expression_List, , and Script/Smart_Controller library blocks. Variable are defined as global, local and block in VisualSim. The initialization, access, and data types are identical in all cases.

22.2 Variable Types

- **Global** - Global variable can be defined anywhere in a model using the VariableList block. These Variable locations are visible throughout the model.
- **Local** - Local variable are defined and used in the same block diagram window. They are defined in the VariableList. The main advantage of Local Variable is that multiple instances of a Hierarchical Block can be added to a model without being concerned that the different Hierarchical Block variables interact with each other. Local variables can be accessed from other model locations by using concatenating the model name and all the levels of hierarchy leading to the Variable location. The model name, level, and Variable name are separated by “.”.
- **Block** - This is a special form of Variable that is defined and used entirely within a block. The Script, ExpressionList and Smart_Controller allow the creation of a Block Variable. This can be accessed within a single instance of the respective block. The DS Language-based Statement blocks have a Block Variable called **DSNow** that holds the incoming Data Structure.

22.3 Variable Data Types

Data Type	Example
Int	123
Long	123L
Double	12.3
String	"string"
Boolean	true/false
Binary string	4'b101 (Verilog format)
Data Structures	{field1=1,field2=1.0}
Arrays	myArray(10)

Array values can contain any of the above data types.

22.4 Variable Names

Memories can have any name. Local Variable names in different BDE can have the same names. Local and Global Variable name cannot be the same. Also, Variable names cannot be the same as the Block names for the Hardware Script, Smart_Controller, Queue or SystemResource blocks. You can define a Variable name as a concatenation of three strings or less. These strings can have parameters in them. Once defined, the Variable can be accessed on the LHS and RHS from any block by using the name. If the name is a concatenation of strings, you can create a reference to these memories by using the readVariable or writeVariable RegEx function.

22.5 Initialize Variable

The Variable must be initialized before being used. Global and Local Variable are defined in the VariableList block using the following format.

Format: `Variable_Name Variable_Type Initial_Value`

Examples are:

`Var_name local 1` (Var_name is a local Variable of type int)

`Var_name global 1.0` (Var_name is global Variable of type double)

Initial_Value formats are:

<u>Data Type</u>	<u>Example</u>
Integer	1
Long	1L
Double	1.0
String	Any string
Boolean	TRUE or FALSE
Binary String	4'b101 (This is being deprecated and should not be used.)
Array	{1.0, 2.0}
Array	{10:Processor_DS} (Creates an array of 10 indices with initial value Processor_DS. Processor_DS is a data structure definition in \$VS/VisualSim/data. If the file is not

<u>Data Type</u>	<u>Example</u>
	in this location, this defaults to a string “Processor_DS”. If the Data Structure definition is in a different location, access it as User_Library.Processor_DS or C:.VS_Lib.Proc_DS.) Processor_DS here can also be replaced with any other data type.
Data Structure	Processor_DS or User_Library.Processor_DS or C:.VS_Lib.Proc_DS
Others	Parameters or Variable, which references a value.

Block variables must be defined in the ExpressionList or Script. It is best to define the variable in the top-section of the script for read-ability. In these blocks, the memories can be dynamically created in the code or assignment. If the variable is not initialized but used, it is essential to assign a value that can be statically mapped to a data type. Otherwise an error message is generated.

22.6 Checkers

There are two blocks and a RegEx function to check the content of the variable at any time. The two blocks are the Variable_Monitor and the Variable_Dump. The RegEx is called readAllVariable().

The Variable_Monitor block monitors the local and global variable names listed in the Trace_Name parameter. The block lists the accessing block name, current value, and variable name. The fields called Read_Variable_Name and Write_Variable_Name indicate whether a read or Write has occurred.

The Variable_Dump block outputs the current value in all the global and local variables in the model. For every input trigger of the block, the name and content are output. The output is a data structure with each field representing one of the memories. Global memories are identified by the name while the local memories have the complete hierarchical path plus name. The field names are the memory names while the value is the current content.

The readAllVariable is simply assigned as followings: Value = readAllvariable().

22.7 Accessing Local Variables

Local memories can be accessed within the same hierarchical windows. If you need to access a local variable from another hierarchical block or anywhere else in the model, the following RegEx approach must be utilized.

```
StringName = local_variable + "My_Local_Variable_Name" or
```

```
StringName = (Block_Path + "My_Local_Variable_Name").StringName.read()
```

You can do a similar operation to overwrite the content of this variable by doing the following:

```
StringName = "My_Variable_Name"
```

```
MyVariableToken = StringName.write(Token)
```

Where Token is the new value.

If you would like to access a Block Variable in a Script or Smart Controller, use the following format:

```
StringName = "My_Block_Variable_Name"
```

```
MyVariableToken = StringName.read(Block_Name)
```

Where Block_Name is the name of the Script block. It is not recommended to overwrite the value of the Block Variable from outside the block, as it is very difficult to debug.

22.8 Things to Remember

- Variables must be initialized before being accessed for the first time.
- If the variable has not been initialized before use, the RHS reference to the name is treated as a String while a LHS usage generates an error saying "Cannot write to a string on LHS".
- Variable names are Case-Sensitive.
- Variable names must be Strings and cannot be Parameters.

- A parameter on the LHS generates an exception, as a parameter cannot be changed during a simulation.
- Names of Global and Local variables cannot be the same. Local names can be the same provided they are not in the same BDE.
- The current content in all variable locations can be accessed using the **Variable_Dump** blocks available in Full Library /Model/ Utility/ Checkers library folder. You can also use the RegEx function, `readAllVariables()` to access the list of all the local and global variables in the model with the full path for the local variable. . In addition, users can use RegEx functions to monitor variable, or Script execution for specific simulation times.

22.9 Pointer / Reference to a Variable

In the Script, Smart_Controller and ExpressionList blocks, you can create reference name to a variable (local and global). This capability is important where the name of the variable is composed of multiple strings concatenated together. This is a convenience feature that enables a concatenated name to be used in an expression without using `readVariable` every time. In these blocks,

```
Ref_Var = readVariable("GlobalVariableName") or
```

```
Ref_Var = ("GlobalVariableName").read()
```

is a reference to the `GlobalVariableName` location. If you would like to access the variable in a new variable, use

```
Ref_Var = newToken(readVariable("GlobalVariableName"))
```

Note: If you place the `GlobalVariableName` or the `Ref_Mem` on the LHS of an equation and have an assignment on the RHS, the reference is lost and the two behave like independent variable variables.

For example, this is correct:

```
Ref_Var = readVariable("GlobalVariableName")  
  
Ref_Var.incr()  
  
Other_Variable = Ref_Var + 2
```

This is incorrect and delinks the variable.

```
Ref_Var = readVariable("GlobalVariableName")  
  
Ref_Var = Ref_Var.incr() /* Creates new variable and reference  
is lost */  
  
GlobalVariableName = Ref_Var + 2 /* Delinks original reference  
*/
```

23 File Paths

There are a few file path methods in VisualSim. The following blocks support the URI standard of the Web. For more information on URI, click [here](#).

<u>Plotters:</u>	<u>Text</u>	<u>Content Management</u>
TimeDataPlotter	FileWriterFile Writer	Database
XYPlotter	File Reader	Transaction_Sequence
Histogram	Traffic_Reader	
DS_TimeDataPlotter	TextDisplay	
DS_XYPlotter	TextDisplay	

These blocks follow the following formats:

- File name: The file is in the same directory as the model XML.
- ./File Name: The file is in the same directory as the model XML. This is the Unix format.
- ../File_Location/File name: The file is located in a different directory but in the same disk. This is the Unix format.
- VS (or \$VS) + File Path + File Name: This uses the VisualSim constant string (VS) that represents the install location of VS_AR.
- Absolute Path: This includes the file path + file name from the base of the disk.
- File:/(Absolute Path): This is the URI format. This includes the file path + file name from the base of the disk. An alternate format can also contain ///.
- \$CLASSPATH + File Path + File Name: The CLASSPATH is defined in the batch script (VisualSim.bat for Windows and VisualSim.sh for UNIX). The system searches in all the directories in the CLASSPATH list. For any block that needs to write, the file must exist.
- [http://URL](#): This format is used to find a file that is on a Web Server. This format is to access data files located on remote Web servers. This is format is used when the model must be used when the model is embedded in the html page and is viewed using VisualSim Explorer. This format is only available for reading. Write is not permitted on Web Servers.

24 Modeling Languages

VisualSim offers a number of methods to construct the model. The fastest way is to use the blocks. Blocks are the components, probes and simulators used to assemble a model and instrument the model for generating analysis output. The blocks provide the required modeling concepts required to describe the system, generate traffic, generate statistics, and make decisions. The Resources, Traffic and Statistics Generation are best built using blocks. The behavior, algorithms and arbitration schemes can be described using ExpressionList blocks, Script, or a commercial programming language such as Python, C, C++, SystemC and Verilog. For the ExpressionList blocks and the Script, VisualSim provides an extensive collection of mathematical, logical and custom functions called RegEx.

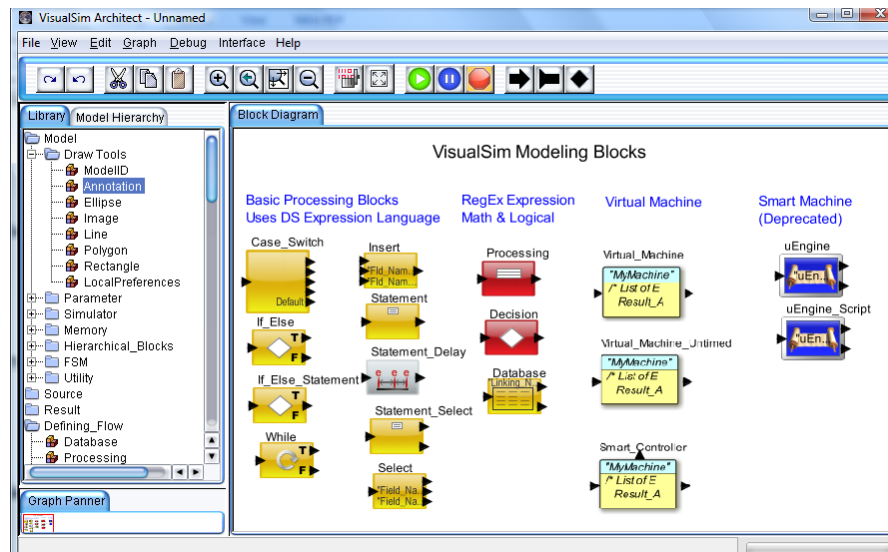


Figure 66. VisualSim Modeling Languages

1. **RegEx Expression:** This is the underlying expression description language in VisualSim engine. The Expression is used in Parameter definitions of all blocks and for the Actions in the FSM. This language contains a large number of functions and methods that are optimized for generating model information and for operating at

extremely high performance. The RegEx can use parameters, variables, and data structure fields. All data types are supported. There are four types of RegEx:

- a. **Operators:** Mathematical, logical, DSP, trigonometric, and imaging functions.
 - b. **Transaction if statement:** $(a > b)?$ value1: value2.
 - c. **Methods:** `getBlockStatus(Queue,"copy",1)`
 - d. **Function:** `array.length()`
2. **Expression Blocks:** The ExpressionList blocks use the RegEx in an Expression containing a RHS and LHS. In this block, the variables and parameters are identified by their name. The data structure is identified by the port on which it arrived. So, the field of the data structure arriving on input1 is `input1.field`. These blocks can have any number of input and output ports. All inputs have to arrive for the block to start executing the lines of expression. All lines of expressions are executed in sequence listed in the block window. The block can send a value, data structure, field, variable or the result of an expression on each port. The ExpressionList block can control whether a value must be sent on an output using the condition. There are no restrictions on the number of values and operands on each expression line.
3. **DS Expression Language:** This language is used in the Basic Processing blocks and are distinguished as the Yellow shaded. This is an easy-to-use subset of the RegEx. There are fixed number of items in an expression line. The block can use the parameters, memories, and data structure fields. The number of input and output ports are fixed. This block is best suited for a casual user. The expression describes Standard, Mathematical, and Logical operations. The operations can be conducted on Scalar Values, that is Integer, Doubles, and Long. There are a number of pre-defined casting provided (no user intervention required) and certain specific function provided (like getting time value, generating distributions and so on). The language does not allow for any extensions, no adding input/output ports and no Array processing (Add, subtract etc.) are allowed in these blocks. The DS Expression has a fixed format namely,

`(X=Y op Z) or ((X logic_op Z) && or || (A logic_op Z)`

4. **Scripting (Script block):** This is a C-like language that is fully integrated with the RegEx. There are three variations of the block - Script can handle timing, Virtual_Machine_Untimed is a high performance untimed block and the Smart_Controller is a subset used in conjunction with the Queue blocks.

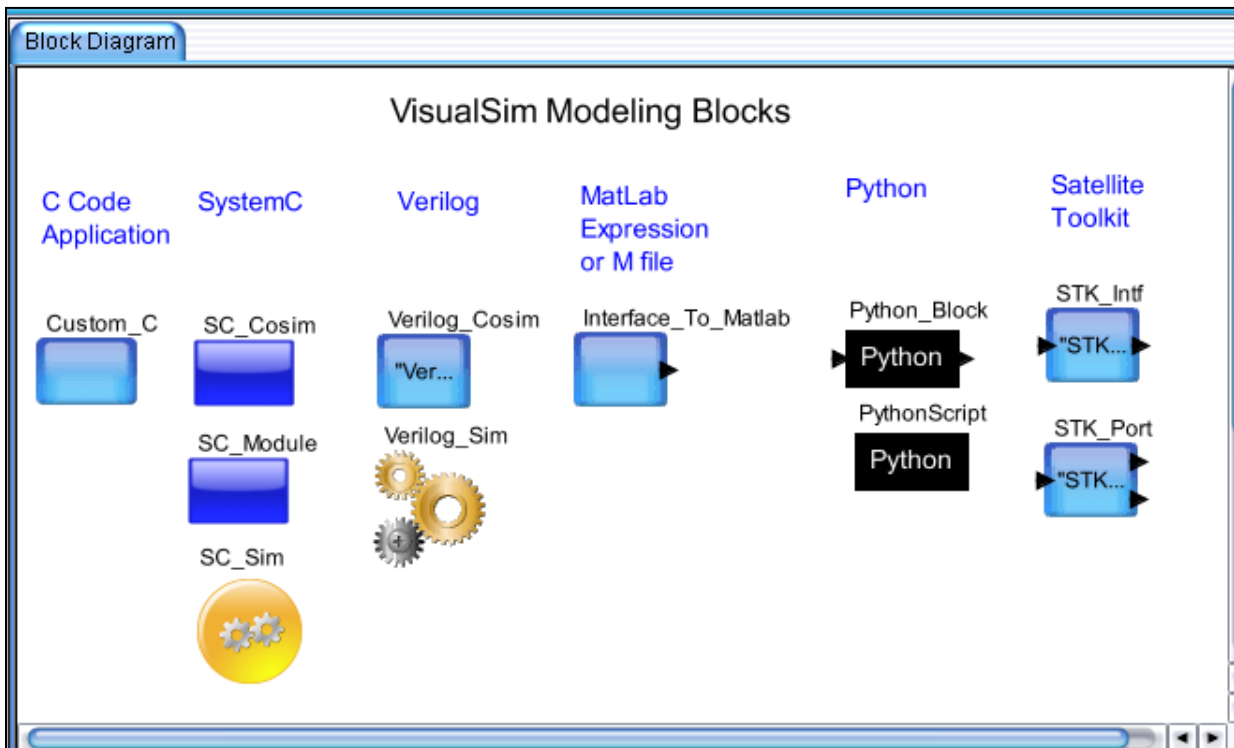


Figure 67. List of Application Interface Blocks

5. **Custom C-Code:** This block allows the user to import C/C++ code that has been constructed to describe a behavior. The block can maintain state information during runs, count cycles, and have multiple input and output ports. The block defines the code source file and the expected input and return values. A wrapper code is generated to integrate this code without modifying the source.

6. **SystemC:** This block allows the integration of SystemC, TLM 1.0, and TLM 2.0 blocks into VisualSim. The block provides a graphical entry to integrate SystemC models and run it in VisualSim. The SystemC simulator is shipped with VisualSim.
7. **Verilog:** This provides a co-simulation with the commercial simulators such as ModelSim. This block generates a VPI2.0 wrapper to integrate the two simulators together. The block synchronizes time across the two simulator.
8. **MatLab:** This block allows the user to dynamically send functions and values to the external simulator and return with a result.
9. **Python:** This block allows the user to create a script and run it as part of a model.

25 Data Structures Expression Language

The Data Structure expression is a simplified expression mechanism and is used by the Statement blocks. These include the:

Statement
If_Else
If_Else_Statement
Statement_Delay,
Statement_Switch
Statement_Select
While
Case_Switch
Insert
Select

The Expression can be of two types - One/Two variable or three variables. The spacing between all variables and between operators is required. If the spacing is not correct between the variable, errors are generated. The two options are just different ways of expressing the same operations. This is along the lines of action statements in C programming.

The format can either be

X = Y op Z

or

X op = Y

The Statement blocks can accept Data Structure Fields, Memories, Parameters, Numerical Values, and String Constants.

The Expression Language provides Arithmetic, Logical/Binary, and Statistical Operators. The use of these different operators is shown in the Example Section below. The following table summarizes them:

Arithmetic	+ , - , * , /
	sqrt (square-root)
	^ (Power)
	% (Modulo)
	! (invert)
Logical	&& (AND)
	(OR)
	== (equals)
	!= (Not equal)
	> (Greater than)
	< (Less than)
Binary	& (AND)
	(OR)
	# (XOR)

	~ (NOT)
	>> (Shift right)
	<< (Shift left)

Statistical	irand (integer random)
	rand (double random)
	Norm (normal distribution)
	exp (exponential distribution)
Combined op + =	++ (Increment)
	--(Decrement)
	+= (add RHS to LHS)
	-= (Sub RHS from LHS)
	= (LHS = LHS RHS)
	/= (LHS=LHS/RHS)
	%= (LHS= LHS Module RHS)
	&= (AND)
	= (OR)
	~= (XOR)

<p>Time Values Can be used on the RHS only</p>	<p>TNow is the current simulation time.</p>
	<p>TLast is the simulation time when the previous Data Structure was at this block.</p>
	<p>TDelta is the difference of TNow minus TLast</p>
	<p>TReal is the current wall clock in msec</p>
	<p>TRealLast is the last wall clock or system time in msec.</p>
	<p>TRealLast is the difference of TReal - TRealLast. Wall clock or system time is useful for benchmarking model performance.</p>

25.1 Format for the Statement Blocks

The format for the Statement blocks is as follows:

Option 1				
LHS: X Field	Assignment	RHS: Y	RHS: Operation	RHS: Z
Can contain a field name of the incoming data structure or variable.	=	Can contain, values, Time, parameter, field name of the incoming data structure or variable.	Arithmetic: +, -, *, /, 1/, %, ^ Logical: & (AND), (OR), ~ (NOT), ! (invert), 'xor' (Exclusive OR) Logical Shift: <<', '<=<', '>>', '>=>'.	Can contain, values, Time, parameter, field name of the incoming data structure or variable.
Data Types supported: Integer, double, Boolean, binary, long.	Space is required on either sides of the “=”.	Data Types supported: Integer, double, Boolean, binary, long.	Space is required on either side of the “operator”.	Data Types supported: Integer, double, Boolean, binary, long.
Notes: 1. Data type casting is from right to left. The “Z” data type is converted to “Y” data type before processing.				

LHS: X Field	Operation + Assignment	RHS: Y
Can contain a field name of	=	Distributions:

LHS: X Field	Operation + Assignment	RHS: Y
the incoming data structure or variable.		irand(lower, upper), rand(lower, upper), exp(mean), norm(mean, std dev).
Can contain a field name of the incoming data structure or variable.	Arithmetic: =, +=, -=, *=, /=, 1/=, %= !, ^, sqrt, ~, &, , xor Logical: '&=', ' =', '~=', 'xor='	Can contain, values, Time, parameter, field name of the incoming data structure or variable.
Data Types supported: Integer, double, Boolean, binary and long.	Space is required on either sides of the “=”.	Data Types supported: Integer, double, Boolean, binary and long.

26 Differences between Script and C Programming

The Script works like a function block in C programming or script. The simple logic expressions use a C/C++ syntax. Following are few differences:

1. The ';' is optional at the end of each line.
2. There must be only one operation per line. This can be an expression, LABEL(), or curly brackets{ }.
3. Declaration are done by Name = value. The data type is polymorphic, meaning that the data type is identified with the first incoming value.
4. Declarations can be anywhere in the code but must be before it is used in an expression on the Left Hand Side (LHS).
5. SWITCH-CASE is all capital.
6. CASE has CASE: LABEL.
7. End of each CASE requires a GTO(LABEL).
8. The last CASE must be CASE: DEFAULT.
9. No pointers are supported and only a reference name for a variable is supported.
10. There must be at least one statement line between { and }.
11. Two { in sequence are not allowed. There must be at least one statement in between.

27 Script Block

This block is used to write scripts and a set of blocks that use a C-like programming format to describe the logic or behaviors. The three supporting blocks are Smart_Controller, Script block, and Virtual_Machine_Untimed. The block can be used anywhere that detailed programming would be more suitable than using multiple blocks. This block can contain all the RegEx functions and contains standard C functions such as if, else-if, else, while, and SWITCH/CASE. RegEx algorithms can be created to perform decoding, loops, blocking waits, non-blocking waits, or execution based on input transactions, or model level variable. Input or Output ports can be added for additional functionality or virtual transactions can be sent, without ports or wires, into or out of the Script block. Event or time-based queues can be declared inside the Script.

The Script block accepts data structures on the input ports, processes a sequence of C-like code, and outputs a data structure. The data structure can arrive at the ports or via virtual connections to the block. All the data structures are placed in a single non-priority input queue in the order of arrival. The data structures are executed in the order of arrival. The executions are requests using SEND to LABEL within the block and events being sent to this block. In the code, the currently executing data structure is named "port_token". The arriving data structure can be associated with an arriving port, SystemResource (return from SystemResource) or "virtual" (virtual connection, and "event" (user event).

The sequence of code can utilize the incoming data structures field, variable (local, global and variable-defined inside this block), RegEx language and parameter values. Using the RegEx functions, this block can send the Data Structures to Virtual Connection, SystemResources and other Script blocks.

To define this code, drag the Script block, Script or Smart_Controller block to the Editor. To access the code, right-click the block and select "**Open Block**". The following are the main differences between the three blocks:

Feature	Script Block	Virtual_Machine_Untimed	Smart_Controller
Time and Events	Yes	No	Yes
Queue	Must be defined	Must be defined	Automatically associated with one queue using available parameter
TIMEQ and Queue	Yes	Only Queue	No
Plotting	Yes	Yes	No
Pop port	No	No	Yes

When the code is entered, make sure you save in the Text Editor and the Block Diagram Editor for your changes to be visible. When simulation is started, the block compiles the code and translates it into machine language. Use Listen to Block to view the compile sequence, to identify errors, and to check execution correctness. The translated code may look different in certain places. For example, the line before LABEL: BEGIN contains a GTO(END) including that all the initialization code is executed without executing the operational code. Other changes include a JIF for if, if-else and else statements; GTO(LABEL) for SWITCH operators and LABEL for CASE.

The block can be self-triggered (Self_Start = true as a block parameter), or contain LABEL: BEGIN (all the lines before it) or triggered by an incoming data structure (either ports or virtual

connection). Both self-triggered and LABEL:BEGIN cannot be used in the same Script block. The self-trigger executes the entire sequence of code at 0.0 time. The LABEL:BEGIN executes all the code until this label at 0.0. The incoming structure executes all the code if LABEL: BEGIN does not exist or start from LABEL: BEGIN if it exists. Both self-triggered and LABEL: BEGIN must not be used, as this duplicates the execute and causes unexpected results.

The code execute in sequence. The code can contain actions, logical operations, and delays. The delays can wait on time or on a required event. To learn more about events, check the section on events in this document. A WAIT in the code creates a blocking operation and prevents any further execution of any data structure until the time/event has elapsed.

Additional ports on the input/output can be added. The structures arriving at the input ports are accumulated in the input queue and executed in the order of arrival. Multiple input ports are useful for a visual view of the connections and for cases where the arrival source must be identified for code execution. Values on all ports do not have to arrive for the code to execute. It takes all the inputs and places them in the input queue, in the order of arrival. The SEND function sends the required values to the output ports, Labels in this code, other Script or virtual connections. SEND also supports a delayed output.

28 RegEx Language

The RegEx is a collection of Mathematical, Logical, Statistical, and Algorithm-Specific Functions. These can be used in scripts and expressions to accelerate model construction and for fast simulation execution. The RegEx functions work with most data types and have a specific format.

28.1 Computation using RegEx

The RegEx can be used in parameter fields to compute the value at the start of the simulation based on other parameters. The RegEx can also be used in the FSM for the actions. In the Script, Smart Controller, Processor, and ExpressionList blocks, RegEx can be used in methods and on the Right Hand Side (RHS) of an equation. The equation can have any number of operators and variables and combine Data Structure Fields, Memories, Values and Parameters. A complex expression can combine the built-in functions in any order, as far as they confirm to the data types. The **Left Hand Side (LHS)** of the equation can only be a **Field** or **Variable**. There are two types of formats:

Scalar and String Data types- Integer, Double and Long

$$X = Y + Z$$

Boolean

$$X = (\text{Boolean function})?Value1:Value2$$

where X is assigned the value1 or value 2 depending on the Boolean function resolving to true and false respectively. Value1 and Value2 can be any expression containing variables, Fields, Parameters, and Values.


Arrays

1. $\text{Array}(i) = \text{Array}(j) - Y + Z$ where Y and Z can reference an Array location, parameters, variables, and values. The data types can be scalar, Boolean or string data types. The indices i and j, must be an integer type and can be a value, variable, parameter or field.

2. $\text{Array}(i)(j) = \text{Array}(i)(j) + Y + Z$. This is a definition for a multi-dimension array. The indices i and j , must be integer and can be a value, variable, parameter or field.


28.2 Casting and Conversions

When an operator involves two distinct types, the expression language has to make a decision about which type to use to implement the operation. If one of the two types can be converted without loss into the other, then it will be. For instance, `int` can be converted losslessly to `double`, so `1.0/2` results in 2 being first converted to 2.0, so the result is 0.5.

 Note	<p>Among the scalar types, <i>unsignedByte</i> can be converted to anything else, <i>int</i> can be converted to <i>double</i>, and <i>double</i> can be converted to <i>complex</i>. Note that <i>long</i> cannot be converted to <i>double</i> without loss, nor vice versa. So, an expression like <code>2.0/2L</code> yields the following error message:</p> <p>Error evaluating expression "<code>2.0/2L</code>"</p> <p>It is because the divide method is not supported between Double '2.0' and Long '2L' as the operation between these types cannot be resolved losslessly.</p>
--	--

All scalar types have *limited precision* and *magnitude*. As a result of this, **Arithmetic Operations** are subject to **underflow** and **overflow**. For **Double Numbers**, **overflow** results in the corresponding **positive** or **negative infinity**. **Underflow** (that is, the precision does not suffice to represent the result) yields **zero**.

For *integer types* and *fixedpoint*, **overflow** results in **wraparound**. For instance, while the value of **MaxInt** is **2147483647**, the expression is "MaxInt + 1 yields -2147483648". Similarly, while **MaxUnsignedByte** has value **255ub**, "MaxUnsignedByte + 1ub" has value **0ub**.

 Note	<p>However the "MaxUnsignedByte + 1" yields 256, which is an int and not an unsignedByte. This is because MaxUnsignedByte can be losslessly converted to an int, so the addition is int addition, not unsignedByte addition. Note that these relational operators check the values when</p>
--	---

possible, irrespective of type.

So, for example,

```
>> 1 == 1.0  
returns true
```

To check for equality of both type and value, use the equals() method, as in

```
>> 1.equals(1.0)  
false
```

28.3 RegEx Functions- Queue and SystemResource; Methods

28.3.1 Mapping Functions to Blocks for getBlockStatus

VisualSim provides a number of special functions for accessing the content of Queues. The following functions are used:

- **getBlockStatus:** This is used to get a variety of information from the block. Below are some usage examples. There are three variations of these functions - 2, 3, and 4 variables. The function returns the value to the LHS after performing certain operations on the selected Queue. The queue number starts from 1 and the positions in each queue also start from 1. Blocks Supported: SystemResource_Extend, SystemResource, Layer_Protocol, Node_Master, Queue, Server, Channel_N, Script, Smart_Controller, DRAM, Processor, Linear Bus, Cache, and DMA.
- **QUEUE:** This is used to define, put, pop, and do processing in a Queue defined entirely with a Script. The queue number starts from 1 and the positions in each queue also start from 1. Blocks Supported: Script
- **TIMEQ:** This is used to define, put, pop time, and do processing in a Timed Queue defined entirely with a Script. The queue number starts from 1 and the positions in each queue also start from 1. Blocks Supported: Script

- **getDeviceStatus:** This function returns the status (either free or currently active) for a specific device. The free means that there is space available in the input Queue.
Blocks Supported: DRAM, Processor, Linear Bus, Cache and DMA
- **getResourceLength:** This functions gets the length of the queue. The queue number start from 1 and the positions in each queue also start from 1.
Blocks Supported: Queue

28.3.2 getBlockStatus Functions

<u>Operation</u>	<u>Explanation</u>
copy	Returns the copy of the data structure at the position.
take	Removes data structure at the position without updating the statistics or placing it on the output port. Note: In the Script block, the QUEUE and TIMEQ methods make these data structures available to the next statement line.
pop	Removes the head of the Queue and places it on the output port. Updates statistics Note: In the Script block, the QUEUE and TIMEQ methods make these data structures available to the next statement line.
stats	Output the statistics for the queue or set of queues. →-(Queue Number) set the statistics and (Queue Number) reset the statistics →For all the Queues, Queue Number= Number Of Queues +1 -(Queue Number)set the stastistics and (QueueNumber) reset the statistics.
length	Current length of the queue.
array	If current length > 0, then true, else false. Position 0 is always false as the Queue number start from 1.
copy.fieldname	Returns the value in the field (fieldname) of all the data structure in the selected Queue

28.3.3 getBlockStatus format and example

x= getBlockStatus("Block_Name", "Queue Name", Type, Queue Number, Position in Queue)

Type is copy, take, pop, stats, length, array and copy.fieldname where fieldname is a name of the field in the Data Structure.

Return values for each type are:

- copy: data structure
- take: data structure. Statistics are not updated for this data structure.
- pop: data structure
- Stats: data structure or array of data structure, if all Queue requested
- Length: integer value
- Array: Boolean array
- copy.fieldname: Array with any data type

Queue Name is only applicable for queues in the Script and Smart Controller.

Queue Number and Position in Queue are only applicable for Queue blocks, Server and Channel_N. First Queue is 1 and the First position in the Queue is 1.

Block/ Function	Function Details
SystemResource_Extend SystemResource	getBlockStatus ("SystemResource Name", "Any value", Type, Any value, Any value) Type can be "length, "copy" and "stats". Does not require Queue number or Position
Queue	getBlockStatus("Queue_Name", "Any value", Type, Queue Number, Position in Queue) Type: copy: Requires Queue Number, Position in Queue take: Requires Queue Number, Position in Queue pop: Requires Queue Number, Position in Queue stats: Requires Queue Number, Position in Queue is ignored length: Requires Queue Number, Position in Queue is ignored array: Does not require Queue number or Position Copy.fieldName: Require Queue number, Position in Queue is ignored
Server	getBlockStatus("Server_Name", "Any value", Type, Queue Number,

Block/ Function	Function Details
	Position in Queue) Type: copy: Requires Queue Number, Position in Queue stats: Requires Queue Number, Position in Queue is ignored length: Requires Queue Number, Position in Queue is ignored array: Does not require Queue number or Position Copy.fieldName: Require Queue number, Position in Queue is ignored
Channel_N	getBlockStatus("Channel_Name", "Any value", Type, Channel Number, Position in Channel) Type: copy: Requires Channel Number, Position in Channel stats: Requires Channel Number, Position in Channel is ignored length: Requires Channel Number, Position in Channel is ignored array: Does not require Channel Number or Position
Layer_Protocol	getBlockStatus("Layer_Protocol_Name", "Any value", Type, Index, Position in Queue) Type: stats: To get statistics, use 1 and for reset use -1 in Index. Position in Queue is ignored length: To get length, Up Queue use 1 and for Down Queue use 2 in Index field. Position in Channel is ignored
Script, Smart_Controller (Input_Queue)	getBlockStatus("Script_Name", "Input_Queue", Type, Any value, Any value) Type: length: Does not require Queue Number or Position in Queue

Any value means that the user enters a value but the value is ignored.

29 Source

User can generate traffic using a standard distribution, sequences, trace files, clocks, and custom distributions.

- **Clock** – Generate all possible clock inputs.
- **Event** – Generate the input according to the Event set.
- **File Import** – Input can be generated according to the file input.
- **Traffic** – Generate input as per the specified DS and time distribution.

29.1 Generating

The **Source** blocks generate the data structures that trigger the model to execute and flows through the model. There are five mechanisms for generating Data Structures in VisualSim.

- In case of using a standard distribution for the time interval between Data Structures, use Traffic.
- If a custom distribution is required or the Data Structure is generated as a function of another activity, or triggered during the flow, use the TriggeredTraffic.
- If the distribution is a specific sequence or the generation rate is a function of time and probability, use the Transaction_Sequence block.
- If a file contains the sequence from an existing system, such as a trace or Network Sniffer or variable activity, then use the Traffic_Reader or File Reader blocks to generate the Data Structure. In this case, the columns of the trace file are the fields and the values in each line form the new Data Structure. The File Reader loads the entire file into computer memory before generating values while the Traffic_Reader reads one line at a time from the file.

30 Result- Analysis and Plotting

Post-Processing is sometimes viewed as a "post" modeling activity. You can use the VisualSim Post Processor to graphically display and analyze performance data collected from the simulation. The Post Processor can organize results into a variety of x-y graphs, bar charts, and scatter plots, and displays them in either graphical or tabular format. The Post Processor can also perform a variety of statistical functions as a mean, min, max, standard deviation, and confidence intervals.

This section focuses on post-processing in terms of what VisualSim can provide in terms of system latency, system throughput, and system utilization. These are the three most common performance modeling statistics to obtain and plot in the post-processor. VisualSim can provide post-processing capability on other system metrics. The approach is similar to the three common metrics.

System Latency -- System latency can be calculated quite easily, because the TIME field in the composite Data Structure contains the time that the Data Structure was created. If one subtracts TIME (creation time) from the current simulation time (TNow), then the difference is the time spent in the system. One might use one of the optional composite Data Structure header fields (DELTA) to record the transaction, or packet latency (DS expression):

```
System_Latency = Sim_Time - Time_Created [DELTA = TNow - TIME]
```

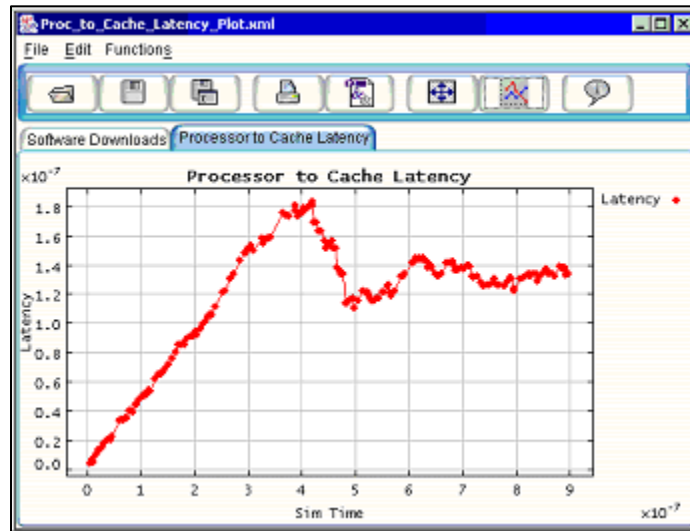


Figure 68. Post Processing Latency

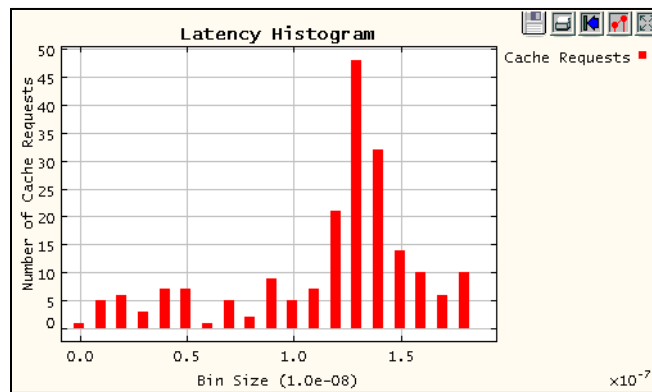


Figure 69. Post Processing Histogram

System Throughput -- System throughput involves accumulating data being sent through a digital model, and at specified time intervals, calculating the Throughput in Bytes per second, KBytes per second, MBytes per second, or Gbytes per second. You need to accumulate the data passing through the system in a variable, or statistical block, and then calculate the system throughput by dividing the amount of data by the time interval in the appropriate units.

$$\text{System_Throughput} = \text{System_Data_Accumulated} / \text{System_Sample_Time}$$

System Utilization -- System utilization is related to system throughput in that is the proportion of system throughput to system capacity:

$$\text{System_Utilization} = (\text{System_Throughput} * 100.0) / \text{System_Capacity}$$

In the case of time-related activities, system utilization may simply be the time the resource is busy divided by the total time:

$$\text{System_Utilization} = (\text{System_Time_Busy} * 100.0) / \text{System_Sample_Time}$$

System Throughput and *System Utilization* can be plotted similar to System Latency, using a **TimeDataPlotter** or **HistogramPlotter** block, because they are both single valued metrics. There are variations of the TimeDataPlotter including XYPlotter, DS_TimeDataPlotter, and DS_XYPlotter. The prefix DS_ allows the user to control the visual effects and attributes of the plot dataset.

30.1.1 TimeDataPlotter Block Output

The following figure shows the TimeDataPlotter Block output in Simulation Cockpit.

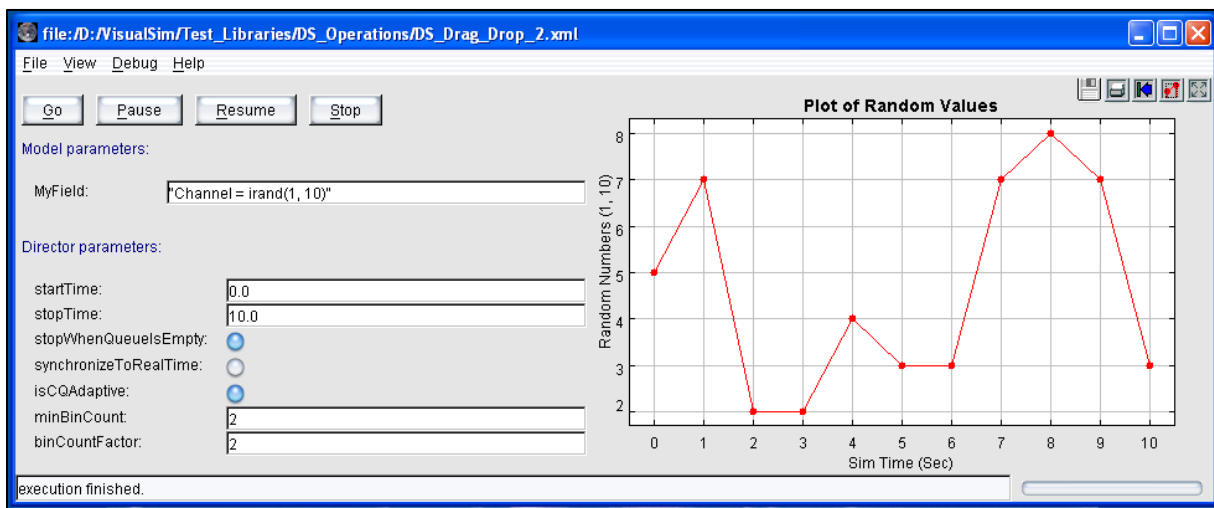


Figure 70. Model Plot

The TimeDataPlotter block accepts a single double input token (Y Axis) and appends the current simulation time (X Axis) to plot each X,Y value. There are other plotting blocks available in the **Result** Library.

31 Resource

Resources model the physical aspects of the system. In the performance of a system design, a model platform is described using the physical components such as **Queue**, **Server**, **SystemResource**, **Flow Control**, and **Associated Arbitration Policies**. The physical attributes could be a Processor, Bus, Cache, and RTOS. Alternately, it can also be a Xon-Xoff flow management and device drivers. The distinction between behavior and architecture is that architecture consumes a quantity - either time, space (such as memory cells and disk bytes) or power. The Time-based, Quantity-based, Event Queues, SystemResource, Channels, and Server are different forms of resources.

There are two ways to define resources - **Active** and **Passive**. Active resources consume **time** while passive resources consume **quantity**. Passive resources can be created using Arrays, Database block or Quantity-shared Resources. All other blocks under resources are categorized as Active.

The usage of a specific block depends on the type of analysis, available information, and the determination of the processing time period.

1. If the processing time for an incoming transaction can be predicted in advance, then the TimedQueue or the Server is preferred. For example, the bus transfer time can be computed in advance for a data size, bus width and speed, after the Bus has been granted. Using the Timed-Queue does not make the model deterministic. It simply means that once the Data Structure gets access to the resource, it is delayed for a fixed time period. There is still queue delay, reordering of the queue for higher priority transactions and arbitration access delay that might create a non-deterministic latency. A Processor, Bus, and other Hardware Entities are best described using the Timed Queue.
2. If there are multiple flows in a model or accesses to a single resource from multiple locations in the model, it is best to use the SystemResource. Moreover, the SystemResource handles the behavior and architecture separation or Y-chart methodology. The SystemResource split the operation between behaviors flow and

the platform. The behavior flow describes the application or task of the algorithms. The platform describes the architecture which includes the hardware, software, and network. The behavior flow has a block called the Mapper that simply takes an incoming request and sends to the named scheduler. The SystemResource performs the arbitration, queuing, pre-computed latency, and the variable latency. Preemption of tasks is performed by the SystemResource and fixed latency + variable latency-based on timers or interrupts is done by the SystemResource_Extend. Any number of Mappers can be targeted to the single scheduler. The SystemResources can also be setup hierarchically where the request come into one scheduler which refers another higher-level scheduler for the actual processing latency. The first SystemResource behaves like a RTOS. Most Mappers can point to the first SystemResource while a few higher priority or interrupt SystemResource can point directly to the higher schedulers.

3. If a slot-based execution is required, then use the **SLOT** option in the Server blocks.
4. If the time depends on external factors and cannot be defined in advance, then the Event Queue is used. In this case, the model has explicit external Pop to get the data out of the Queue. Queues, FIFOs, and other queuing structures can use the Event Queue.
5. If the output from the Queue is based on an external factor such as a proprietary arbitrations scheme, then Queue is the solution. The operation is similar to the basic type. But the Pop can be connected to a Smart_Controller script and the statistics and queue length can be accessed using the Queue Name. So, any algorithm can be engaged to perform the Pop.

31.1 Queues

Examples of using Queues are shown in Pre_Built Models > Performance Modeling Blocks > Event Queues. The Data Structures are queued in order (order of priority, if Priority version) and is removed from the queue when a “Pop” arrives. The "Pop" can be triggered by a control operation anywhere in the model. This is used wherever Queues or Stacks (queue in LIFO mode)

are required. The queues can be triggered in different ways depending on the flow control or other operations in the system model. Depending on the number of queues in the block, the Pop needs to arrive along with a Queue Number (separate ports). The Queue is a regular Queue or a priority-driven preemptive Queue with a FIFO or LIFO processing. The M/M/1 system is made of a Poisson arrival, one exponential (Poisson) server, FIFO (or not specified) queue of unlimited capacity and unlimited customer population. This assumption is a very good approximation for arrival process in real systems that meet the following rules:

- a. The number of Data Structures in the system is very large.
- b. Impact of a single Data Structure on the performance of the system is very small, that is a single Data Structure consumes a very small percentage of the system resources.
- c. All Data Structures are independent, that is. their decision to use the system is independent of other users.
- d. The blocks are G/N/1, which means the arrival is variable and the size of the queue is defined.

31.2 Timed_Queues:

Examples of using Queues are shown in **Library Models > Performance Modeling Blocks > Timed Queues**. Similar to a queue, this maintains the incoming data structures in a Queue. The Queue is a regular Queue or a priority-driven preemptive Queue with a FIFO or LIFO processing. Unlike the basic queue, this does not require an external Pop. At the output of this Queue, there is a Server resource which delays the Data Structure by the quantity of time provided in advance. This is used when the latency or delay through the resource is known prior to the Data Structure entering this block. For example, the latency across a bus after the bus has been allocated is predictable. This block queues the Data Structure along with the time value. When the Data Structure reaches the head of the Queue, it is delayed by this time value and then placed on the output port.

Note: A special case of the TimedQueue is the ServerN block. Here there is a single queue that is connected to multiple server resources. The Queue is a priority-driven preemptive Queue with a FIFO processing.

31.3 Passive Resources:

Examples of using Queues are shown in **Library Models > Performance Modeling Blocks > Quantity-Shared Resources**. This represents a discrete quantity of resources (Battery charge or cache words) that are available in a resource pool. When a request comes in, the Data Structure is allocated quantity, based on the amount available in the pool. The allocated is returned to the queue at some future times. The time between the allocation and release is the processing time. The allocation is done using the Resource_QS and the Task_Complete returns the resource back to the pool.

31.4 Channels:

This block extends the concept of Queues by defining the operation as a series of logic operations, as opposed to an external Pop or a fixed delay value. This block has a single Queue with access to multiple Channels. A special case of this block is the Channel_N I has an individual Queue for each Channel. This block is used to define channels that are noisy or have a loss probability or have algorithms performed on the data. The channels contain three parts- a dispatcher block; the logic using any VisualSim blocks and a completion block. The issuer block accepts the incoming data structure and assigns it to one of the channels. The logic is functionality defined between the issuer and the complete blocks. The complete blocks can either be used to acknowledge a successful completion (accept_port) or request a retransmission (reject_port).

The Channel blocks model a fixed number of channels. The key difference between the Channel and the Channel_Priority is the additional priority parameter that is used to determine the next task to be scheduled on the channel. The Channel_N has a separate priority-based queue for each channel.

31.5 SystemResource

Examples of using SystemResource are shown in **Library Models -> Resources -> SystemResources**. SystemResource is used when the queue requires preemption. SystemResource_Extend is used when granularity, dependent firing and other operations must be performed. Schedulers are also preferred when the request to the resource has to come from many physically separated parts of the model. The schedulers emulate hardware and RTOS resources more accurately. There are two types of scheduler blocks. The blocks receive the input virtually from a Mapper or a RegEx scheduler call. The input port triggers the statistics. The SystemResource is used where preemption is required or the scheduler is defining a lower-level resource. A lower level resource depends on another resource to actually execute the operation. A good example of this is a RTOS requiring a CPU to complete the processing. The SystemResource_Extend is a highest-level processing resource such as a bus, CPU or memory. This block is preferred where the processing cannot be entirely defined with the block parameters and time value. For example, a processor may need to access memory before completing the processing. The SystemResource_Extend can be connected on the output port to another Mapper that calls another SystemResource to emulate the cache access. The differences between the SystemResource and SystemResource_Extend are explained below.

31.6 Key Difference between SystemResource and SystemResource_Extend

Features	SystemResource	SystemResource_Extend
Preemption	Yes (Pre-emption is not allowed if there are more than two schedulers in a hierarchy or the SystemResource_Extend is extended using the "output_port" port.)	No

Features	SystemResource	SystemResource_Extend
Hierarchical	Yes	No
Extended Task Processing	No	Yes
	Can reference another scheduler	Cannot reference and execute in the next-level scheduler

Caveat: A SystemResource can support preemption only when there are zero or one SystemResource above this one.

32 Processing

1. **Defining Flows blocks:** These are programming blocks used in defining expressions, evaluating, assignments, and making control decisions. The types of operations includes:

- ⇒ Mathematical or Logical Statement
- ⇒ if-else
- ⇒ else
- ⇒ while
- ⇒ switch-case
- ⇒ Field selection

The Data flow blocks are used to evaluate expressions, assign values to a Field or variable, randomize Field values, calculate processing cycles on a scheduler or Resource_FCFS blocks, compute statistics such as latency (TNOW - TIME), utilization and throughput and create assumption values. Control Flow blocks are used make decisions, create loops, and take branches.

2. **Using Database:** The Database block is a high-performance lookup utility and resembles a relational database. Create a lookup table using this block and link it with other database blocks in the model. The table can be read by one Database block when it is written by another block. The lookup table can have up to 4000 entries and each entry can contain multiple columns of data. This example `$VS\demo\system_architecture\Msg_DMA\Message_DMA.xml` shows the creation of the lookup table, modifying it based on external content and conducting a DMA transfer based on the lookup. Notice that all three operations are performed with a single instantiation of the table.

Virtual Connections: The IN, OUT, MUX, and DEMUX blocks constitute a set of powerful blocks that are intuitive to use and do not require any routing information, except the user entry of the proper source and destination names. In the simplest form, the IN, OUT Blocks are similar to references in a CAD drawing linking to a specific point in the model. If an IN and OUT Block have the same reference name, then they are linked directly in the Graph Editor space. The biggest concern of user is that named references are unique; else certain connections are inadvertently linked to others in Graph Editor. These blocks can be used for model routing, making decisions, and triggering events in the model. Use RegEx function called `readAllVirtual` to get list of virtual connections in model.

33 Hardware Modeling

The Hardware Modeling toolkits generate transaction-level and cycle-accurate models of complex, hardware devices. Using this generator and the associated hardware architecture library, platform architecture can be defined graphically without the need to write C code or create complex spreadsheets of the instruction sets. These platform models can execute software profilers or compare hardware accelerators. The virtual platform can be used to select components, optimize component size and speed, and define arbitration algorithms. This virtual platform can be saved as a library for use by processor architect, systems engineer, and software architect within an organization.

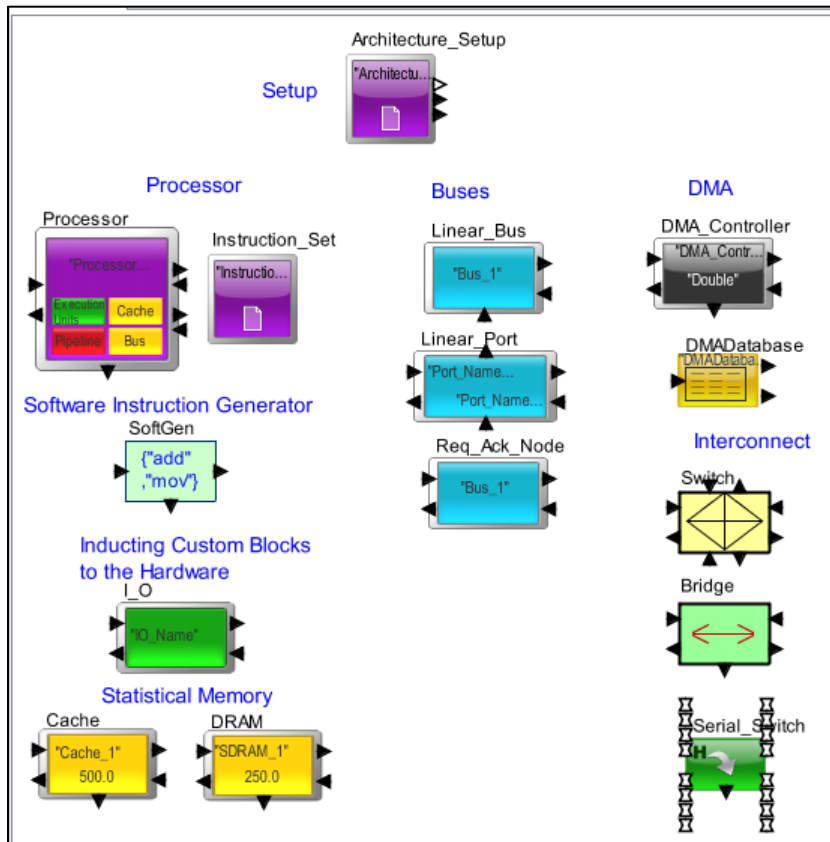


Figure 71. Hardware Modeling Library

33.1 Processor

The Processor block can model embedded, super-scalar, DSP, or application-specific processors by defining parameters commonly found on a Processor data sheet or website. The Parameter_Value column can also reference other model parameters.

33.2 Software Generator

The TaskGenerator block is used to generate new tasks to execute on the processor. The mix of instructions in the task is read from the file that is referenced by the parameter Read_My_Instruction_Mix_Table.

33.3 DRAM

This block combines a basic memory controller (delay function) and the memory cells to form a memory device.

This block handles pre-fetch, read, write, refresh, and controller operations. The block can be connected to BusInterface, BusArbiter or Buses/controller directly. Alternately, it can also connect to a SystemC or other models of a Bus not constructed using the VisualSim Hardware Architecture libraries. The incoming instructions are treated as Read, Prefetch or Write.

33.4 Integrated_Cache

This block is used to emulate a cache in an architecture model. The block supports both stochastic and address-based modeling. The block support requests arriving from the processor/accelerator on one side and output to the next-level cache or memory on the other side. Both sides are connected to buses. There are interfaces on both sides of the block for connectivity. The block handles request queuing, cache access latency, cache hit-miss evaluation, Cache Prefetch, Read/Write data response, and Cache miss activity to the next level of memory.

33.5 Linear Bus

A Linear Bus is another term for a shared Bus with independent queue at each interface and single arbiter. The BusArbiter block represents the Arbiter for a Linear Bus. This is combined with multiple

instances of the BusInterface to create a Shared Bus topology. Examples of Bus structure created using this block include Shared Ethernet, AMBA (AHB and APB), and CoreConnect (OPB). Custom and proprietary bus topologies can also be created using this block.

33.6 DMA

DMA block that represents a memory controller that sits between the Processor or bus or DeviceInterface Block and the Memory bank. The IO Controller acts as an intermediate block and just transfers the transactions from bus or DMA Controller to appropriate memory bank or devices connected to the DeviceInterface. DeviceInterface receives the response from memory bank or devices and transfers it back to the bus/DMA. The DeviceInterface can be connected to either a Linear or Point to Point bus.

33.7 Bridge

The Bridge block is used to connect two Buses together. If two connected buses send out hello messages, the connected devices do not require a Routing Table entry.

33.8 Switch

The Switch block can be used for both Blocking and Non-Blocking mode. There is a selector parameter that determines the mode of operation.

The Blocking Switch is a crossbar switch with a single internal bus resource. This switch transfers request from a Source (A_Source) to a Destination (A_Destination) in a First Come-First Serve order. There is a single internal queue and all transactions across the switch are placed in this queue.

The Non-Blocking Switch is a mesh crossbar switch with a point-to-point connection between each source (A_Source) and destination (A_Destination). This switch transfers requests from each Source (A_Source) to each Destination (A_Destination) in a First Come-First Serve order. Each Source-Destination combination has a separate queue. There are multiple channels assigned for each Point-to-Point connection. The transaction is assigned to a channel based on the value in the

Field Name containing the channel. Multiple channels can be dynamically created during a simulation just by the value in the Channel Field.

33.9 Serial Switch

The Serial Switch is a serial mesh crossbar switch with a point-to-point connection between each source (A_Source) and destination (A_Destination). The standard block has 16 Input/Output Device connections. Multiple Channels can be defined to each Source-Destination combination. This block supports Power estimation. This block supports multiple PHYs to be connected to each Channel. In this case, multiple bits can be transferred in parallel for each Channel.

34 Buses

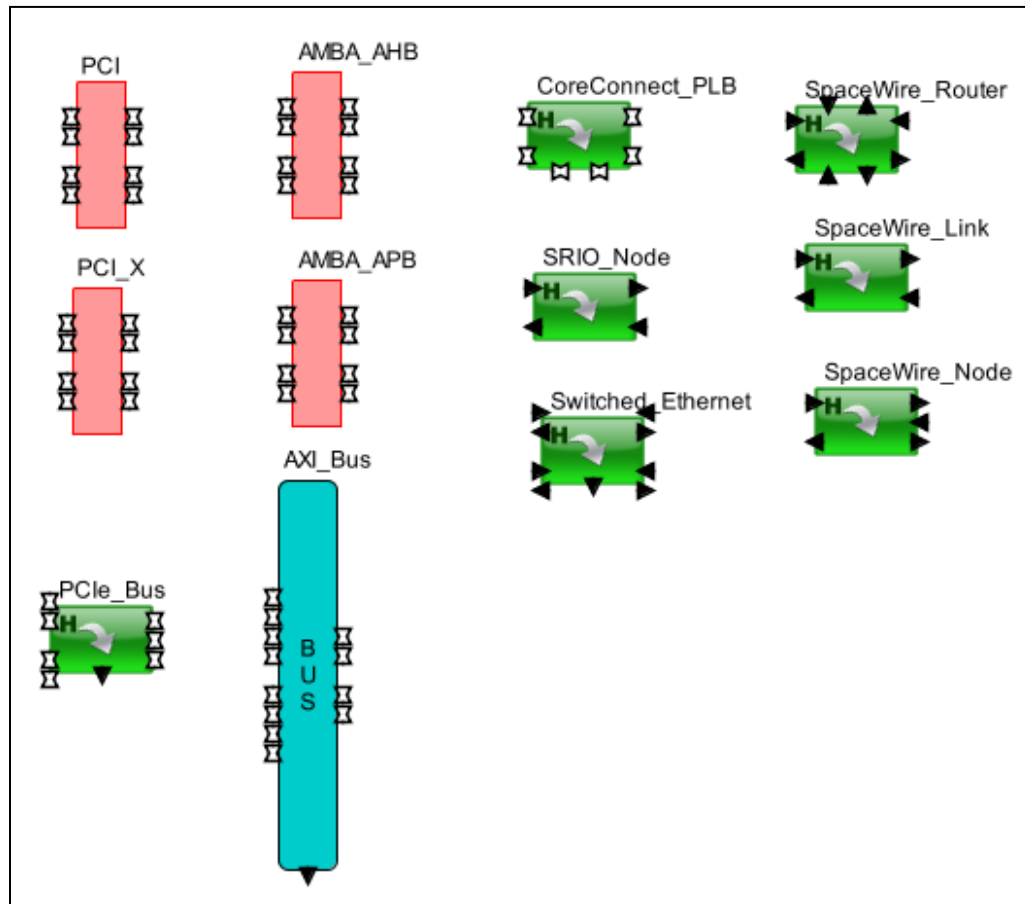


Figure 72. List of Hardware Buses

The above figure shows the list of hardware buses. Network or box levels buses are not included.

34.1 AHB and APB

The AMBA-AHB and APB Local bus protocol are high performance buses for interconnecting peripheral IP to any independent processor/memory subsystems within a SoC. The AMBA-AHB bus block can use as interconnect between high bandwidth peripherals closer to the CPU for performance gains.

- AMBA AHB features:

- High performance
- Pipelined operation
- Multiple bus masters
- Burst transfers
- Split transactions
- Statistics collected for the AMBA Bus include
 - Throughput in Mbps
 - Utilization percentage
 - Input Output transactions per sec (IOs_per_second)
 - Input buffer occupancy in words

This model has been fully validated against the specification. Refer to the Bus Documentation section to see the validation details. This library component is used to assemble complex systems that contain one or more AMBA buses. The default AMBA comes with split-and-retry turned on and uses a First Come-First Server arbitration. The user can modify these two attributes to turn off Split-Retry and make the protocol Round-Robin. The Linear Bus has a hidden parameter called AHB_Mode. To make the linear port an AHB or APB bus, this parameter is added and set to true. This allows only a single transaction to be active on the bus.

34.2 AXI

The AMBA AXI Bus protocol is targeted at high-performance, high-frequency system designs and includes a number of features that make it suitable for a high-speed sub-micron interconnect. The objectives of the AMBA AXI Bus are to be suitable for high-bandwidth and low-latency designs and enable high-frequency operation without using complex bridges. It meets the interface requirements of a wide range of components and it is suitable for memory controllers with high initial access latency and provide flexibility in the implementation of interconnect architectures.

34.3 PCI and PCIx

The PCI and PCI-X Local bus protocol are high performance buses for interconnecting peripheral chips to any independent processor/memory subsystems. The PCI bus block can use as interconnect between high bandwidth peripherals closer to the CPU for performance gains.

This model has been fully validated against the specification. Refer to the Bus Documentation section to see the validation details. This library component is used to assemble complex systems that contain one or more PCI buses. The default PCI comes with split-and-retry turned off and uses First Come-First Server arbitration. The user can modify these two attributes to turn on Split-Retry and make the protocol Round-Robin.

34.4 PCIe

PCI Express (PCIe) provides a scalable, high-speed, serial I/O bus that maintains backward compatibility with PCI applications and drivers. The PCI Express layered architecture supports existing PCI applications and drivers by maintaining compatibility with the existing PCI model. PCI Express having parallel bus topology and Multiple point-to-point connections. A switch may provide peer-to-peer communication between different endpoints and this traffic. A PCI Express link consists of dual simplex channels, each implemented as a transmit pair and a receive pair for simultaneous transmission in each direction. Each pair consists of two low-voltage, differentially driven pairs of signals. A data clock is embedded in each pair, using an 8b/10b clock-encoding scheme to achieve very high data rates.

34.5 CoreConnect

The Processor Local Bus (PLB) protocol is a high performance bus for interconnecting processor, memory subsystems, and high bandwidth peripherals. There are IBM and Xilinx versions of the bus that match specific timing for reads and writes. The CoreConnect Bus hierarchical block supports four master and two slave ports with bi-directional ports.

34.6 Switched Ethernet

Switched Ethernet is an Ethernet technology deployed from a central box over Category 5 twisted-pair wire or fiber optic. Switched Ethernet allows the full utilization of bandwidth for each network conversation by switching connections point-to-point between stations talking to each other, providing in effect a dedicated channel between each source and destination. This library models the messaging and the backbone switch associated with the Switched Ethernet. The setup contains the PHY, MAC, connected Queue, and the Switch. This library models a full Duplex operation and does not support collisions.

34.7 Spacewire

The SpaceWire standard addresses the handling of payload data on-board a spacecraft. It is a standard for a high-speed data link, which is intended to meet the needs of future, high-capability, remote sensing instruments, and other space missions. SpaceWire provides a unified high-speed data-handling infrastructure for connecting together sensors, processing elements, mass-memory units, downlink telemetry sub-systems and, EGSE equipment.

The SpaceWire standard specifies the physical interconnection media and data communication protocols to enable data to be sent reliably at high-speed (between 2 Mbps and 100 Mbps or more) from one unit to another. SpaceWire links are full-duplex, point-to-point, serial data communication links.

34.8 RapidIO

The **RapidIO Block Set** contains the RIO_Node and a Serial_Switch. The RIO_Node handles the Ingress buffer for the Source, Egress Buffer for the destination, v1.3 and v2.1 flow control, fragmentation, mailboxes and logical layer processing. The Serial_Switch provides the virtual channel bandwidth assignment, the physical lanes, switch buffers and packet selection algorithm. The RapidIO library supports the v1.3, v2.1, and the v3.2 specifications. These include support for 8/10 signaling, 64x lanes, and 100Gbps per lane.

34.9 TimeTriggeredEthernet

Time-Triggered Ethernet functionality is implemented based on the SAE AS6802 specification of the Layer 2 Quality-of-Service (QoS) enhancement for Ethernet networks. The library provides the capability

for deterministic, synchronous, and congestion-free communication, unaffected by any asynchronous Ethernet traffic load. The block supports the isolation of the synchronous time-critical dataflow from other asynchronous Ethernet dataflow. This implementation of the standard enables designers to test, define the topology and validate their architecture for performance latency, throughput, jitters, and other intrusions such as large, high priority packets, rate-controlled data streams and virtual LANs. This means that distributed applications with mixed time-criticality requirements (for example, real-time command and control, audio, video, voice, data) can be integrated and coexist on one Ethernet network.

The TimeTrigeredEthernet or TTE contains the Traffic Generator, the Node, Bridge, and Statistics blocks. In addition, the network is configured using a Config and a Network Setup library blocks.

34.10 Avionics Full-Duplex Switched Ethernet

The VisualSim AFDX data network library is a specific implementation of ARINC Specification 664 Part 7, a profiled version of an IEEE 802.3 network per parts 1 & 2, based on the Airbus implementation. The six primary aspects of an AFDX data network include full duplex, redundancy, deterministic, high speed performance, switched ,and profiled network.

The library implements redundant switches with a single block for Transmitter and Receiver. The traffic for all the nodes is controlled from a single source. The output plots can be used to identify system bottlenecks, determine the feasibility of the topology, and measure the latency for messages across the network.

34.11 CAN/CAN-FD

The CAN library in VisualSim is based on the Bosch specification and the international standard defined in the ISO 11898-1. This is a single library that combines both the standards in a single block. The formats are consistent with Vector CANdb. Models with multiple networks separated by bridges and connected to Ethernet networks through switches are supported.

34.12 Audio-Video Bridging

Mirabilis Design provides an Audio-Video Bridging (AVB Library) as a standard add-on to the Ethernet and Networking application library in VisualSim Architect modeling environment. Using this environment,

systems engineers and product architects can evaluate the impact of design decisions on the performance of their system. The AVB library has been built to the specification of the IEEE 802.1BA for time-synchronized low latency streaming services. The library supports the following standards:

- IEEE 802.1AS: Timing and Synchronization for Time-Sensitive Applications (gPTP),
- IEEE 802.1Qat: Stream Reservation Protocol (SRP),
- IEEE 802.1Qav: Forwarding and Queuing for Time-Sensitive Streams (FQTSS), and
- IEEE 802.1BA: Audio Video Bridging Systems

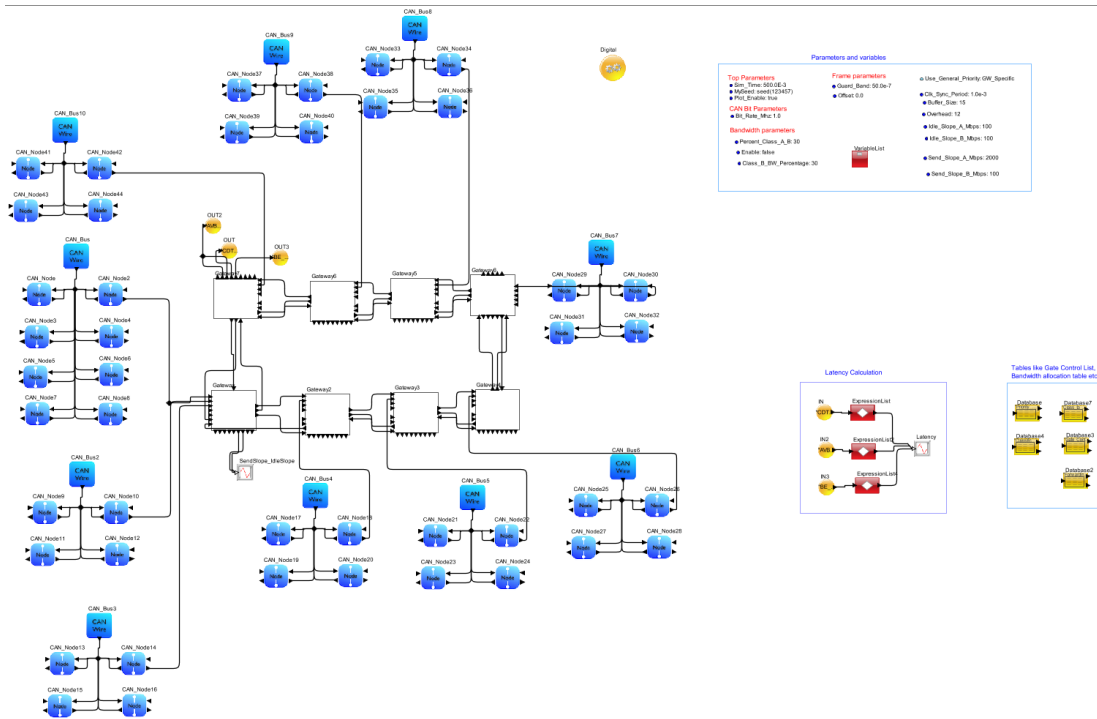
VisualSim AVB modeling environment supports the requirement of the automotive, consumer, and professional audio and video markets. Combined with the industry hardware, software, and system library provided in VisualSim Architect, designers assemble an end-to-end system and evaluate the throughput, latency, and other performance attributes. The proposed system can be tested for various fault and error conditions to evaluate the susceptibility of the system for real-world conditions.

VisualSim AVB can be used to design a completely new AVB-based network to integrate all the equipment, upgrade existing networks, and to design the electronics that are used in such networks. The AVB system can include the talkers and listeners such as video cameras, radars, broadcast systems, displays, and Electronic Control Units. The network can include AVB interfaces, bridges, switches, and gateways.

34.13 TSN

TSN is a set of standards defined by Time-Sensitive Networking task group of the IEEE 802.1 working group, the standards which define mechanisms for the time-sensitive transmission of data over Ethernet network. For Ethernet to be used here, the strict priority scheduling of IEEE802.1Q needs to be enhanced. Deterministic Ethernet refers to a networked communication technology that uses time scheduling to bring deterministic real-time communication to standard IEEE 802 Ethernet. The criticality of frames is as follows: **CDT>AVB>BE**

TSN library supports IEEE802.1Qbv, IEEE802.1Qbu, IEEE 802.3br, IEEE 802.1Qca, IEEE 802.1Qcc, IEEE 802.1Qci, IEEE 802.1QCB, IEEE 802.1Qch and IEEE 802.1AS protocols.



Each of the message frames will be assigned a HashID which is unique to them in the entire model. Here, the implemented test case has 8 Gateways. We make use of a table called Classification Table which stores information on the type of Routing, parent Gateway, associated Hash ID for the message frames and parent CAN bus name. A table called ForwardingTable is used for forwarding the generated packets out to the destination and for assigning a Class type to each frame. The packets which have to go to CAN nodes at a different Gateway have to go through ETH. If a packet coming into the Gateway has its destination local to the Gateway, the packet is converted into respective protocol and sent out on the local interface. Each of the class types specified has a Bandwidth allocated to it. It can be obtained from another table called Priority BW. The TSN library uses a table called Gate Control List defining time slices and the classes associated with it.

In this Test case, we have used two time slots. For the first slot the Class Measurement Interval (CMI) is of 2 msec. This time slot is allocated only for CDT frames. A Maximum Interval Frame (MIF) of 5 is used. The remaining time is allocated for AVB Class A and B and BE. First, Class A and class B frames are given the opportunity to transmit frames. This continues until they deplete their allocated Bandwidth or complete transmitting the data, then BE is given a chance.

For the second time slot, CMI is 8 msec and MIF of 15000 is used. If the bandwidth allocated for AVB and BE is exhausted after task completion but there is time remaining, we check for any priorities

defined with zero bandwidth. At the end of defined time slots, a guard band of specified time is added to prevent overlapping and to send frames. The VisualSim library has implemented Time Aware Shaping (TAS) which ensures on each slot getting their time resulting in an efficient use of resources.

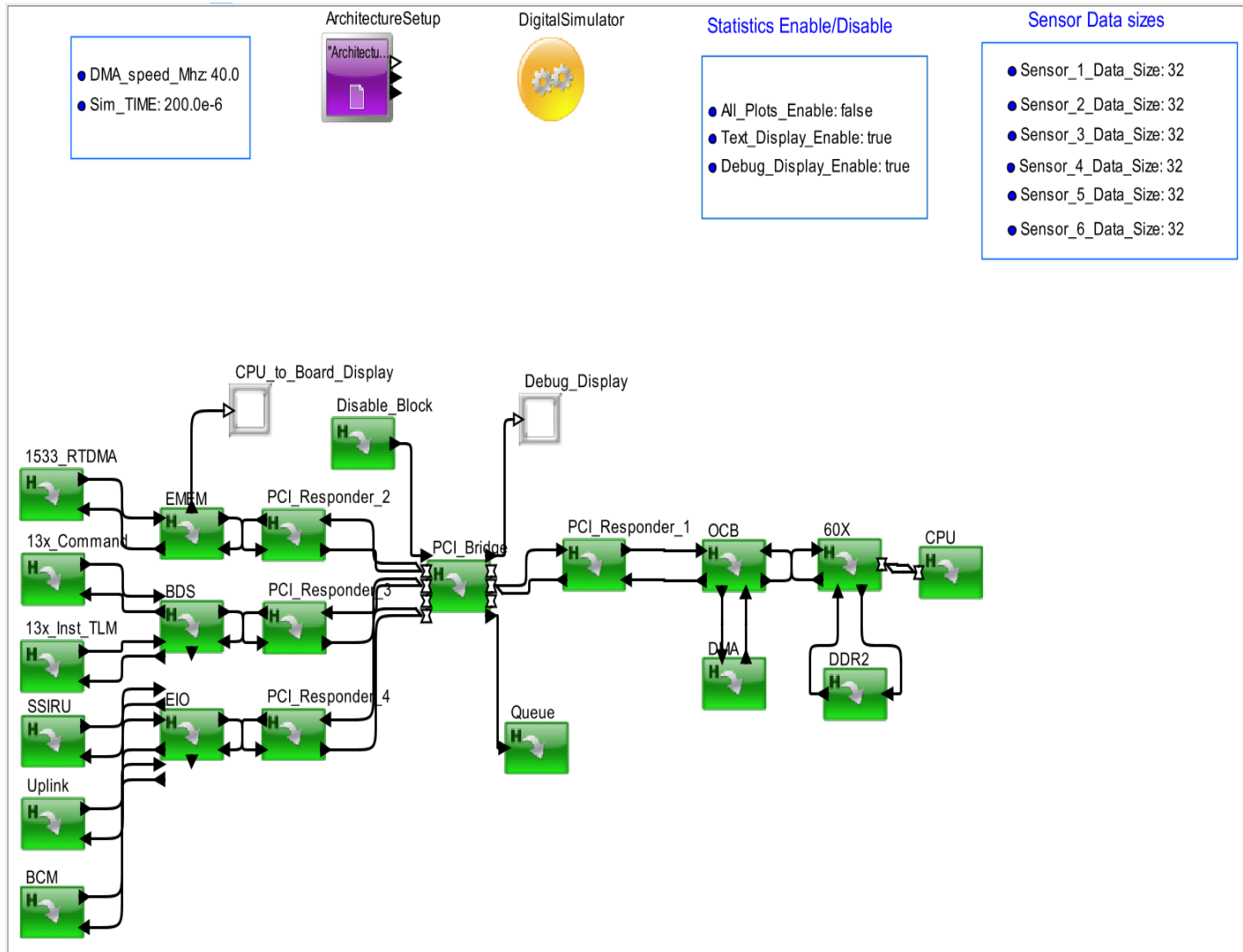
34.14 PCI RAD

The PCI RAD is an arbitration based bus which is used for interconnecting peripheral chips to any independent processor/memory subsystems. This library emulates all the functionality of the PCI RAD standard. There is a single block called PCI_Bridge. There are 7 ports for this block. Each port can act as a master and slave. For this blocks to operate correctly, the model must contain two blocks as prerequisite- Architecture_Setup and Digital Simulator. The PCI_RAD implements an arbitration scheme according to which masters are given access to the bus. The PCI_RAD is having 3 priority levels. Priority Level 1 is given highest priority then level 2 and then level 3. Lets say Priority Level 1 has following masters : Master_1, Master_2 and Master_3. Priority Level 2 has the following masters: Master_4 and Master_5. Priority Level 3 has the following masters: Master_6 and Master_7. Then according to the arbitration scheme this is the order at which masters are given access to the bus. Master_1, Master_2, Master_3, Master_4, Master_1, Master_2, Master_3, Master_5, Master_1, Master_2, Master_3, Master_6, Master_1, Master_2, Master_3, Master_4, Master_1, Master_2, Master_3, Master_5, Master_1, Master_2, Master_3, Master_7, Master_1.....

At a moment only one read and write could take place and not more than one. Lets say a "Read" has been sent from the PCI. So until that Read has been completed, the PCI_RAD cannot issue another "Read".

There is a Latency Timer in both Initiator side and Responder Side. If any one of them expires, then a Terminate happens and the values are stored in respective queues. Then the next master which is having a "Read" is given access. While a "Read" is taking place, a Master having a "Write" can also issue its task.

If any of the data structure coming into the PCI has a field called Terminate and if that fields value is true, then the current task is terminated and stored in the queue. There is also a Disable port provided, through which we can disable a master for our desired period of time.



35 Cycle-Accurate Cache and Memory

VisualSim provides the ability to model the entire memory hierarchy at the implementation-level detail. These libraries are fully extensible using both parameters and the input of custom arbitration algorithms using the scripts.

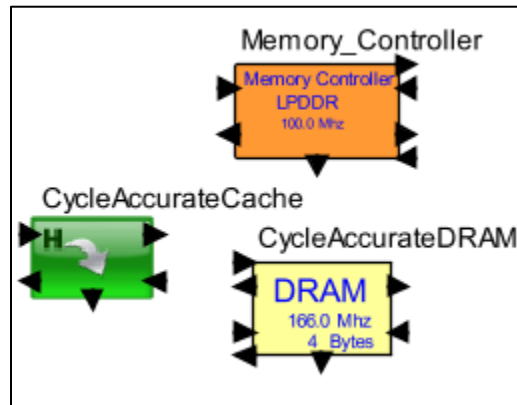


Figure 73. Cycle-Accurate Cache and Memory Models

35.1 Cycle-Accurate Cache

The HW Cache is a cycle accurate cache model that performs all standard cache operations. The size, associativity, and current cache content determines the hit ratio.

35.2 Cycle-Accurate Memory Controller

This is the framework for an extensible Memory Controller. All common and standard features for the arbitration, generation of DRAM signals, look-ahead and the FSM for the control are included. In addition, the user can add their own custom algorithm by referencing an external script file.

35.3 Cycle-Accurate DRAM

The HW_DRAM is a cycle accurate dynamic RAM model that accepts commands that reflect specific memory processing, including multiple memory banks and a bi-directional bus. This block supports most common DRAM formats including, SDR, DDR, DDR2, LPDDR, LPDDR2_NV, LPDDR2_S2, LPDDR2_S4, and DDR3. This DRAM block is used in conjunction with the hardware Memory Controller,

which generates the detailed dynamic RAM commands. In addition, the Memory Controller has knowledge of specific bank activity to coordinate requests and not overwrite ongoing transactions. This block emulates common SDRAM technology. The block can be used to capture the functionality and accurate timing of any variation of DRAM. The block supports addressing, multiple banks and can save data into a memory array. The block supports sequential, non-sequential, and random reads. The block supports burst, non-sequential, and random writes. The block handles the following conditions:

- Sequential burst Read
- Non-Sequential burst Read
- Random burst Read
- Sequential burst Read with row crossing
- Read followed by Sequential Write
- Read followed by Non-Sequential Write
- Sequential burst Write
- Non-Sequential burst Write
- Write followed by Random Write
- Write followed by sequential burst Read
- Write followed by a Non-Sequential burst Read
- Write followed by Random Read
- Active to Active latency
- Bank to Bank latency

The block plots the DRAM_Bank_N (tRAS (empty space), tRP, tRCD, Data (shorter values)); DRAM_BiDir_Bus activity; MC Read Requests; and MC Write Requests.

36 PowerTable

The **VisualSim PowerTable** is used to define the power details of the blocks in a model and generate the statistics for all the blocks in the model. The Power_Table can be built hierarchically, which means each level can have its own Power Table. When a top-level Power_Table is connected to a Battery block, it will transfer the power request from all the Power_Tables in the hierarchy of this branch. This Library is used to evaluate the effectiveness of power scheduling algorithms and to estimate the power consumption of a design. The PowerTable updates the instantaneous and cumulative power using dynamic state change information of the individual devices. The PowerTable is fully integrated with the ArchitectureLibrary, scheduler blocks, and the RegEx language. RegEx- stateChange function can dynamically alter the power level of a state. The devices analyzed can be a VisualSim library block, custom hardware accelerator, and software components. The PowerTable library consists of the Power_Table, Battery, Power Harvesters and RegEx functions for making state changes and accessing the statistics content of the table.

Multiple Power_Tables can be maintained in a single model. Any number of devices can be associated with a single PowerTable block. Each standard device can have any number of states, single transition time between states that is used for all states and a reference to the state that is currently associated with Active and Standby. VisualSim libraries blocks support Active and Standby. The Processor has Wait and RAM block uses Wait for Refresh. The **VisualSim** PowerTable is based on dynamic system operation and enables users to design application-based power schedulers and make trade-offs between performance and power consumption including battery drain.

The power for each device is maintained individually. When the operation state of a device changes (idle, standby, wait, and busy), the power level goes to the new state. There is a delay to go to the new state called State Transition delay. This value may be different for different power states. It is possible for a designer to assign delay for individual states.

Let us take an example. When the Processor is in standby state, the PowerTable maintains the current power consumed by this processor to be value in the standby column for this processor. When processor moves to active to busy state, the PowerTable delays by that amount as

mentioned in t_OnOff. This is an automatic internal process and the user does not have to do anything. If the user has a hardware accelerator, the model uses the functions listed below to update the state change or a new power level.

RegEx Functions:

X = powerManager(power_manager_name)- Gets the power that contains the power statistics for all hardware blocks associated with this power table.

X = stateChange(power_manager_name, Device name, Operating State, New State Name)- Changes the Operating state (Existing, Active or Idle) of a device to the New State Name.

37 Selecting the right block for your model

VisualSim has a number of library blocks. After you understand the operation of a block, you can apply it in many ways. We have created a table that provides guidance on the use of VisualSim.

37.1 Traffic Generation

Action	Blocks	Example Model
Fixed Rate with fixed size For example, Sensor, I/O	Traffic (Set Distribution to Fixed)	
Clock	Traffic (or) Clock	
Packet-based network traffic Variable data size	Transaction_Sequence (or) Single_Event + TriggeredTraffic + ExpressionList (generate size and delay to next) + Delay in the loop-back to start next sequence	
Multiple instance of any traffic generation	Dynamic Instantiation + (Any combination of blocks inside)	
Bursty traffic + periodic interval	Transaction_Sequence (Time_Field) + Delay in the loop- back to start new sequence	
Sequence of operations. For example, Read, Write, read, Read For example, 32, 64, 128, 256 Bytes	Transaction_Sequence (Time_Field) + Delay in the loop- back to start new sequence	
Custom Distribution	Transaction_Sequence (Time_ and Probability_Field) + Delay in the loop-back to start new sequence	
Custom Distribution with variable	Transaction_Sequence	

Action	Blocks	Example Model
delay	(Probability_Field) + Delay in the loop-back to start next row	
Trace- Network and hardware	Traffic_Reader	
Use traffic generated from another model	File Reader, XML_Task	
Read from file and use the content for the delay between transactions	Transaction_Sequence	
Start a model execution	Single_Event	
Read from csv/Excel file	Database, Traffic_Sequence and Excel_to_DS	

37.2 Variables

Action	Blocks	Example Model
Constants or fixed values. Value needs to be changed for each run and stays constant in a single simulation	Parameter	
Register or variable	Variable	
Flags for setting system condition For example, Resource availability.	Variable	
Storing same states of multiple devices For example, Queue length of multi-core.	Variable (array type)	
Storing intermediate values	Data Structure field	

Action	Blocks	Example Model
associated with a specific transaction For example, Device trace. For example, Time arrived at a port or processor.		
Attributes of a transaction For example, Data size, priority, source, destination	Data Structure field	
Fragment number, last fragment indicator	Data Structure field	
Communication information from one part of the system to another instantaneously For example, Queue length of an ingress port.	Variable	
Send notification from one device to the next one	Event (not a block)	
Trigger the sending of the next transaction based on completion of prior transaction	Event (not a block)	

37.3 Plotting

Action	Blocks	Example Model
Latency	ExpressionList + TimeDataPlotter For example, TNow – input.TIME	
Throughput	Variable- Increment each	

Action	Blocks	Example Model
	<p>completed size into a variable location</p> <p>Display: ExpressionList + TextDisplay (end of sim)</p> <p>Plotting: Trigger (Traffic) + ExpressionList + TimeDataPlotter</p>	
Read_Latency	<p>ExpressionList + TimeDataPlotter</p> <p>Probe at Source in return path.</p>	
Write_Latency	<p>ExpressionList + TimeDataPlotter</p> <p>If acknowledge required (A_Task_Flag==true), then probe at source, else probe at destination (like DRAM)</p>	
Custom calculation plot (separate based on packet size)	<p>Variable (store results, can be a array) ExpressionList + TimeDataPlotter (might need trigger for regular output)</p>	
Timing Diagram Processor, Cache, DRAM, Linear_Bus, AHB, APB, PCI, PCIx, CA_DRAM, Memory_Controller, AXI	Timing_Diagram	
Extract fields to plot	<p>ExpressionList block (output_values to specific field like input.ID) + TimeDataPlotter</p>	
Two data sets against each	ExpressionList block (two	

Action	Blocks	Example Model
other (Throughput vs. packet size)	output) + XYPlotter	
Any dynamic variable	Variable + ExpressionList (update) Display: ExpressionList + TextDisplay (or) TimeDataPlotter	
Histogram	Statistics + Histogram (or) Variable + ExpressionList + Histogram	
Multiple dataset from different blocks	TimeDataPlotter or XYPlotter (each dataset comes from a different block or connected to a relation)	
Multiple dataset from a single block output	DS_XYPlotter (for different x and y values) (or) DS_TimeDataPlotter (for y value vs. time)	
Use data structure input but plot specific field values arriving from the same block output.	DS_XYPlotter (for different x and y values) (or) DS_TimeData (for y value vs. time)	
Set specific color for each dataset arriving from the same block output.	DS_XYPlotter (for different x and y values) (or) DS_TimeDataPlotter (for y value vs. time)	

37.4 Statistics

Action	Block	Example Model
Generate statistics for custom values	Statistics + TextDisplay (or) Statistics + Histogram	
Statistics for Server, Queue and SystemResource	ResourceStatistics + TextDisplay	
Hardware Blocks: Processor, Cache, DRAM, Linear_bus, AHB, APB, PCI, PCIx, DMA_Controller, Req_Ack_Node, CoreConnect	ArchitectureSetup (internal_stats_out, util_stats_out) (or) ArchitectureSetup (Statistics_to_plot parameter + plots_out)- Must set the width of output link to the number of items to be plotted	
Other Hardware: AXI, PCIe, Rapid IO, Switch Ethernet, VME, 1553B, Memory_Controller, CA_DRAM, CA_Cache	Connect blocks' status port to TextDisplay Set Sim_Time parameter to end time	

37.5 Power Statistics

Action	Blocks	Example Model
Average Power	PowerTable (middle port) + TimeDataPlotter	
Instant Power	PowerTable (top port) + TimeDataPlotter	
Power Dissipation	PowerTable (lower port) + TimeDataPlotter	

Action	Blocks	Example Model
Power/device	Use RegEx powerCumulative + TimeDataPlotter	
Bar graph of Power/device	RegEx powerCumulative + TimeDataPlotter	
Bar graph of power/Device as a percentage	RegEx powerCumulative/RegEx powerCumulative for POverTable + TimeDataPlotter	
Check Deadline for task completion	For scheduler, (Time Finish – Time Activation) > Task_Deadline	
VCD output	VCD_Writer	
Write data structure for use later or in another model	FileWriterFile Writer	
Write to Excel	CSVWriter	
Write to XML	DS_to_XML	
Write to file any text display or plot	Use the Save setting of the plotters	

37.6 Resources and Hardware

Action	Blocks	Example Model
DMA	Channel (statistical) (or) DMA + DMADatabase	
Switch	Switch (or) SystemResource (Blocking) (or)	

Action	Blocks	Example Model
	Non_Blocking_Switch (or) Server (Non-blocking)	
Multi-core with a pool of cores for first come-first serve	Server_N_Resource	
Multi-core with assignment to specific cores	SystemResource (or) Server	
Multi-core with selection of first available	Group of SystemResource (or) Server + RegEx Queue Name + “_Length” to find the first 0	
Wireless/wired channels with error detection and retransmission	Channel + Channel_Complete + Database (error probability)	
Wireless channels with errors but no retransmission	Channel + Channel_Complete (all data sent to accept port and rejected after channel_complete) (or) Server (rejected after block)	
RTOS	SystemResource (or) Queue + Smart_Controller (or) Server (Slot Mode)	
Scheduling- First come-First Serve or Round Robin	SystemResource or SuystemResource_Extend	
Scheduling- Any algorithm	Queue + Smart_Controller	
Scheduling- Preemption	SystemResource	
Memory allocation & deallocation	DRAM (or) CycleAccurateDRAM + Memory_Controller (or) Counter (Memory) + ExpressionList (to check for available memory) + Queue	

Action	Blocks	Example Model
Cache	Cache (or) CycleAccurateCache (or) Memory + ExpressionList (generate hit-ratio and see if it is below a threshold)	
Processor	Processor (See all Processor examples in Block Documentation for different configurations) (or) Traffic (or) Traffic_Reader (Trace file input) (or) SystemResource (or) Server (or) Computer Model	
Thread Management	Queue + Smart_Controller (for coordinating the threads)	
Timer	Server	
I/O and any form of interface	Traffic (or) Transaction_Sequence (or) Traffic_Reader (or) SystemResource	
Multichannel I/O	Server_N_Resource (or) Server (or) Channel	
Fiber Channel	Channel	
Disk	DRAM (or) use Disk Template	
Flash	DRAM + Script (custom controller) (or) Flash template	
Non-blocking switch	Non_Blocking_Switch (or) Server	
Ingress/Egress Ports	Server (for known delay) (or) Queue + Smart_Controller (for	

Action	Blocks	Example Model
	custom arbitration, with traffic management) or SystemResource (for single port)	
SATA	Queue + Smart_Controller	
Arbiter/Scheduler	SystemResource (or) Queue + Smart_Controller	
Manage resource quantity with intelligent data organization on physical media	Quantity_Based_Resource	
Memory (or) Storage (or) Archive	Quantity_Based_Resource	

37.7 Utilities and Functions

Action	Block	Example Model
Fragmenting	While (Requires field to identify each fragment and another field to denote last fragment)	
Defragment	ExpressionList (Look for last fragment field)	
Routing or path selection	Database (lookup or routing)	
Redirect or select a flow	Virtual Connection (IN, OUT, Mux and Demux)	
Goto	Virtual Connection (IN, OUT, Mux and Demux)	
Wait for control to send output	Boolean_Switch	
Manage clock boundary transition	ClockAlign	

Action	Block	Example Model
Manage clock boundary transition and do a calculation before output	ClockAlign	

38 Accelerating Model Simulation Performance

Models in VisualSim can be developed in three ways:

1. You can make the model very verbose. This means that you build the model with many blocks. This allows the user to understand the flows, debugging based on functionality and also for transferring a specification to other team members. This model can have many real-time viewers. This model is not expected to be very fast and speed is not a consideration here. This model is also very quick to develop because all the library blocks are available.
2. Simulation depends greatly on the number of blocks in a model. You can reduce the number of blocks by creating the functionality using Script. These models take much longer to develop because every line has to be analyzed with the profiler to get maximum performance out of the design.
3. Another way to build the model is to use Java or C++ code. Java code is preferred because all the same functions from the GUI are available from the code. C++ is preferred for areas where there is no timing, just functionality.

Below are recommendations to accelerate an existing model.

1. Minimize the number of simulation time events, which can take the form of scheduled events in schedulers or Script block WAIT() or TIMEQ() functions. This has the biggest impact on performance.
2. Minimize the number of blocks, which minimizes the number of port to port events. These events are approximately 60% faster than simulation time events.
3. Reduce the size of the Data Structure by eliminating non-required fields. The number of fields have a direct correlation to simulation. When the data structure is modified or routed to multiple destinations they need to be modified. This has to be done for every transaction and will slowdown the simulation. This problem is very specific to the "ExpressionList", and Script blocks.
4. In the case of processor designs, storing the large instruction array (data structure field 500 to 5000) in a global variable reduces duplication of large arrays. This is faster than appending to the main data structure.

5. Minimize the number of ports added to key blocks. Internally, the simulator must search each port multiple times to determine which ports have tokens.
6. If one knows that the fields have not changed in the Data Structure being passed through the model, then one can add a parameter to the Script called Duplicate_Input, and set it to false. This does not duplicate the incoming Data Structure and improves performance.
7. If one knows the fields have not changed in the Data Structure being passed through the model, then one can add an argument to the Script SEND (output, MyToken, no_dup) function, and it does not duplicate the outgoing Data Structure.
8. In the Script, minimizing the number of statements improves overall performance. Also, the type of statement has an impact. For example, Boolean decisions are faster than statements.
9. In the Script, use of events to trigger the next activity or to initiate an acknowledgment. This is faster than input port processing of a block. If the event arrives via EVENT() before executing WAIT("MyEvent") or TIMEQ("MyEvent") executes, this results in 10X faster performance for this function alone.
10. User can add Profile_File parameter to the Script to see exactly how long a statement takes to execute to further refine the logic, flow. One can see the average time for each instruction, and the number of times it was executed. This can also be used for code coverage investigations.
11. In the Script, consider use of the CLOCK() event, which is like an EVENT(), except the event is only issued if the referenced WAIT() or TIMEQ() has a data structure waiting. Think of this as issuing a clock only if the register equivalent WAIT() or TIMEQ() has some data to be processed. It is a selective event, and improves performance as it does not process non-existing data.

39 Error messages

There are three types of errors in VisualSim.

1. The first is a **Syntax Error** which means that information in the block fields has been entered incorrectly. VisualSim does not allow the user to continue until the error is corrected.
2. The second is a **Run-Time Error** which is identified when the model starts executing. These are the errors that require some basic understanding to detect.
 - a. **Data Type Error**: All blocks have ports that identify the data type at runtime. Some block ports might be assigned a specific data type, typically **Double** or **Boolean**. If a block is pre-assigned a fixed data type, this port type cannot be modified. The data type for the port attached to it must be modified. The port type is modified by right-clicking the block and then selecting "**Configure Port**". The Type can be modified by selecting the appropriate data type from the list.
 - b. **Channel not in range**: This indicates that the input port listed requires to be connected but is currently open. This port is a required port and must have an input for the block to fire.
 - c. **Null**: This is typically the most difficult error to detect. If this occurs for the Display_Fast (Buffered), then simply delete the block, and replace it with a new one. If this is for any other block, this indicates that a port is not connected in the data flow. Look at all the wires and identify the ones that are thin as opposed to fat. This wire will not be connected.
3. The third type of error is an activity in the model that causes an error. For example, the queue may overflow due to the arrival rate being too high. This requires the queue depth to be increased or the input rate to be reduced. These are design consideration errors.

40 Model-level Debugging

VisualSim has a number of graphical and textual debugging built into the environment. In addition, the user can attach third-party code-level debuggers to the environment debugging block level details. You can easily debug your models in VisualSim by using a combination of techniques. The easiest and fastest way to "see" what the model is doing in terms of block execution is to use the visual animation through Model Animation. Next, one can find the Data Structures being sent through the model, using the "**Listen to Port**" feature on any output port in the model.

The key capability available includes:

- **Listen to Port:** All blocks including Class instances, except Hierarchical blocks, support a block context-click the port to select "**Listen to Port**". You have to click the inner-most point of the port to get the Menu. If you need to see the data flowing into and out of a Hierarchical block, you could add a "relation" in front of the port. You can connect a Text_Display to this relation to view the activity.
- **Listen to Block:** All blocks, except Hierarchical blocks and Class instance, support a block context-click to select "**Listen to Block**". If you need to see the details of operation within a Hierarchical block, you need to Open Block and select the block to view the execution details. If you need to view the detailed operation of a Instantiated class, you need to select Open Instance and select the block to view the execution details.
- **Listen to Simulator:** This feature provides a sequence of execution for the selected simulation. This is also integrated with the Digital Debugging utility in the Digital simulator. This window displays the usage statistics, current block execution, and model summary information. From the Debug Menu, select "**Listen to Simulator**".
- **Animated Debugging:** Animate the model by selecting **Debug** > "**Animate Execution**" and specifying a time in ms. Select "**Stop Animation**" to bring the model execution back to the regular mode.
- **Breakpoints:** The model can be stopped by setting a Breakpoint on a block by right-clicking the block and select "**Set Breakpoint**". Refer [40.12 Setting Breakpoints](#).

- **ShowTypes:** Drag and drop this block to see the individual port types. If the port type mismatch, error is generated. This block helps in identifying the non native connection of ports.

40.1 Model Animation

You can animate block diagrams to debug your simulation or simply to view the dynamic operation of the system model. VisualSim animates a model by highlighting the executing block, based on the 'Debug/Animate Execution' time setting (msec). One can also turn off animation by using the main menu bar 'Debug/Stop Animating'. The figure below illustrates Statement_Select Block is currently firing with animation enabled.

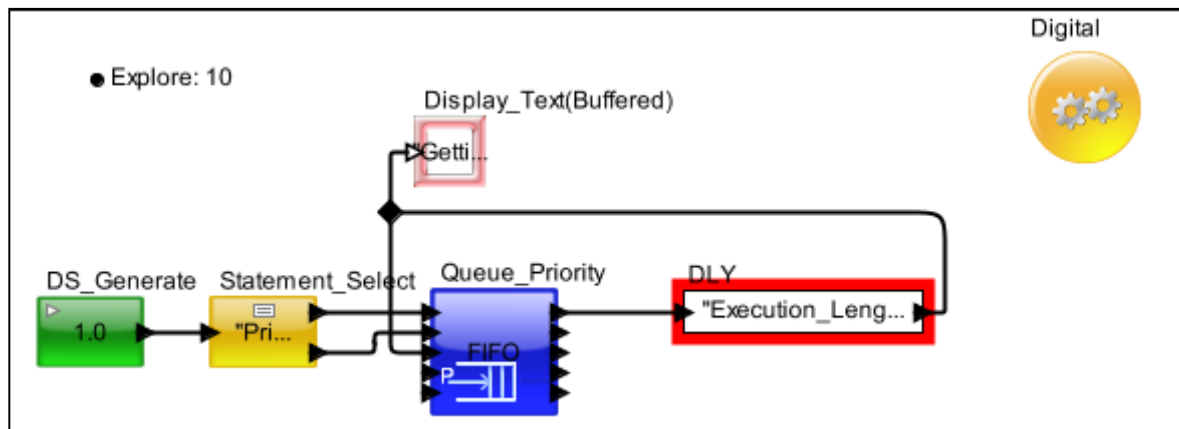


Figure 74. Model Animation

The animation can be paused. At that point, either you can start the simulation, stop the animation or start other debugging operations.

40.2 Probes, Display and Statistics

Operation: Select the display or probe block from the Library palette. Drag the block onto the canvas. Connect the block to the input and output as required in the model.

Explanation: Probes, display, and statistics are provided as extract information from the model during simulation. These blocks can be embedded in the simulation model during construction. These entities will extract the appropriate fields in the data structure or the entire object and display them.

The change in these values can be viewed while the simulation is being executed. Moreover, all the SmartBlocks have built-in statistics gathering.

40.3 Listen to Simulator

Operation: In the menu of the Simulation Cockpit, select the **Listen to Manager** and **Listen to Simulator**.

Explanation: The internal operations of each block and the model, itself, can be viewed by turning on the "Listen to ..". The **Listen to Simulator** records the activities at the simulation kernel level. This records the specific models that are fired and kernel activities for total debugging.

40.4 Listen to Port

"**Listen to Port**" can be enabled in the Block Diagram Editor, simply by right-mouse clicking over the desired port. **Listen to Port** then opens a separate window, identifying the output port location in the top bar of each window. You can open as many "Listen to Port" windows as needed to monitor a simulation. After the simulation is started, each Token passing through a port is displayed in "Listen to Port" window. If the Token type is IntToken, DoubleToken or BooleanToken, then one sees the value. If the Token type is RecordToken or StringToken, then one sees either a simple string, or the Data Structure in an Array. If there is no output on the "Listen to Port" window, make sure the right port was selected, or alternatively this indicates that the model did not generate any output from this block. If there is no output, then one needs to check the ports, or virtual connections, driving this block to see that they are being activated correctly. If the ports driving the block seem to be correct, then experiment with "Listen to Block" on that block.

This feature is not available for Hierarchical blocks. It is supported for regular blocks and instantiated hierarchical classes. If you need to see the data flowing into and out of a Hierarchical block, you could add a "relation" in front of the port. You can connect a Text_Display to this relation to view the activity.

40.5 Listen to Block

"Listen to Block" can be enabled in the Block Diagram Editor, simply by right-mouse clicking the desired block. "Listen to Block" provides more insight into the internal block operation, and may explain why an expected output port did not fire as anticipated. For example, if one is using If_Else Block, and a Data Structure did not appear on the "true" output, then one can view the "If-else" decisions being made internally, simply by performing "Listen to Block". In addition to block level information, "Listen to Block" provides simulator level information relative to methods being fired, and so on. Simulator information is probably most useful for evaluating your custom blocks in the simulation environment.

This feature is not available for Hierarchical and instantiated hierarchical class blocks. If you need to see the details of operation within a Hierarchical block, you need to Open Block and select the block to view the execution details. If you need to view the detailed operation of a Instantiated class, you need to select Open Instance and select the block to view the execution details.

40.6 Script Profiler for the Script block and Smart Controller

The Script Profiler is embedded in the block execution and keeps track of the number of times a statement executes and also the average time the statement took to execute down to the nano-second level. This feature provides all users with the detailed execution information about their script. In addition, it provides the script address, and the script statement associated with that address. If the number of times executed equals 0, then this provides feedback on whether a certain function is even executed. This may be useful information, sometimes referred to as code coverage in lower level verification testing.

Profile_File: The Script Profiler can be turned on by adding a parameter to the Script and Smart_Controller block called "Profile_File". This identifies the name of the file to be generated by the profiler. If the parameter does not exist, or is set to "none", then the Script Profiler is turned off. A typical Profile_File, Block_Name + "_Profiler.txt".

Path:One can place the entire path in "Profile_File" variable, or add the "Path" variable. A typical path, "C:/VisualSim/Profiles".

40.7 Listen to File for Script block and Smart Controller

The Listen to File is a text based version of listen to block.

Listen_to_File: The Listen to File can be turned on by adding a parameter to the Script and Smart_Controller block called “Listen_to_File”. This identifies the name of the file to be generated. If the parameter does not exist, or is set to “none”, then Listen to File is turned off. A typical Listen_to_File value is Block_Name + “_Listen_to_File.txt”.

Path: One can place the entire path in “Listen_to_File” variable, or add the “Path” variable. A typical path is “C:/VisualSim/Listen_to_Files”.

40.8 Debugging Variable

There are two blocks - **Variable_Dump** and **Variable_Monitor** Block for viewing variable content. **Variable_Dump** can generate the value in a variable location when triggered on the input port. The variable name is specified in the parameter and can be a location or the complete list of global, local or block variable. If the default is retained, the complete list of all variables is printed out. The **Variable_Monitor** Block can monitor individual variables by name or by triggering the input port of this block. One can list "all" variable names, values on an output port, each time it is triggered. The Variable_Monitor Block has a parameter entry that one can enter a comma separated list of variable names to monitor as the simulation executes. Each time the list of internal variable names are accessed, read or write, then it will generate a trace Data Structure on its output. The primary difference between the blocks is that the Variable_Dump requires a trigger to generate the variable values while Variable_Monitor will generate the values every time variable is accessed.

One might also use the Read_Variable Block. Each Data Structure triggered on the input gives the current value of the named-variable on its output. You can also have multiple Read_Variable Blocks in the model to read the same variable location. One could "Listen to Port" on the output of Read_Variable to see the variable values as the simulation runs.

Read_Variable block is in **Model >Variables**.



Finally, one might use the IN Block, then you can trigger from any number of OUT blocks within the model, which triggers the IN Block (assumes OUT and IN names match and of same type (local or global)). When the IN Block is triggered it reads the variable parameter name entered (local or global) and sends to its output. Though this block was created for easier plotting, it works equally well for variable monitoring. IN Block can perform conversions, such as integer to double.



IN is in **Defining Flow** -> **IN**.

40.9 Debugging a New Model

If you are debugging a new model, then there are some things you can do while still constructing the model:

- **Workload Generator** -- After adding the workload generator, or trace file that generates composite Data Structures, it might be helpful to test that this portion of the model is generating the necessary workload, using "Listen to Port", or adding a Text_Display Block. This save time later, when more behavioral and architectural blocks are in the model.
- **Hierarchical Block** -- For each hierarchical block used in the model, it might be useful to debug each hierarchical block before adding it to the top level model. To debug a hierarchical block, one needs to add a DE Simulator, possibly disconnect input and output ports, and add a simple traffic generator to test the functionality of the blocks. After debug is completed on the hierarchical block, then one needs to remove the DE Simulator, reconnect the external input and output ports, to use it in the top level system model.

After the top-level system model is constructed that is items (1) and (2) are completed, then one can begin to look at the following items:

- **Data Structure Flow** – The Traffic blocks generate the data structure. To check the correctness of the field values, use "Listen to Port", "Listen to Block", or Display Block at the output of a block.
- **Behavioral, Architectural Processing** -- Now begin to focus on the functionality of the behavioral aspects of the model, the state machines (if any), algorithm validity, and so on. A behavioral portion of a model typically has pure function associated with it, and no delays. To check out the behavioral portion, one can use "Listen to Port", "Listen to Block", or TextDisplay Block to check the Data Structure flow within state machines, protocol, or algorithms. The

architectural aspects of the model can be debugged in terms of Data Structure flow, similar to the behavioral debugging. An architectural portion of a model typically has architectural delay.

VisualSim has a number of debugger features and methodology that simplifies model development and refinement.

40.10 Digital Debugging

This is a graphical editor version of the popular textual debuggers. In the Digital Simulation mode, users can get model summary, the firing order of the blocks and perform step-by-step evaluation of the model. To enable this feature, select **Pause**, **Summary_Only** or **Run** in the **Digital Simulator** icon. If the top-level simulator is enabled, all lower-level simulators must be set to **Off**.

The debug mode can be triggered when the "**DigitalDebuggingExpr**" parameter evaluates to **true**. This parameter is a condition and can contain any **RegEx** function. You can use keywords such as **TNow**, RegEx functions such as "**getBlockStatus**", **global** and **local** (requires the Window name.variable_name) memories and number accesses to a block name.

To view the debugging activity, select **Listen to Simulator** at the current or top-level. The debugging can be turned on at the top-level to view activity for the entire model or can be done at any Hierarchical window.

When the expression evaluates to false, the model continues running as before.

Note: To stop the simulation, while debugging, you need to press Stop and Play/Go twice.

The debugger parameters are:


- **Off**: This disables the debugging mode and is recommended when the model is running in batch mode or when running interactive simulation of a complete model.
- **Pause**: This turns on the debugger to stop at every block in the model flow. The GO button must be selected to continue the simulation after the model stops at each block. Use Listen to Simulator to determine which block is currently being fired. This provides a model summary at the end of the simulation (see Summary_Only).

- **Summary_Only:** At the end of the simulation, this generates a list of all the blocks in this Hierarchy. For each block, the output shows the number of times the block was fired, the average execution time for each firing, and the total time spent in that block. It also lists all blocks that are not used in the model. Some blocks do not get fired by a port. These will show in the inactive list. Example of these blocks are IN, OUT, SystemResource, and Init_variable.
- **Run:** This mode outputs the order in which each block is fired in the model. This provides a model summary at the end of the simulation (see Summary_Only). This does not stop the simulation at every block.

40.11 Debugging Scripts

For small scripts, less than 30 lines, right click the Script block and select Listen to Block. Checkout the RegEx statement during execution. To debug larger scripts, enable the option Single_Cycle and set the block parameter Breakpoint to an expression that evaluates to true. The most common “Breakpoint” expression is `TNow >= 1.0`, or a user simulation time. One can also set the “Breakpoint” expression equal to a specific address, such as

```
TNow >= 1.0 && Address == 10
```

This expression stops on statement 10, if the Simulation time `TNow >= 1.0`. Everytime the Run/Resume Run  is pushed, the next script line executes. In addition, Block_Memories are displayed prior to the execution of each Single_Cycle statement, so one can check out the values.

Before each execution statement in Single_Cycle mode, one can see the following (typical) output:

Block Memories:

```
self_start      : false
port_token      : {BLOCK="Transaction_Source",DELTA=0.0, DS_NAME =
                  "Header_Only",ID=1,INDEX=0,TIME=1.0E-10}
port_name       : input
local_variable  : BEGIN_Thread_Model3.
```

Length : 1
Input : {BLOCK="Transaction_Source",DELTA=0.0,DS_NAME =
"Header_Only",ID=1,INDEX=0,TIME=1.0E-10}
address : 27
Tstop : 10.0
Tresolution : 1.0E-10
Tnow : 1.0E-10
Expression (27) : LABEL: BEGIN
Result : "No Result for Expression"

40.12 Setting Breakpoints

40.12.1 Set Breakpoints context menu choice

The context menu for actors includes a "Set Breakpoints" menu choice.

"Set Breakpoints" is currently only implemented for the Digital and SDF domain. "before iterate" and "after iterate" work with SDF. In the case of the Digital Simulator, you can "Stop on Entry to Block" or "Stop before Executing Timed Activity". After the simulation stops at a breakpoint, you can unselect the breakpoint choice.

The **Set Breakpoints** facility stops the model at a specific point in a specific actor. This is helpful if there are multiple instances of an actor within a model.

- ⇒ Start ModelBuilder from within a debugger
- ⇒ Open an SDF model

Warning: Save your model before running with breakpoints set because saving in the middle of a debugging session may not work.

- ⇒ Right click an actor in an SDF model, select Set Breakpoints > before iterate.
- ⇒ Run the model.
- ⇒ The model stops when it hits the breakpoint.

A message appears in the status bar at the bottom of the ModelBuilder graph display.

The actor with the breakpoint is highlighted in magenta.

⇒ Click **Run** again to continue execution.

40.13 Pause and Resume function with Debugging facility

Pause and Resume function is a debugging and step simulation facility that allows users to specify time stamps to pause simulation and save the simulation data, events and status in a file. The saved model can be restarted from that simulation time. This feature is handy to debug simulations that run for a large period of time. Moreover the user can analyze system behavior at various points in the simulation. The pause and resume function can also be used for debugging. User can pause at a timestamp and analyze the system response and continue simulation step by step from that point onwards. The system can be analyzed for required functionality and also helps the designer to identify if the crucial tasks are being executed within the deadlines.

40.13.1 How to Use Pause and Resume Function

The latest version of Pause and Restart supports the following library blocks - SystemResource, SystemResource_Extend, Server, Queue, Script, ExpressionList, Database, Delay, SingleEvent, Smart Controller, Traffic and File Reader.

The PauseSimulationAt.txt file must be located in the same directory. This file contains the timestamps at which the simulation activity needs to be saved.

Note: The simulation pauses at the closest event after the time value in the PauseSimulationAt.txt file. This means that the simulation may not stop at the exact timestamp.

40.13.2 Steps:

Manual Mode

12. Save your current model.
13. Run Simulation by clicking the green arrow button in the tool bar or press CTRL+R.

14. Pause Simulation by clicking Pause button in tool bar.
15. Click Save As.
16. Select the check box "Save Simulation Data".
17. Give Name for the model with .xml extension
18. Click Ok.
19. .bin file is created in the same directory and this file has the Simulation data.
20. Continue the simulation and repeat the above process to stop the simulation at additional times.

To start the simulation at a specific point,

1. Open the saved file for that simulation point.
2. Model starts running from the time stamp where it was stopped.
3. The model runs to completion, if the PauseSimulationAt.txt file does not exist or the user does not Pause the simulation.

40.14 Testing the RTL

Hardware designs are built to a specification. Due to Clock-based accuracy requirements and the need to migrate the design components from specification to implementation, a VCD writer is provided as a standard block in the library. This block can be used to generate vcd files and the resulting values can be used as the golden reference to validate the implementation. An example is provided in VisualSim to show the application of this block in a real example. The generated vcd file can be viewed by any standard waveform viewer. The generated file can support integer, wire, register, and double.

40.15 How to Debug- Using the methodology provided

40.15.1 INTRODUCTION

Models constructed in VisualSim can help you make better design specification decisions. Evaluations of system specification using VisualSim performance, power and architectural models can help eliminate clearly inferior choices, point out major problem areas, and evaluate a variety of cost, performance and partitioning trade-offs. Simulation is cheaper and faster than building hardware prototypes and can also help with software development, debugging, testing, documentation, and maintenance. This document will provide the information on how the models are debugged. It also explains the various methods of debugging a model.

METHODS TO DEBUG

Animate
Listen to Simulator
Listen to Port
Listen to Block
Tracer

40.15.2 Animate

When there is an error in the model we should identify where the error has occurred, so Animate will help you to trace the path and to capture the block where the error has occurred.

To enable this feature

Go to Debug >> Animate Execution from the menu
Click OK
Then Run the model

Now you can notice the animation over the blocks which helps you to capture the error.

40.15.3 Listen To Simulator

Listen to Simulator will help you to get the detailed analysis on the model. It summarizes the firing order of the block and performs step by step evaluation of the model.

To enable this feature

Go to Configure >> Digital Debugger >> Summary_only in the Digital Simulator
To view the debugging information, select Debug >> Listen to Simulator from the menu.
Then run the model.

This will help you to view the summarized result of the model.

40.15.4 Listen To Port

Listen to Port will help you to find out the incoming/outgoing data of that particular port of the block along with the time, which will be useful for identifying the missing data.

To enable this feature

Right click on the port and select Listen to Port

Then Run the model

The tokens that are sent/received are displayed.

40.15.5 Listen To Block

Listen to Block will help you to get the detailed analysis of the data present in the block at a particular time. It also displays the input and output of that block along with the time. It is basically used for ExpressionList, Script, Smart Controller where it displays the result for each of the statements.

To enable this feature

Right click on the block and select Listen to Block

Then Run the model

The tokens that are present in the block are displayed along with the input and output.

40.15.6 Tracer

The Tracer Block is similar to the Listen To Block feature. When the Tracer Block is instantiated in the model, it captures the information of multiple scripts when they are executed and writes them into a text file. It is used to check the communication between different scripts in the model and also the sequence of execution. It writes into a text file called Trace log.txt in Visualsim. In the Log file we could see what happens when a data structure comes into each of the script blocks and how the execution flows within. This makes debugging easy.

40.15.7 Difficulties in debugging any system and how it is different from debugging a regular piece Java or C/C++ code.

Software systems are complex and debugging is hard. This is especially true for embedded systems where there may be real-time constraints on when data is received or sent, the timing of interrupts, and so on. This means that traditional techniques, such as breakpoints or changing to code to print out state information, cannot be used because they will drastically change the timing and therefore the behavior of the program. Program flow is often controlled by asynchronous and external events, for example inputs from touch sensors and other peripherals whereas while debugging a java code it will be either a compile time error or a run time error. Generally, these two scenarios are encountered :

Syntax error: Consists of grammatical errors or incorrect use of syntax in code.

Logical error: More difficult to rectify as it involves correcting logic in the code itself. The program may still run with a logical error, it will not run with a syntax error though.

This can be fixed by means of traditional techniques such as breakpoints or changing to code to print out state information.

40.15.8 Sequence for debugging

With the help of Display Stack Trace find out the error block.

The animate can also be used to track down the bug in the model so that we can find which block has to be modified.

Perform Listen to port/block at the particular block.

Check for the correct values in the fields

Check the expected order of execution.

Debugging feature used

SCENARIO 1

Click on the Display Stack Trace and check where the error has occurred. In this case it's in the Dynamic_Mapper. It says that the Task_Name is not found, so go to configure and give a unique name in the Task_Name field and then run it again.

SCENARIO 2

Even if the model runs we will get some incorrect output so to rectify that we need to first animate the model while running and then check whether it is traversing through all the blocks if not we need to stop the process and make changes in the block by using Listen to Port/Block. In this model there is a continuous loop in the script so we need to change the script and then run it again.

41 Software Estimation and Modeling

One of the hardest parts of software design is the estimation of task execution times on a target hardware platform. This section provides a step-by-step view of estimation resource utilization at both abstract and micro-architecture levels to achieve the required functionality, performance, and power. Algorithm and embedded software designs utilize MatLab/Simulink, UML or paper document approach. The first two allow for software generation while the third provides for a block diagram with dependencies. Software can be protocol stacks, DSP or communication functions, control operations, and imaging. These tasks can be sequential, control-driven and/or multi-threaded.

41.1 Approaches

There are four major approaches to integrating software with the hardware system:

1. Use a UML model of the code. This is especially useful if you want to parallelize the code. The user can create use case/activity, state chart, and sequence diagrams in VisualSim. Alternately, import directly from a generated xml file.
2. Run the code in a virtual environment and use the statistics in the model. We have built up a complete extractor using an environment called QEMU. The code is a single thread but the resulting model is multi-core/multi-threaded. The integration is available to you for the import. The output looks like this:

```
{InstructionCount = 103414, InstructionCycle = 174792, ICacheHit = 0, ICacheMiss = 0,
DCacheReadHit = 1242, DCacheReadMiss = 942, DCacheWriteHit = 10, DCacheWriteMiss = 74,
DDR_Read = 1016, DDR_Write = 1016, Flash_Read = 0, Flash_Write = 0, LCD_Read = 1938,
LCD_Write = 498, Wifi_Read = 319, Wifi_Write = 591, TouchScreen_Read = 0, TouchScreen_Write
= 0, Audio_Read = 11820, Audio_Write = 11390, Timer_Read = 170, Timer_Write = 33, RTC_Read
= 0, RTC_Write = 0, SimHostTime = 662.208251, SimTargetTime = 635864950, Index = 0,
ioReadCount={48, 0, 0, 170, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 65, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 283}, ioWriteCount={24, 0, 0, 33, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 101, 10, 0, 0, 0, 10, 0, 0, 0,
0, 0, 0, 0, 178}, LdTotal=123176086, LdNonIo=123041475, LdIo=133739, LdDiff=872}
```

3. Generate a profile of the code and then generate random instructions to match the profile. This is very good to stress test the system as it is not just checking one sequence. Rather it is testing for alternate code writing skills.
4. Generate an assembly sequence of the code and run this on our processor block.
5. Run the above virtual environment fully integrated into VisualSim. The core is the virtual platform but the rest of the system is in VisualSim. In this case, no profile is generated. Every request to variable, peripherals or FPGA is sent to the model block in VisualSim.

The software estimation requires two parts - platform model and the software task sequence. The platform model can be constructed in two ways:

41.2 Abstract approach

In this case, the processor and all the peripherals are constructed using the Schedulers, Queues, and Timed Queues. Use time or cycle count estimates of the processing required for each task. The schedulers emulate the mapping of tasks on to a processor. This model can be used for architectural exploration. To accurately measure the software activity, follow the steps below.

- a) If UML or Simulink is used, generate the code from the model. In case of using a paper diagram, Visio or Word, skip to 3.
- b) Break the code into manageable task sizes. A task is something that is between a get from flash and write to flash, or a function like FFT or thread.
- c) Create a software organization including the connectivity, dependencies, and task name. The software organization resembles a UML diagram. The diagram also requires the external dependencies such as gets and puts from sensors, IO, data source, and memories.
- d) The above diagram can be in an Excel spreadsheet and does not need to be graphical. See the example in **Pre-Built Models > VisualSim Domains > Distributed Systems Model** and the associated dependency table.
- e) Annotate the start and end of each task with **GetSystemTime** to print out the time. Make sure you exclude all the gets and puts from this task counter.

- f) Now run this annotate code on the desktop/laptop. Collect the task name, start time, and end time for each task. If the tasks executes multiple times, then take the average to increase the accuracy. This provides the task latency on the Pentium.
- g) Use the above value as your baseline. To match the target processor, compute the ratios of the Pentium vs. the target processor speed and the number of target processor instructions for each Pentium instructions. In VisualSim, create a parameter for the speed and instruction ratios. Now multiple the task latency by these two ratios. For example, if the task took 1 μ S to run on the Pentium and we have a speed ratio of 10.0 and the instruction ratio is 3, the time would be 30 μ s.

The above Software Task Estimation can be used to get the individual time. For each task, create a range around the estimates. For example, rather than saying 30 μ s, go with a distribution of 20-50 μ s.

41.3 Cycle-accurate approach

With this approach, the processor, DSP, and the peripherals are constructed using hardware Architecture library. This model uses a sequence of instructions to execute on the processor pipeline.

There is a C annotation function provided to generate the instruction sequence. Look at the section in this document on C Code Software Annotation. To view the annotation, look at the example file `$VS/demo/HAL/SAR/c/sarsim.c`. Notice how each function has been translated into the equivalent instruction. The list of instructions in the code can be generated by a disassembler that comes with the compiler.

The annotation is only for the executed code and not for the setup and so on, which are not required for the exploration.

Compile this code with the target compiler and execute it on the Pentium or any target machine. If you have a cross-compiler, this is straight-forward. Else, you can easily do an instruction name swap in the annotated output file for your target processor instruction list.

The output files looks like `$VS/demo/HAL/SAR/annotate3.txt`.

This file is used in the model to feed the processor. The instruction sequence is used as in the model **\$VS/demo/HAL/SAR/SAR8.xml**.

If the target processor is a multi-core or multi-processor blade, tasks are executed in parallel. A lot of flexibility is exploring parallel execution, dependency between tasks to prevent certain tasks from getting out-of-order, and so on. If there is a DMA task, then another task can be processed while the current task is **of** getting data or waiting. You can see examples of multi-thread processing in **Pre-Built Models > Hardware Architecture Blocks > Processor**.

41.4 Adding functionality to the timing accurate model

The above approach only focuses on the cycle-accuracy and timing-correctness of the design. In some cases, the timing along with the functionality is required. In those cases, add a combination of Script, CustomC, and processing blocks after the Mapper blocks to model the functionality. The functionality can be setup to execute in synchronous time, thus not affecting the timing performance. For tasks that are currently not available in software or models, the Script can be used to model the functionality. For code that is available, import the C/C++ code directly into a VisualSim model using the CustomC block. Look at the examples in **Pre-Built > Interfaces > Custom C**. These blocks can have any number of input and outputs/return ports. The **CustomC** executes in zero and require all inputs.

41.5 Using QEMU Virtual Environment for system sizing

QEMU is a generic and open source machine emulator and virtualizer.

When used as a machine emulator, QEMU can run OSes and programs made for one machine (for example, an ARM board) on a different machine (for example your own PC). By using dynamic translation, it achieves very good performances.

When used as a virtualizer, QEMU achieves near native performances by executing the guest code directly on the host CPU. QEMU supports virtualization when executing under the Xen hypervisor or using the KVM kernel module in Linux. When using KVM, QEMU can virtualize x86, server and embedded PowerPC, and S390 guests.

You can get more information on Qemu from the Website at <http://www.qemu.org>.

VisualSim uses Qemu to run an application on the target hardware platform and OS, and extract the instruction and cache access. The preferred approach is using a file-based interface. There is a CORBA-based direct interface. The CORBA can be great for a demonstration, though the file-based would be preferred for analysis and investigation. The execution unit of code in QEMU is called as TranslationBlock. The InstructionCycle is calculated for a TranslationBlock.

In this case, the target ARM model has PC (Program Counter). If an execution of code at PC is required, the emulation engine looks at the cache of TranslationBlock. If it is the first time to execute the code at PC, dynamic translation procedure is started. A series of ARM instruction is translated into x86 native binary. At the time, the InstructionCycle is counted for a TranslationBlock and the counted InstructionCycle is recorded. The TranslationBlock is stored in the cache, and the translated x86 code is executed.

In the next time of executing the code at PC, the cached TranslationBlock is used. At that time, the recorded InstructionCycle is used for the statistics.

The android variable map is roughly like this:

0x00000000-0x05afffff AREA1: User memory space 0x05b00000-0x05ffffff AREA2: VRAM(LCD)
0x06000000-0xfeffffff AREA3: Dynamic library (so) memory space 0xff000000-0xffffffff AREA4:
Goldfish HW I/O and Stack memory space from the end.

We separated the memory access by address and counted them.

DDR_Read/Write is a count of AREA1+AREA3.

LCD_Read/Write is a count of AREA2.

ioRead/Write is a count of AREA4.

There are PID (Process ID) information in QEmu execution that can be used to find the dependency between tasks. The purpose is to find "independent task" to execute tasks in parallel. The events have sequence number as the Index field.

42 C Code Software Annotation

42.1 Description

One can annotate existing C Code to generate instructions. It is based on the target processor instruction set which is modeled by the processor. One needs to add a C header file as a **#include** statement, and place the header file in the same folder as your user C code. It is self-contained and has three task related macros, and one macro to close the generated text file.

The macros have the following syntax for a single task:

a) **start_task(file_name,data_structure)**

This macro starts a task based on a **file_name** for the annotated text file and the beginning portion of a **data_structure** used by VisualSim. The **data_structure** is a string version of the beginning of a C struct like token used in VisualSim containing field names and values. For the processor model we use the **Processor_DS**, which is defined in a text file in the "VisualSim/data" folder, see prior description of **Processor_DS**.

b) **append_instr(instructions)**

This macro appends instructions as text into the data structure. First it is defined in macro (1), as elements of a token array and as a field of the **Processor_DS**. The token array then becomes the list of mnemonic instructions that the processor model executes.

c) **last_instr(instruction)**

This is the last instruction for a task and it is essentially closing the data structure as one complete line in the resulting text file. It is based on **file_name** in argument of **start_task**. Typically, the last instruction might be a store type of instruction and its purpose is to complete a task in the final text file.

One can have multiple tasks within a single C code, simply by having multiple **start_task()**, **append_instr()**, and **last_instr()** macros in the same file. They operate sequentially in the specified text file.

d) `close_annotate_file()`

This simply closes the **start_task** file, denoted by **file_name**. It would be added at the end of the annotation, and just closes the text file.

42.2 Step-by-Step

Here are step-by-step actions needed to annotate C code:

1. Add **annotate.h** into the C code folder, so it is in the compiler path.
2. Add to C code an include statement for the **annotate.h** file, here is line #44 of the reference file, sarsim.c:

```
#include "annotate.h" // Mirabilis Design added
```

3. Add **start_task** before AES loop, see line #605 of sarsim.c reference file:

```
start_task("annotate.txt", "{Processor_Name=\"PPC_7410_\", Processor_ID=2  
,  
A_Task_Name=\"FIR\", A_Task_ID=1, A_Priority=0, A_Instruction={"});
```

Suggest just copying this line into your C code and simply change the text for **PPC_7410_ to My_Processor** to describe which processor it will be sent to. Next, one can change the **A_Task_Name** FIR to describe a task more appropriate for the AES algorithm, such as "Byte_Substitution_Table". **Note:** no spaces in data_structure entry.

4. Add **append_task** in the loop itself. **append_task** are the mnemonic instructions the processor will execute in the order appended to the current task. See line #613 of the reference file, sarsim.c:

```
append_instr("\fpu_s_mul.2\", \"fpu_s_add.2\"); // Mirabilis Design  
added  
  
append_instr("\l_s\", \"l_s\"); // Mirabilis Design added
```

The second line is line #617 in the example code, it is placed directly after the C statements, could have been one append line instead of two. One can note that the *.N at the end of the instruction mnemonic can be used for multiple instructions, or array processing, assuming one knows the length of the array. Maybe copy and paste this line and just replace the instruction mnemonic with My_Processor instructions one wants to append. Note: no spaces in the instructions.

5. Finally, add last_instr to close the current task with single, or multiple, instructions. Line #619 of the reference file shows this:

```
last_instr("\l_s\"); // Mirabilis Design added
```

This closes the task with a load/store instruction and is processed by the Processor model as one task.

The items shown in red are all that one needs to modify for a new processor. One can select a subset of the instructions, group the instructions, as long as the mnemonic instruction name matches the Instruction_Set block name when executing the model.

6. At line #778 we close the annotation file, named "annotate.txt" the name given to the annotation file in item (3).

```
close_annotate_file(); // Mirabilis Design added
```

This is all that needs to be added to one's code. If there are DSP-like loops, then the annotation process is simplified.

42.3 Example of Generated Task sent to Processor

An annotated task data structure, defined as a single line of text in the "annotate.txt" file created in the annotation process, might look as follows when sent to the processor, note the A_Instruction sequence of processor mnemonics:

```
{A_Address          = 100,  
A_Branch            = false,  
A_Bytes              = 8,
```

```

A_Bytes_Remaining    = 4,
A_Bytes_Sent         = 4,
A_Command            = "Read",
A_Data               = "MyData",
A_Destination        = "PPC_7410_1",
A_Hop                = "PPC_7410_1",
A_IDX                = 0,
A_Instruction         = {"FPU_s_add", "FPU_s_add", "FPU_s_add", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_add", "FPU_s_add",
"*b", "b", "FPU_s_add", "FPU_s_add", "FPU_s_add", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_add", "FPU_s_add", "*b", "b", "FPU_s_add", "FPU_s_add",
"FPU_s_add", "*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_add", "FPU_s_add", "*b", "b", "FPU_s_add", "FPU_s_add",
"FPU_s_add", "*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_add", "FPU_s_add", "*b", "b", "FPU_s_add", "FPU_s_add",
"FPU_s_add", "*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add", "FPU_s_add", "FPU_s_add", "*b", "b",
"FPU_s_add", "FPU_s_add", "FPU_s_add", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_add", "FPU_s_add", "*b", "b", "FPU_s_add", "FPU_s_add",
"FPU_s_add", "*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",

```

```

"FPU_s_add",    "FPU_s_add",    "*b",    "b",    "FPU_s_add",    "FPU_s_add",
"FPU_s_add",    "*b",    "b",    "FPU_s_add",    "FPU_s_div",    "*b",    "FPU_s_add",
"FPU_s_div",    "*b",    "FPU_s_add",    "FPU_s_add",    "FPU_s_add",    "*b",    "b",
"FPU_s_add",    "FPU_s_add",    "FPU_s_add",    "*b",    "b",    "FPU_s_add",
"FPU_s_div",    "*b",    "FPU_s_add",    "FPU_s_add",    "FPU_s_add",    "*b",    "b",
"FPU_s_add",    "FPU_s_add",    "FPU_s_add",    "*b",    "b",    "FPU_s_add",
"FPU_s_div",    "*b",    "FPU_s_add",    "FPU_s_div",    "*b",    "FPU_s_add",
"FPU_s_div",    "*b",    "FPU_s_add",    "FPU_s_add",    "FPU_s_add",    "*b",    "b",
"FPU_s_add",    "FPU_s_add",    "FPU_s_add",    "*b",    "b",    "FPU_s_add",
"FPU_s_div",    "*b",    "FPU_s_add",    "FPU_s_add",    "FPU_s_add",    "*b",    "b",
"FPU_s_add",    "FPU_s_add",    "FPU_s_add",    "*b",    "b",    "FPU_s_add",
"FPU_s_div",    "*b",    "FPU_s_add",    "FPU_s_div",    "*b",    "FPU_s_add",
"FPU_s_add",    "FPU_s_add",    "*b",    "b",    "FPU_s_add",    "FPU_s_add",
"FPU_s_add",    "*b",    "b",    "FPU_s_add",    "FPU_s_div",    "*b",    "FPU_s_add",
"FPU_s_div",    "*b",    "FPU_s_add",    "FPU_s_div",    "*b",    "FPU_s_add",
"FPU_s_div",    "*b",    "FPU_s_add",    "FPU_s_div",    "*b",    "FPU_s_add",
"FPU_s_add",    "FPU_s_add",    "*b",    "FPU_s_add",    "FPU_s_add",    "FPU_s_add",
"*b",    "b",    "FPU_s_add",    "FPU_s_div",    "*b",    "FPU_s_add",    "FPU_s_add",
"FPU_s_add",    "*b",    "b",    "l_s"}},

```

```

A_Interrupt      = false,
A_Prefetch       = false,
A_Priority       = 0,
A_Proc_Return    = -1,
A_Return         = -1,
A_Source         = "Src",
A_Status         = "Status",

```

```
A_Task_ID           = 1,  
A_Task_Name        = "cdf",  
A_Time             = 0.0,  
A_Variables        = 16,  
BLOCK              = "uEngine",  
DELTA              = 0.0,  
DS_NAME            = "Processor_DS",  
ID                 = 1,  
INDEX              = 0,  
Processor_ID       = 1,  
Processor_Name     = "PPC_7410_1_Instr",  
TIME               = 0.0}
```

Normally, an annotated file contains multiple tasks, especially if the tasks can be processed on more than one processor, or processor core. One just specifies a different target processor in the **start_task** macro. In terms of modeling efficiency, single task instruction sequences in the range of 100 to 1000 mnemonic instructions perform well. However, mnemonic instruction sequences up to 16,000 can be run with some slowdown in simulation performance. Above 16,000 mnemonic instructions per task, the simulator are modeled like the processors. Typically they have difficulty with extremely large arrays. Thus, if one has approximately 1,000,000 instructions to model for a key portion of code, then it might be better to generate multiple tasks of 5,000 to 10,000 each, or 100 to 200 individual tasks. If the processor has a Real-Time Operating System (RTOS), then actually performs a similar large task fragmentation operation, as to not cause other threads, or tasks, to increase their individual latency. The model could perform the large task fragmentation in the model processing of the data structure prior to sending to the target processor, however, fragmenting at the annotation level may be the best all-around approach.

One can process C Code software annotations using the **uEngine** or **LineReader** and the RegEx expression language. Next, one can send the resulting **Data structureTokens** to the Processor block for execution. The concept behind C code software annotations is to provide a simple mechanism, whereby one can insert a couple lines of code into an existing C code file or several, and generate Processor Data Structures (Processor_DS) to run on the Processor block. One has to only annotate the key code flow, or loops, to model the software performance on a processor. The annotation methodology to follow, shows how this can focus the evaluation of the software, whether on a general purpose micro-processor, ASIC, or DSP. The hardware architecture library can model all three and then one can evaluate sending the software tasks to these different resources.

First, one needs to add a file into the folder containing the C code software, named `annotate.h`, and also add the following statement in the specific C code file:

```
#include "annotate.h"                               /** Mirabilis Design added **/
```

This provides most of the code to annotate for the Processor model. There are only four macros that the user needs to use. The first one starts a new task, providing the file name, in this case “`annotate.txt`”, and a text sequence that defines the beginning of a Data structureToken, as a string.

```
/**
```

```
Added by Mirabilis Design, No spaces in start_task entry
```

```
**/
```

```
start_task("annotate.txt", "{Processor_Name=\"PPC_7410_\",Processor_ID=1,A  
_Task_Name=\"cdfc\",A_Task_ID=1,A_Priority=0,A_Instruction={\"});
```

`start_task` is the macro to start a new task, and if desired, the opportunity to save as a separate text file entry. One can set the `Processor_Name` to match the Processor model name, and in the above example, the `Processor_Name` ends with ‘`_`’ so that the `Processor_ID`, the next entry in the Data structureToken, can be appended to the `Processor_Name` for a multi-processor model. In addition, one can set the `Task_Name` to a relevant name for the C code task, so that it can be tracked later in the model. One can also set the priority of the task, when it is sent to the Processor block with the field `A_Priority`, see above.

Some assumptions for the annotation code:

1. Only one `start_task` macro at a time, meaning one file can be opened, and a software task can be generated.
2. To annotate one task that starts and then call a secondary method as a separate task, label the starting task in `start_task`, `append_instr` (see below) to the starting task. Add `last_inst` (see below), prior to `start_task` for secondary method. When the secondary task completes, then restart the initial task with the same task name. This generatea three tasks for one higher level task and a secondary task.
3. The C code annotation macros are suited for loops to correctly generate the proper number of instructions.
4. C code annotations can also be used for if-else flow, dependent on internal method arguments or C variables.

Next, one can append an instruction to the `start_task` macro, by adding this macro in the C code flow:

```
append_instr("\FPU_s_add\", \FPU_s_div\", \b\");
```

In this case, the instruction names correspond to `FPU_s_add` and `FPU_s_div`, which also appear in the Processor instructions, found in the `Instruction_Set` block. The names should match. The escape character plus double quote `\` is necessary to interpret the entire line written into the `annotate.txt` file properly to generate a `Data structureToken`. In other words, it is best to just copy each macro instruction, as shown and modify only the instruction names, the syntax is preserved.

Once, all of the instructions have been appended for this example task, “`cdft`”, then a third macro completes the annotated task:

```
last_instr("\l_s\"); // Mirabilis Design added last instruction
```

In the above case, “`l_s`” is an instruction, load-store, that is appended to the end of the annotation. Finally, the fourth macro closes the annotation file:

```
close_annotate_file(); // Mirabilis Design close annotation file
```

If this method is not called, the annotation file should still be generated, so more for the multi-annotation file case, if used. The C code annotation macros might look like the following for a typical loop in C code:

```

/**
Added by Mirabilis Design, No spaces in start_task entry
**/
start_task("annotate2.txt", "{Processor_Name=\"PPC_7410_\", Processor_ID=1,
A_Task_Name=\"EQ_Taylor_Weighting\", A_Task_ID=1, A_Priority=0, A_Instructio
n={"});

for(i=0; i<NCSAMPLES-niq; i++)
{
    cmult(cbuf[j+NPULSE][i], cbuf[j+NPULSE][i], w[i]);

    append_instr("\"vpu_fp\", \"*b\"); // Mirabilis annotation
}

last_instr("\"l_s\"); // Mirabilis annotation

```

Use a LineReader plus Expression block to read the annotated file. The model looks similar to the following:

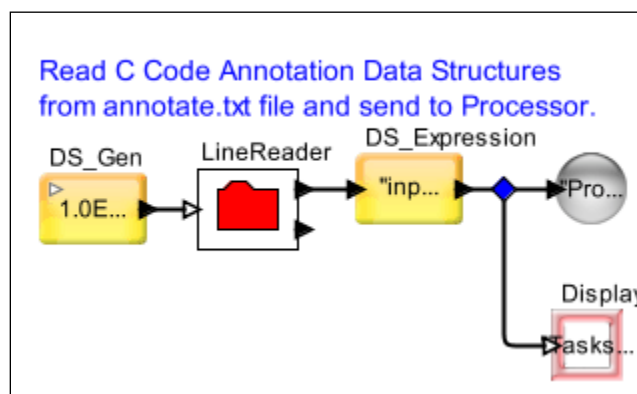


Figure 75. Annotation with LineReader plus Processing block

The Expression block contains the following statements :

```



```

In essence, one can create a `newData structureToken` in the `RegEx` language, whether a string

`{a=1, b=2}`, or by name, such as `"Processor_DS"`. These are the added `RegEx` methods:

```

Public static Token cast(StringToken token)
{ ... }

public static Data structureToken newData structureToken(String
token_name_)
{ ... }

public static Data structureToken newData structureToken(StringToken
string_token_)
{ ... }

```

The generated Data Structures from the annotation process looks as follows:

```

send to channel 0: {A_Address  = 100,
A_Branch          = false,
A_Bytes           = 8,
A_Bytes_Remaining = 4,
A_Bytes_Sent      = 4,
A_Command         = "Read",

```

```

A_Data                = "MyData",
A_Destination         = "PPC_7410_1",
A_Hop                 = "PPC_7410_1",
A_IDX                 = 0,
A_Instruction         = {"FPU_s_add.3", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b",
"FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3",
"*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b",
"FPU_s_add.3", "*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3",
"*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div",
"*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b",
"FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3",
"*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b",
"FPU_s_add.3", "*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3",
"*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div",

```


"FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b",
"b", "FPU_s_add.3", "*b", "b", "FPU_s_add", "FPU_s_div", "*b",
"FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3",
"*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div",
"*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b",
"FPU_s_add.3", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add", "FPU_s_div",
"*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b",
"b", "FPU_s_add.3", "*b", "b", "FPU_s_add", "FPU_s_div", "*b",
"FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3",
"*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div",


```
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3",
"*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div",
"*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b",
"FPU_s_add.3", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add", "FPU_s_div",
"*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b",
"b", "FPU_s_add.3", "*b", "b", "FPU_s_add", "FPU_s_div", "*b",
"FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3",
"*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div",
"*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div", "*b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "FPU_s_add.3", "*b",
"b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b",
"FPU_s_add.3", "*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add",
"FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3", "*b", "b",
"FPU_s_add", "FPU_s_div", "*b", "FPU_s_add.3", "*b", "b", "FPU_s_add.3",
"*b", "b", "FPU_s_add", "FPU_s_div", "*b", "FPU_s_add", "FPU_s_div",
"*b", "FPU_s_add", "FPU_s_div", "*b"},
```

```
A_Interrupt      = false,  
A_Prefetch      = false,  
A_Priority      = 0,  
A_Proc_Return   = -1,  
A_Return        = -1,  
A_Source        = "Src",  
A_Status        = "Status",  
A_Task_ID       = 1,  
A_Task_Name     = "cdfc",  
A_Time          = 0.0,  
A_Variables     = 16,  
BLOCK           = "One",  
DELTA           = 0.0,  
DS_NAME         = "Processor_DS",  
ID              = 0,  
INDEX           = 0,  
Processor_ID    = 1,  
Processor_Name  = "PPC_7410_1_Instr",  
TIME            = 0.0}
```

The annotate.h file contains the following macros:

```
/*=====
```

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Support code for annotating C code.

```

=====*/
/* $Id: annotate.h,v 1.0 2007/10/23 koivisto Exp koivisto $ */
/**
$Log: annotate.h,v $
*
* Revision 1.0 2007/10/23 koivisto
* Initial revision
*
**/

#ifndef __annotate_h
#define __annotate_h

#include <stdio.h>
#include <string.h>
#include <errno.h>

/**
File Values
**/

FILE *f;
int sample_count = 0;
int task_count = 0;
char current_task[512];
char temp[2048];

#define max_samples 512 // Maximum Annotated Task Size, All Instructions Processed
#define max_tasks 50 // Maximum Task Count
#define start_task(file_name,data_structure) { if (f == NULL) f = fopen((file_name), "w"); \
strncpy(current_task, data_structure);
\
if (task_count < max_tasks) fprintf(f, "%s", current_task); }
#define append_instr(instructions) { ++sample_count; \
strncpy(temp, instructions); \
if (sample_count < max_samples && task_count < \
max_tasks) strcat(temp, ","); \
if (sample_count >= max_samples && task_count < \
max_tasks) strcat(temp, "}}\n"); \
if (sample_count >= max_samples && task_count <

```

```
        max_tasks) strcat(temp, current_task); \  
if (sample_count >= max_samples && task_count <  
    max_tasks) sample_count = 0; \  
if (task_count < max_tasks) fprintf(f, "%s", temp); }  
  
#define last_instr(instruction)    { strcpy(temp, instruction); \  
    strcat(temp, "}}\n");          \  
if (task_count < max_tasks) fprintf(f, "%s", temp); \  
sample_count = 0;                 \  
++task_count;                     }  
  
#define close_annotate_file() { fclose(f); f = NULL; task_count = max_tasks; }  
  
#endif                             /* !__annotate_h */
```

43 Concept of Time

43.1 Introduction

The **Simulator** controls the concept of time and the advancement of the simulations schedule. As VisualSim is a multi-domain simulator, the time is synchronized across multiple simulations. Some Simulators such as the un-timed digital have no concept of time. These Simulators move the data token from one output port to the next input port.

During model initialization, a topology map of the entire model is constructed. Each **Hierarchical** block can contain a **Simulator** icon instance. This partitions the model structure for the local simulators to handle the processing and the master simulator to manage the central communication and the **Master Clock**. For time-based **Simulators** such as **Discrete-event Simulator**, it is important to add a **Simulator** icon to each level of the Hierarchy for large models. This keeps the events occurring at that level of hierarchy local and maintains a smaller calendar of events, thus increasing simulation performance.

Sub-models or classes must always have a Simulator instantiated in them.

43.2 Time Resolution

Time Resolution of the **Simulator** is provided as an attribute of the **Simulator** icon. This is a **double** value which defaults to **1.0e-12**. The **Time Resolution** of the **Simulator** must be smaller than the smallest delay in the model. **Zero** is not a possible value. If the smallest time in your model is **0.1** ns, then the **Time Resolution** must be smaller than **0.05** ns. The Time Resolution is used to resolve any contention occurring at the same time.

Note: If you have identical results for different time resolutions, the time resolution must always be of the form $1.0e(x)$ which x is a positive or negative integer. The time resolution cannot be $0.5e-11$ or something similar. It must always be $1.0e(x)$.

Blocks in different levels of the hierarchy or even within the same hierarchy can be fired in synchronous time. This means that there is no advance in time between the individual firing. This is

called concurrent operation. In real life this would be a processor which is acting on instructions in two **Execution Units**, while another **Execution Unit** is waiting for a **Cache** access.

43.3 Simulation Time

The simulation time depends on the number of events in the model and the time resolution. The StopTime in the Continuous and Digital simulator depend on the time resolution. The largest simulation time can be derived using the following formula:

$$\text{TimeResolution} = 1.0\text{e-}12$$

$$\text{Bits} = \text{floor}(-1 * \log_2(\text{TimeResolution})) + 1 = 40.0$$

$$\text{maximumGain} = 52 - \text{Bits} = 12$$

$$\text{stopTime} = 0.90 * \text{pow}(2.0, \text{maximumGain}) = 3686.4$$

The simulation stops at this point and any remaining events are not completed.

If all the activities in the model finish prior to the StopTime and there are no more items remaining, the clock simply jumps to the StopTime and the simulation ends.

43.4 Relative vs Clock Time

The **Digital Simulator** operates on “Relative Time” and “Clocks”. In Relative Time, time advances in the model using a delay value. The delay value has a base of seconds. If the model is clock-driven, there are inherent clock cycles and clock edges. This means that every block in the model is synchronized to a clock and fires at the clock edge. Models can be a combination of clock and Relative Time.

43.5 Computing Time

One unit of time is one second and one unit of data size is one byte. One nanosecond is denoted by 1.0e-9 while, 8 bits is denoted as 1 byte. The clock generated and any math calculations can be accurate to a resolution of **1.0e-14**. So, the clock generated can be at least as accurate as the hardware clock.

Values are stored in VisualSim at a resolution of 1.0e-20. Calculations are performed at the accuracy of 1.0e-14. When you use a time value in any delay block, the expression is first calculated with the

calculation accuracy and then rounded to time resolution. If you are using multiple of a clock value for the delay, it is best to create another clock with the required value.

For example, the time resolution is $1.0e-13$. $1.0e-13$ is the resolution of the number inside the WAIT(x) statement or Delay block. x is rounded internally according to time resolution to be used by WAIT(x).

The value of x in other parts of the model has the original resolution of $1.0e-14$. When x is multiplied with N, and the $N*x$ is used inside WAIT($N*x$), the result $N*x$ is rounded again according to $1.0e-13$. But in the calculation of $N*x$, the resolution is $1.0e-14$.

43.6 Clock Synchronization

The WAIT (time) and TIMEQ function in the Script support clock synchronization for an integer and long value. If the time value is a double, then the simulator is delayed by this value. If the WAIT() uses an integer, then the value is treated as a clock speed. This means that function will delay to the clock boundary. For example, if the value is 1000000. This is considered as the speed of the clock in hertz. In this case, the delay value is $(1.0/1000000)$ or $1.0e-6$ or 1 micro-second. The use of an integer or long value as the clock value in Hertz for the WAIT() or TIMEQ() delay argument causes the statement to execute at exactly the clock rate based on the simulation time. There is no need to perform any other clock synchronization.

43.7 Model Event

A Model Event is similar to a time event, except generated by the user, and can occur at any time between blocks. In other words, a model condition triggers a Model Event for synchronizing between blocks, or within clock-driven processes. The most common use is to generate clocks from a single block to multiple blocks that are waiting for a clock event. Model Events can be generated from any RegEx block using the following RegEx function:

```
newEvent ("MyEvent")
```

The argument of newEvent must evaluate to a string name. The string argument can be composed of newEvent(MyParameter + "_MyEvent") notation for events inside a hierarchical block. This function can be applied in ExpressionList, Script or Smart_Controller Blocks. The Script and

Smart_Controller blocks also support the following syntax which executes locally in the Script or Smart_Controller block.

```
EVENT ("MyEvent")
```

This notation is preferred over the **newEvent()** RegEx notation, for faster execution. In a corresponding Script or Smart_Controller block, the user needs a matching syntax as follows:

```
WAIT ("MyEvent")
```

This statement continues processing on the next statement after it receives a newEvent() or EVENT(). If the newEvent() or EVENT() is generated before the WAIT() on event, characterized as a string argument, then the WAIT() immediately goes to the next statement. Finally, if two newEvent()s or EVENT()s are generated prior to a WAIT ("MyEvent") only one will execute similar to an 'OR' of pending events. This is done to prevent the unintentional build up of events in a model that may not execute as expected.

44 Introduction to Finite State Machine

Finite State Machines (FSM's) are used extensively in designing sequential control logic. FSM is a very intuitive way to capture control logic and easier to communicate a design. The VisualSim philosophy of hierarchical composition of heterogeneous models of computation allows embedding hierarchical FSMs within a variety of concurrency models. FSM model is contained by an instance of FSM Block. The FSM model reacts to inputs of the FSM block by making state transitions. Actions such as sending tokens to the output ports of the FSM block can be associated with state transitions.

For a detailed explanation on the VisualSim Finite State Machine usage and Simulator, visit the [Chapter 4- Simulator Documentation](#) Chapter on FSM.

Expressions give the guards for state transitions, as well as the values used in actions that produce outputs and actions. This sets the values of parameters in the refinements of destination states. The exceptions are parameters that are strictly string parameters, in which case the value of the parameter is the literal string, not the string interpreted as an expression, as for example the *function* parameter of the *TrigFunction* actor, which can take on only "sin," "cos," "tan", "asin", "acos", and "atan" as values.

44.1 Finite State Machine

44.1.1 FSM-Controller

The FSM Block contains states and transitions. The State has two ports: incomingPort, which links to incoming transitions to the state, and outgoingPort, which links to transitions going out from the state. The Transition links to two ports - the outgoing port of its source state and the incoming port of its destination state. The two ports of the States are not displayed on the circle.

44.1.2 Guard Expressions

The guard of a transition is specified by its guardExpression string attribute. Guard expressions are parsed and evaluated using the RegEx expression language. Guard expressions must evaluate to a Boolean value. A transition is enabled if its guard expression evaluates to true. Parameters of the FSM block and input variables (defined below) can be used in guard expressions. Input variables represent the status and input value for each input port of the FSM block.

44.1.3 Actions

A transition can have a set of actions that produce output tokens or set parameters of the FSM block. A transition has an outputActions attribute and allows the user to specify a list of semicolon separated output actions of the form destination = expression. The expression can use parameters of the FSM block and input variables.

44.2 Execution

The methods that define the execution of an FSM block are implemented as follows:

Preinitialize: Create receivers and input variables for each input port; set current state to the initial state as specified by the initialStateName attribute.

Initialize: perform simulator-specific initialization by calling the initialize (Block) method of the Simulator. Note that in the example given in AMI Coder of the Simulation Domain documentation under FSM, the Simulator is the Untimed Digital Simulator.

Prefire: always return true. An FSM block is always ready to fire.

Fire: set the values of input variables; choose the enabled transition among the outgoing transitions of the current state; execute the choice actions of the chosen transition.

Postfire: execute the commit actions of the last chosen transition; change state to the destination state of that transition.

Non-deterministic FSMs are currently not allowed. The fire() method checks whether there is more than one enabled transition from the current state. An exception is thrown if there are more than one

transition from any state. In the case when there is no enabled transition, the FSM will stay in its current state.

44.3 FiniteStateMachine

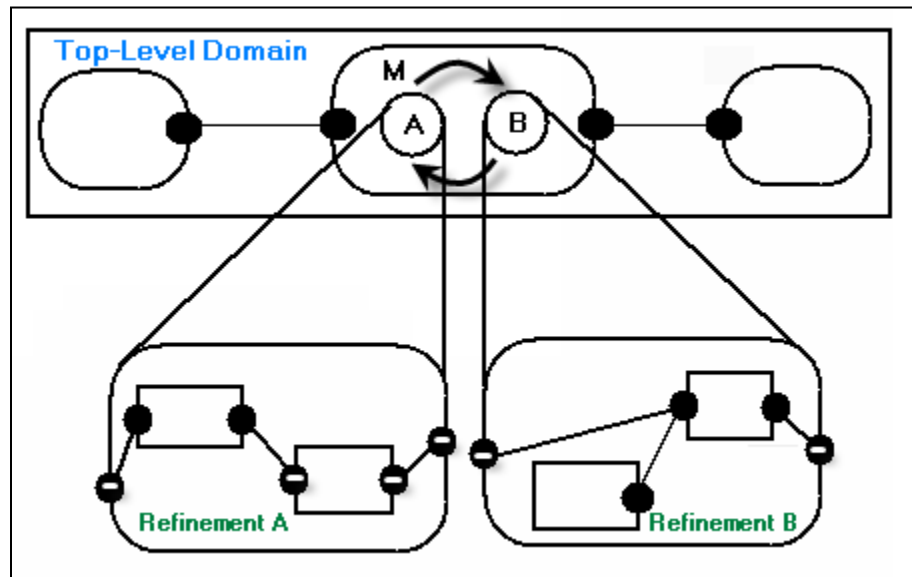


Figure 76. FiniteStateMachine Illustration

The FSM simulator supports the *charts formalism with modal models. The concept of modal model is illustrated in Figure 76. M is a modal model with two operation modes. The modes are represented by states of FSM that controls mode switching. Each mode has a refinement that specifies the behavior of the mode. In VisualSim, a FiniteStateMachine is an entity in the Base Blocks and uses the FSM simulator internally. The refinement in the States and the Transitions can either be another FSM or a Block Diagram.

45 Explorer, Export to HTML and HTML Page Generation

Explorer enables the user to share the models with non-VisualSim Architect users through the Web Browser. To use this capability, the user must purchase and install the optional VisualSim Explorer. Instructions for installing and configuring VisualSim Explorer are described in the [Installation Guide](#) document and on the [VisualSim software download](#) page (password-protected).

The model and simulation views are embedded in an html page as an Applet.

The following steps must be followed to prepare the model to execute in the Browser.

1. Prepare the configuration file- webExport.Properties
 2. Export to Web
 3. Edit generated jnlp file
- **webExport.Properties**
Configurations are performed in webExport.Properties file in <VisualSim Install Directory>/VS_AR/VisualSim/WebExport/template directory.
 - Codebase- Root of Explorer install directory. At Mirabilis Design, this is:
codebase= http://mirabilisdesign.com/new/VisualSimjnlp
 - webRootDir- Unchanged for now
 - All other items must be set to the default values
 - **Export to Web**
 - To use this capability, open the model to be exported in the BDE and select **File → Export → Export To Web**.

Note: The model name must not contain a space.

A window will popup and will contain the definition for the export.

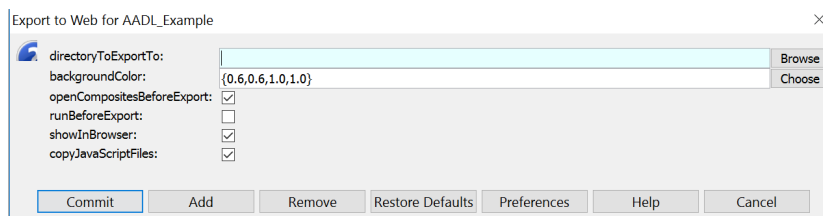


Figure 77. Export to Web Dialog Window

- directoryToExportTo. This will be the directory that will contain the model on the Web
- Select openCompositesBeforeExplor, showInBrowser and copyJavaScriptFiles.
- Do not select runBeforeExport. This is a future feature.

Select Commit and html, jnlp, javascript and the model will be saved in a sub-directory with the name of the models. The Top directory must be copied to the Explorer root.

- **Edit the jnlp file**

The first and last line of the generated model_name.jnlp must be edited. This is a required step.

Let us say that the top-line of the model_name.jnlp is as follows:

```
<jnlp codebase="http://mirabilisdesign.com/new/VisualSimjnlp"  
href="../../../VisualSim/CModel/User_Library/AADL_Video/AADL_Example/AADL_Example.jnlp">
```

Say the top directory is /AADL_Video/ and the file must be located at

<http://mirabilisdesign.com/new/VisualSimjnlp> . Then the href will look as follows:

```
href="../../VisualSimjnlp/AADL_Video/AADL_Example/AADL_Example.jnlp">
```

To start the model in the Explorer, point the Browser to

```
http://mirabilisdesign.com/new/VisualSimjnlp/AADL\_Video/AADL\_Example/AADL\_Example.html
```

The model opens on the page. The user can mouse-over any block to view the parameter definition and the values. The hierarchical blocks can be opened by clicking on the block.

To run the model from your web browser click on Launch button and click OK to execute the jnlp file.

This will open the model from within the Web Browser. The first time, the jar files will load up and will take about 30 seconds. After that the execution will be instant.

The user can customize the html page using any popular Web Page Editor. At Mirabilis Design, we use the Mozilla free editor called Kompozer (<http://kompozer.sourceforge.net/>). To this page, the user can add additional explanations, specification of the products, and other required images.

46 VisualSim® Interface with FPGA

We describe the integration of the VisualSim modeling environment with FPGA-in-the-loop. Here we have considered Xilinx Zynq 7000 platform board as the example device that communicates with VisualSim®. However the source code and the setup is completely generic. This interface has been demonstrated on Xilinx Zynq 7000 platform board (Zybo board), using the Vivado tool suite from Xilinx and the accompanying Xilinx SDK. The version of Xilinx tool used is Vivado 10.2.

Using this interface the designer can communicate in both direction between VisualSim and the FPGA boards.

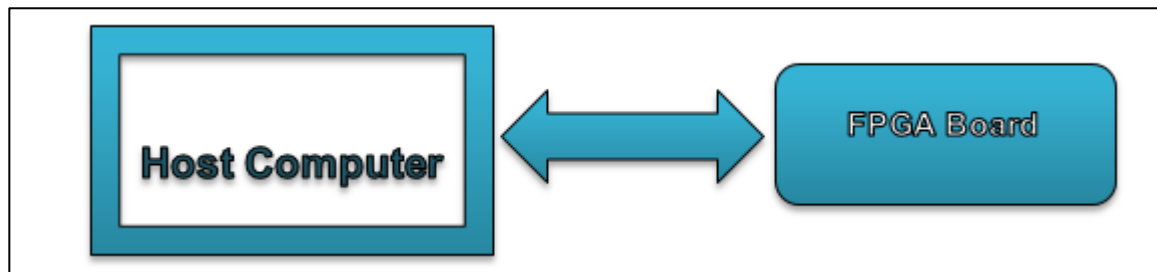


Figure 78. VisualSim Interface with FPGA

46.1 VisualSim FPGA Interface applications

VisualSim FPGA Interface can be used for System level analysis of Embedded Systems including performance, protocol checking, power, and for generating test scenarios for the target FPGA.

VisualSim can generate verities of test scenarios very quickly and enables the user to validate application on FPGA covering all corner cases.

VisualSim FPGA interface allows users to adopt below mentioned applications but it is not restricted.

- Generating and running system level scenarios
 - VisualSim can be used to generate system level scenarios from the system definition.
 - Transferring the data to the FPGA to run actual data through the system.
 - Transfer the data back to VisualSim to perform analysis and display the information in user readable format.
- Run performance simulations on the actual hardware system
 - VisualSim to generate complex use case scenarios that define performance bottle necks.

- Run these scenarios on the actual hardware system.
- Collect process and display the results, so system level optimizations can be performed.
- Run power scenarios on the actual hardware
 - Generate complex power scenarios for the system.
 - Run these scenarios on the actual hardware.
 - Collect process and display the results, so system issues can be identified and fixed.

46.2 Hardware and Software Requirements

The FPGA must have a microprocessor, Ethernet Port and a Ethernet MAC core on the device. Example Hardware and Softwares are as follows; Xilinx Zynq 7000, SmartFusion2, Xilinx Vivado.

46.3 VisualSim FPGA Interface Kit

VisualSim FPGA Interface Kit provides all the interface files and demo examples. As VisualSim FPGA Interface Kit is provided as completely configurable, users can compile the interface based on their requirements.

46.4 How Interface Works

The Zynq platform has an ARM processor and an FPGA as part of its architecture. This interface uses the ARM processor to enable the interface, so the users can use all of the FPGA for their logic, except for a small layer to communicate with the interface.

The software running on the ARM processor is a lwIP Echo Server. The lwIP Echo server application starts an echo server at port 7. Any data sent to this port is accepted by the FPGA, processed by the FPGA and sent back through this interface.

By default, the program assigns the following settings to the board:

IP Address: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
MAC address: 00:0a:35:00:01:02

These settings can be changed in the file main.c.

platform.c implements processor and platform dependent functions.

The file `platform_config.h` is generated based on the hardware design. It makes two assumptions: The timer has its interrupt line connected to the interrupt controller, and all the Ethernet peripherals (`xps_ethernetlite` or `xps_ll_temac`) accessible from the processor can be used with lwIP.

46.4.1 Procedure to Run Example

- Import the Vivado project into the Vivado tool suite.
- Make the required changes to the project to suit the hardware being used for the demo.
- Compile the project in Vivado.
- Launch the SDK from Vivado, so all the required board support packages are exported to the SDK.
- Import the SDK project into the SDK.
- Make the required changes in the SDK to match the paths of the new packages that were generated for the board being used.
- Compile the software.
- Program the FPGA with the generated bit stream.
- Then launch the software to run on the FPGA and monitor using a telnet from the host PC.

To communicate with FPGA, VisualSim uses UDP socket ports and the user can send packet data from VisualSim to FPGA using VisualSim's "Datagram Writer" library block and receives packet from FPGA using "Datagram Reader" library block. Sample VisualSim model and configuration of Datagram Writer and Datagram Reader is shown in below figure.

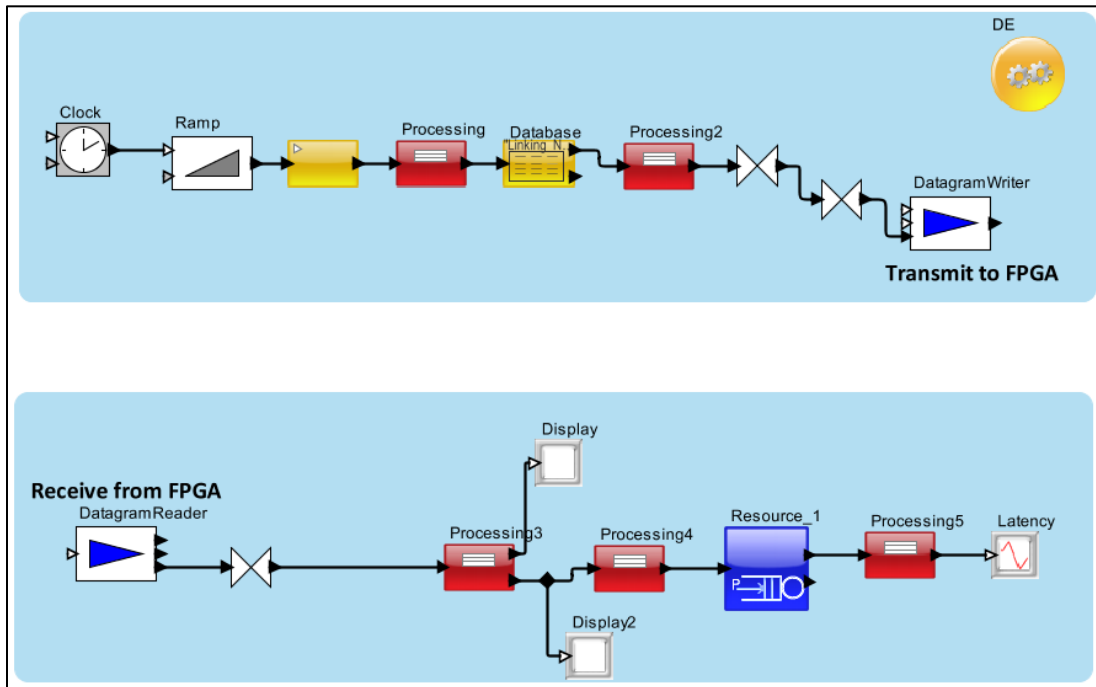


Figure 79. VisualSim Model

VisualSim Datagram Writer and Datagram Reader play a very important role in VisualSim FPGA interface. Datagram Writer and Datagram Reader should be configured with right Socket number and Remote/Local address.

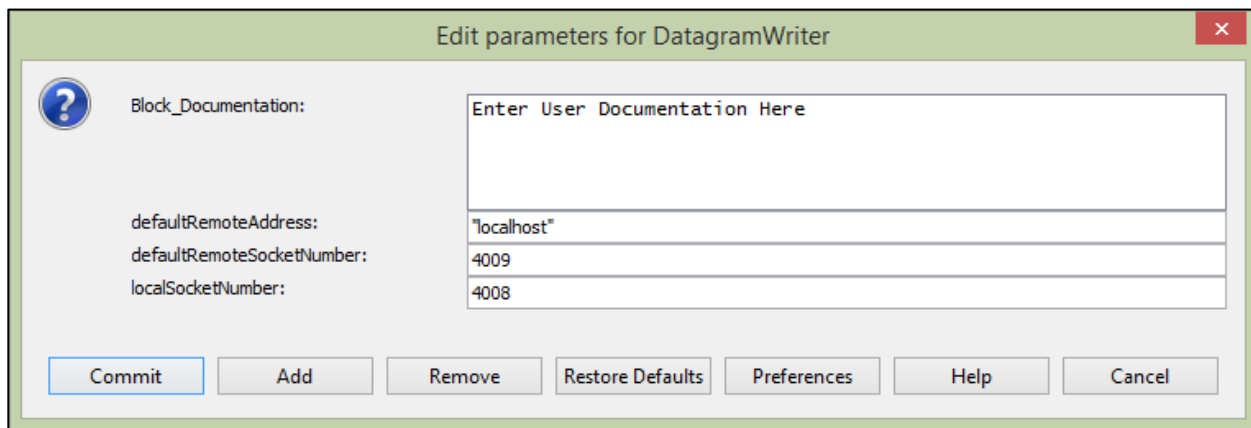


Figure 80. Configuring Datagram Writer block

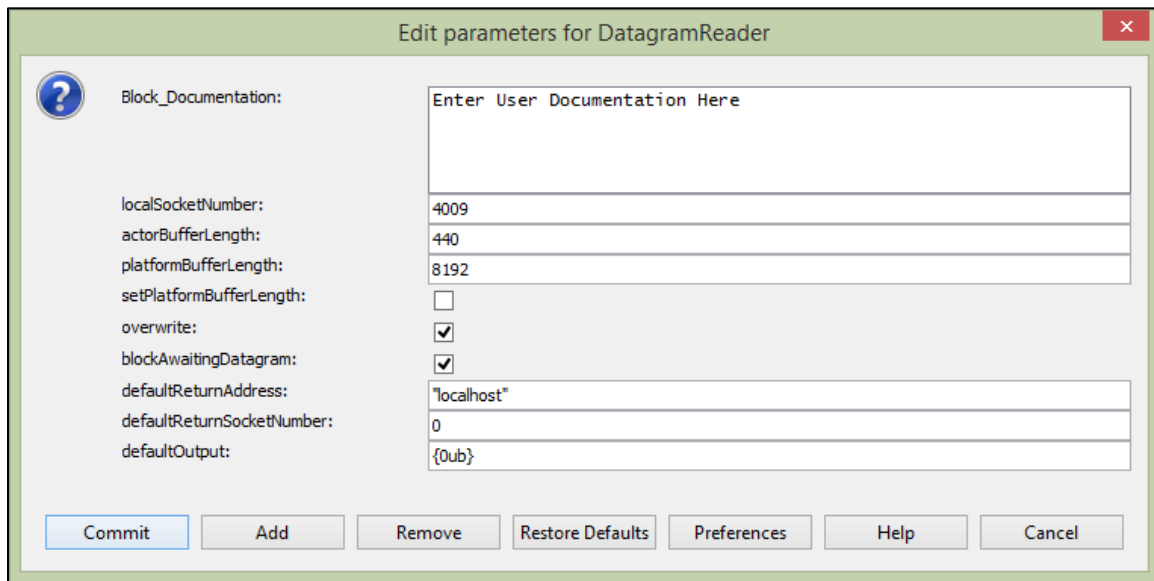


Figure 81. Configuring Datagram Reader

The blocks connected after Datagram Reader correspond to the subsystems that are connected to FPGA platform and does processing based on the data from FPGA. In this example, we have connected a Server that models a simple buffer and it delays the incoming data based on the data size and buffer speed MHz.

46.5 Configuring FPGA and Source Files

We have created a sample Vivado project that works with VisualSim. Import the Vivado project into Xilinx Vivado tool suite. To Import the project, please click on **File > Open Project** and select **mirab_eth.xpr** and **click Ok**. Now the project has been loaded into Vivado design suite.

Now we need to generate bit stream for programming FPGA. Click on Run Implementation from the menu bar **Flow > Run Implementation** or click on the green arrow button on the tool bar.

After successful Implementation Run, generate bit stream by selecting Generate Bitstream Option as shown below.

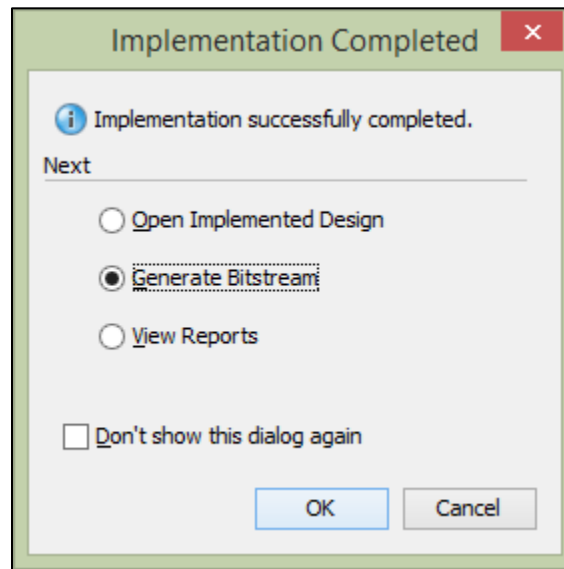


Figure 82. Generate Bitstream

After successful Bitstream generation, we need to export hardware description file for SDK. To perform this, click on **File → Export Hardware**. As the original project was compiled using Vivado 10.2, users with latest version of Vivado need to upgrade IP and generate a new block diagram. Refer appendix 1 for more details on updating IP and block diagram generation.

When you click on **Export Hardware**, Vivado Suite will open as if you want to generate output products or to Skip generation of output products.

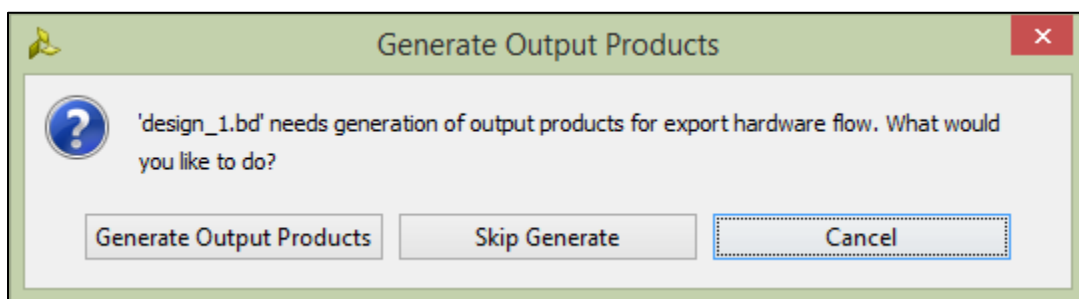


Figure 83. Generate Bitstream

Click Generate output Products.

After generating output products for hardware, select the export location as local to project.

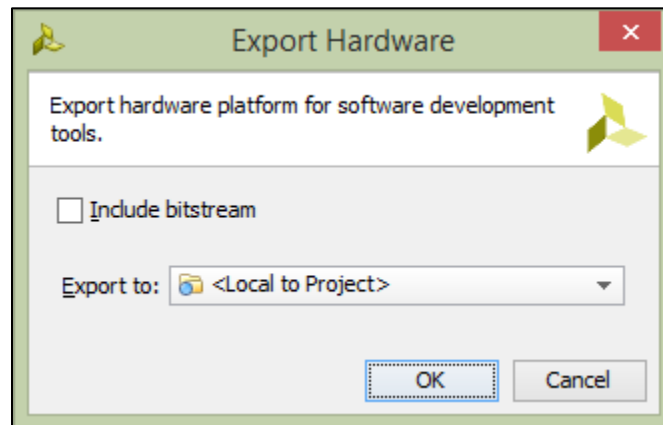


Figure 84. Export Hardware

Click OK.

Now we need to launch Xilinx SDK. Make sure that you have installed Xilinx SDK package during installation procedure.

As we need all the board support packages in SDK, launch Xilinx SDK from Vivado Design suite. Click on **File > Launch SDK**. This opens Xilinx SDK, make the required changes in the SDK to match the paths of the new packages that were generated for the board being used. By default you can select the exported location as Local to project as shown below.

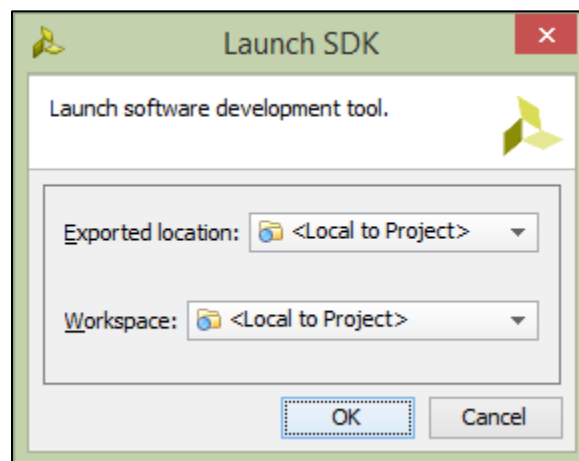


Figure 85. Launch SDK

Click on Ok.

The source files are listed under TestApp1, select TestApp1 in Project Explorer as shown below.

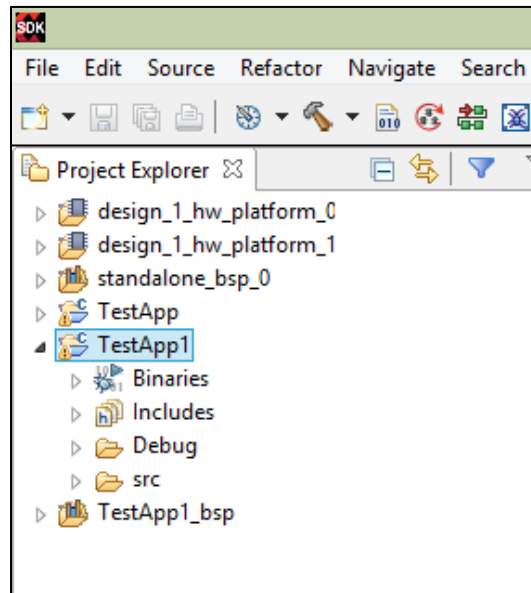


Figure 86. Project Explorer

To compile source file, click the Run menu from the Menu bar or Run button on the Tool Bar. Now program the FPGA with the generated bitstream by clicking on **Tools > Program Device**. Launch the software to run on the FPGA and monitor using a telnet from the host PC.

46.6 Possible Errors

1. Failed to create a new socket on port {Port Number}.
Solution: This error appears if the Datagram Writer local socket number and Datagram. Reader local socket number are same. Make sure that both are different.
2. Blank Report display.
Solution: This is due to incorrect remote address/IP address or Remote socket number defined in Datagram Writer.

46.7 Appendix

1. For the users with Vivado design suite above 10.2, follow the steps mentioned below to upgrade IP and to generate new block diagram.

If you are running Vivado design suite above 10.2 you may receive a message as mentioned below while performing **Export Hardware**.

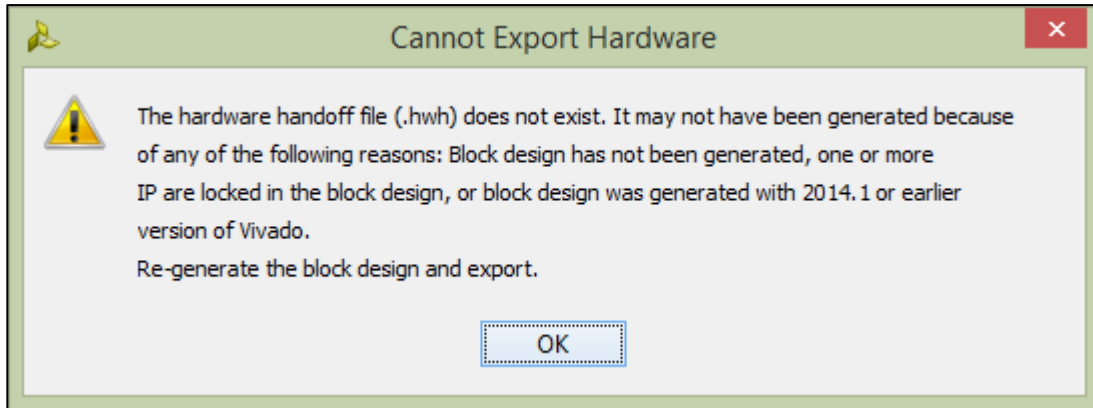


Figure 87. Cannot Export Hardware

At this point, click on Open Block Design from the flow navigator as shown below.

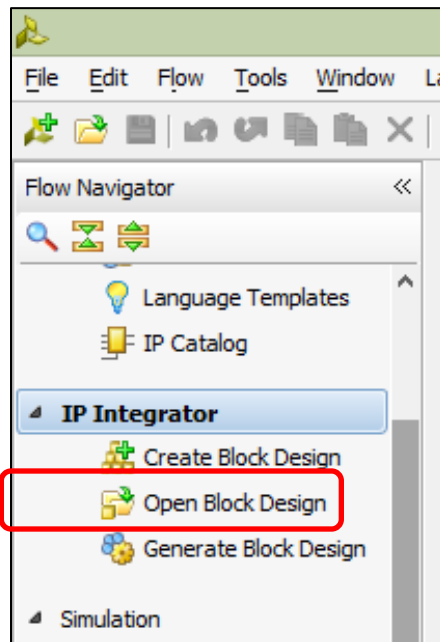


Figure 88. Open Block Design

Click on **Show IP Status**

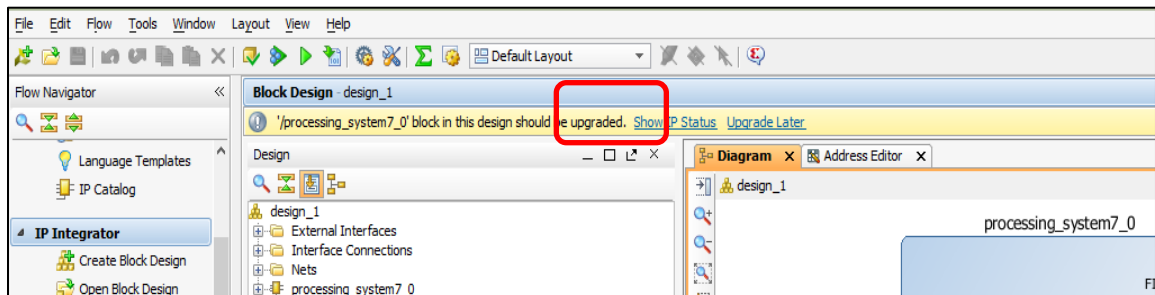


Figure 89. Show IP Status

Click on **Update Selected**

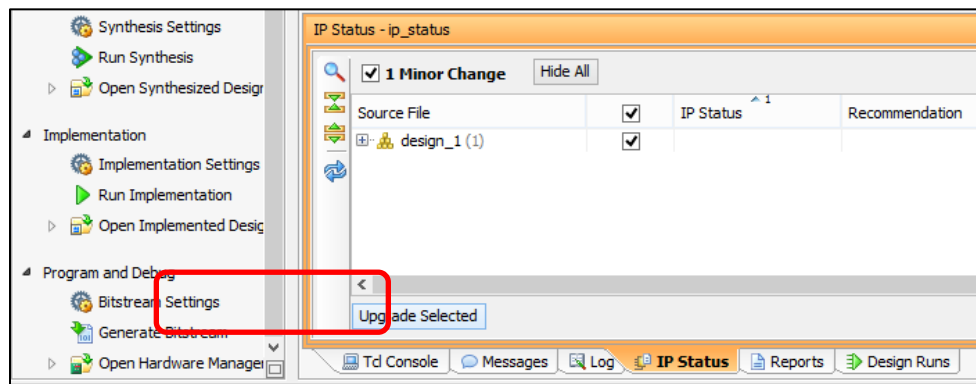


Figure 90. Update Selected

This updates the existing IPs.

47 Diagnostic Engine



Figure 91. Recommendation Engine Block

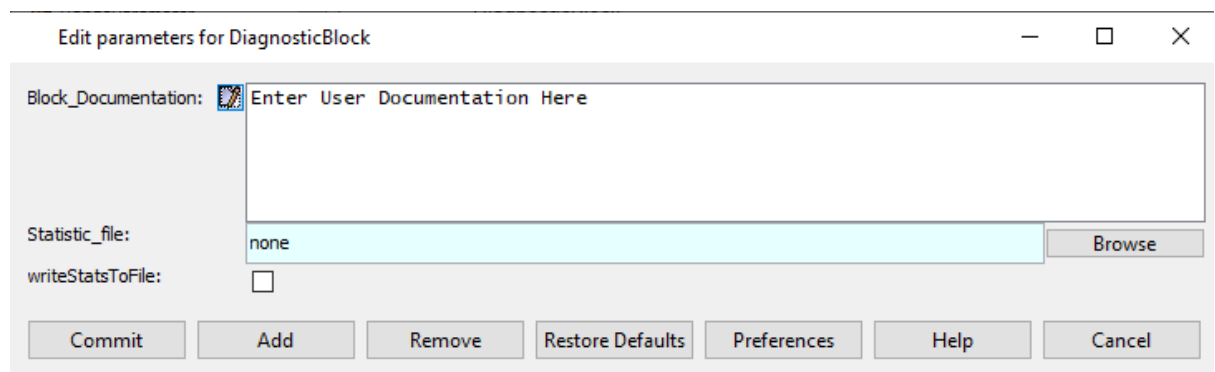
Directory: VisualSim\actor\arch\Diagnostic_Block\

47.1 Features of Diagnostic Block:

1. Statistic Generation for Resource block.
2. Analyzing variables in Script Block.
3. Error detection in Resource block.
4. Listing of Virtual Connections.

47.2 File required for generating Statistics:

1) Input CSV file: .CSV statistic file (below image: Statistic_file parameter) for giving file name.



a) **Mandatory Columns** : Block_Name, Stats_Name, Constraint, Value, Type

b) **Optional Column** : Correlate

Statistic evaluations supported in Diagnostic block.

- a) Latency
- b) Utilization
- c) Buffer_Occupancy
- d) Script Block Variables - Int, Double & Array Data Types
- e) Average, Maximum & Minimum values of all the aforementioned stats

Constraint supported in Diagnostic block-

- a) <
- b) >
- c) >=
- d) <=
- e) =
- f) !=

Columns Description –

Number	Heading	Content
	Column Name	Block_Name
1	Description	The "Block_Name" parameter value of the module which we want to monitor. Every component we use in a demo model will be having a unique name. We need to provide it here.

<p>Example</p>	<div data-bbox="581 260 1471 730"> <p>Edit parameters for Queues</p> <p>Block_Documentation: Enter User Documentation Here</p> <p>Block_Name: "Smart_Resource"</p> <p>Queue_Number_Field: input_Q_Num</p> <p>Priority_Field: Int_Dbl_Expr_Mem_Fld</p> <p>Max_Queue_Length: 30</p> <p>Number_of_Queues: 5</p> <p>Initial_Queue_State: First_Token_Flow_Through</p> <p>Queue_Reject_Mechanis...: Incoming_Token_Rejected</p> <p>Queue_Type: FIFO</p> <p>Commit Add Remove Restore Defaults Preferences Help Cancel</p> </div> <p style="text-align: center;"><u>Resource Blocks</u></p> <div data-bbox="581 802 1471 1390"> <p>Edit parameters for Script</p> <p>Block_Documentation: Enter User Documentation Here</p> <p>Block_Name: "MyMachine"</p> <p>Optional_Parameters: /* First row contains Column Names. */</p> <table border="1"> <thead> <tr> <th>Parameter_Name</th> <th>Parameter_Value</th> </tr> </thead> <tbody> <tr><td>Path</td><td>VS/User_Library</td></tr> <tr><td>Read_File</td><td>none</td></tr> <tr><td>Save_Files</td><td>false</td></tr> <tr><td>Profile_File</td><td>none</td></tr> <tr><td>Listen_to_File</td><td>none</td></tr> <tr><td>Duplicate_Input</td><td>true</td></tr> <tr><td>Profile</td><td>0</td></tr> <tr><td>Maximum_Loops</td><td>1000000</td></tr> <tr><td>Block_Reference</td><td>Block_Name</td></tr> <tr><td>Port_Order_Array</td><td>{"input"}</td></tr> <tr><td>Add_Scheduler_Times_to_DS</td><td>false</td></tr> </tbody> </table> <p>Single_Cycle: <input type="checkbox"/></p> <p>Breakpoint: none</p> <p>Commit Add Remove Restore Defaults Preferences Help Cancel</p> </div> <p style="text-align: center;"><u>Script Blocks</u></p>	Parameter_Name	Parameter_Value	Path	VS/User_Library	Read_File	none	Save_Files	false	Profile_File	none	Listen_to_File	none	Duplicate_Input	true	Profile	0	Maximum_Loops	1000000	Block_Reference	Block_Name	Port_Order_Array	{"input"}	Add_Scheduler_Times_to_DS	false
	Parameter_Name	Parameter_Value																							
Path	VS/User_Library																								
Read_File	none																								
Save_Files	false																								
Profile_File	none																								
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Profile	0																								
Maximum_Loops	1000000																								
Block_Reference	Block_Name																								
Port_Order_Array	{"input"}																								
Add_Scheduler_Times_to_DS	false																								
<p>Column Name</p>	<p style="text-align: center;">Stats_Name</p> <p>Description</p> <p>For standard resource blocks (like Queue block, Server block, System resource block, system resource extend block),</p>																								

2

following list of stats are only supported:

1. Latency
2. Utilization
3. Buffer_Occupancy

For Script blocks, we can use any variable defined within the script under this column

Example

```

file/C:/VisualSim/V... Editor for Expression_List of .model.Script2
File Edit Help
1 idx=0
2 arr1 = {0.0,0.0,0.0,0.0,0.0,0.0}
3 arr2 = {}
4 while (idx<10) {
5     index = irand(0,arr1.length()-1)
6     arr1(index) = rand()
7     arr2.append(cast(1L, irand(0,idx)))
8     idx = idx + 1
9 }
10 LABEL:BEGIN
    
```

Variables - idx, arr1, arr2, index

```

chitect - file/C:/VisualSim/V... Editor for Expression_List of .Script_Test.Script2
File Edit Help
1 prioArr = {}
2 id_arr = {}
3 LABEL:BEGIN
4 id = port_token.id
5 index = id_arr.search(id)
6 prio = port_token.priority
7 if (index < 0) {
8     id_arr.append(id)
9     prioArr.append(prio)
10 }
11 else {
12     prioArr(index) = prio
13 }
    
```

Variables - prioArr, id_arr, id, index, prio

Script Blocks

3	Column Name	Constraint																																																	
	Description	<p>Following types are supported:</p> <ol style="list-style-type: none"> > < >= <= != = 																																																	
	Example	<table border="1"> <thead> <tr> <th>Block_Nar</th> <th>Stats_Nar</th> <th>Constraint</th> <th>Value</th> <th>Type</th> </tr> </thead> <tbody> <tr> <td>Smart_Res</td> <td>Latency</td> <td>></td> <td>3.05</td> <td>Avg</td> </tr> <tr> <td>MyMachin</td> <td>idx</td> <td><</td> <td>1</td> <td>Avg</td> </tr> <tr> <td>MyMachin</td> <td>idx</td> <td>>=</td> <td>0</td> <td>All</td> </tr> <tr> <td>MyMachin</td> <td>idx</td> <td><=</td> <td>0</td> <td>Max</td> </tr> <tr> <td>MyMachin</td> <td>idx</td> <td>!=</td> <td>0</td> <td>Min</td> </tr> <tr> <td>MyMachin</td> <td>arr</td> <td>></td> <td>{ 0=10; default=5 }</td> <td>Avg</td> </tr> <tr> <td>MyMachin</td> <td>arr</td> <td><</td> <td>0</td> <td>All</td> </tr> <tr> <td>MyMachin</td> <td>arr</td> <td>!=</td> <td>0</td> <td>Max</td> </tr> <tr> <td>MyMachin</td> <td>arr</td> <td>></td> <td>0</td> <td>Min</td> </tr> </tbody> </table>	Block_Nar	Stats_Nar	Constraint	Value	Type	Smart_Res	Latency	>	3.05	Avg	MyMachin	idx	<	1	Avg	MyMachin	idx	>=	0	All	MyMachin	idx	<=	0	Max	MyMachin	idx	!=	0	Min	MyMachin	arr	>	{ 0=10; default=5 }	Avg	MyMachin	arr	<	0	All	MyMachin	arr	!=	0	Max	MyMachin	arr	>	0
Block_Nar	Stats_Nar	Constraint	Value	Type																																															
Smart_Res	Latency	>	3.05	Avg																																															
MyMachin	idx	<	1	Avg																																															
MyMachin	idx	>=	0	All																																															
MyMachin	idx	<=	0	Max																																															
MyMachin	idx	!=	0	Min																																															
MyMachin	arr	>	{ 0=10; default=5 }	Avg																																															
MyMachin	arr	<	0	All																																															
MyMachin	arr	!=	0	Max																																															
MyMachin	arr	>	0	Min																																															
4	Column Name	Value																																																	
	Description	<p>Specifies the threshold value to which the comparison is being made by diagnostic block.</p> <p>Supported values:</p> <ol style="list-style-type: none"> Integer 																																																	

	<p>2. Double</p> <p>3. A structure (for array alone)</p> <p>The structure should be of the following format: <code>{id1=value;id2=value;id3.....;default=value}</code> default value must be specified if user is choosing this format. This is because, if an id which is not specified in the value structure comes in, then the default value will be used as the threshold value.</p> <p>id1, id2 etc. used in the above structure can either correspond to an index value in the array (starting from 0 to n-1, where n is the length of the array) or to the corresponding value in the correlated array mentioned in the <i>optional</i> 'Correlate' column for the array.</p>																																																		
<p>Example</p>	<table border="1"> <thead> <tr> <th>Block_Nar</th> <th>Stats_Narr</th> <th>Constraint</th> <th>Value</th> <th>Type</th> </tr> </thead> <tbody> <tr> <td>Smart_Res</td> <td>Latency</td> <td>></td> <td></td> <td>3.05 Avg</td> </tr> <tr> <td>MyMachin</td> <td>idx</td> <td><</td> <td></td> <td>1 Avg</td> </tr> <tr> <td>MyMachin</td> <td>idx</td> <td>>=</td> <td></td> <td>0 All</td> </tr> <tr> <td>MyMachin</td> <td>idx</td> <td><=</td> <td></td> <td>0 Max</td> </tr> <tr> <td>MyMachin</td> <td>idx</td> <td>!=</td> <td></td> <td>0 Min</td> </tr> <tr> <td>MyMachin</td> <td>arr</td> <td>></td> <td>{ 0=10; 2=20; default=5 }</td> <td>Avg</td> </tr> <tr> <td>MyMachin</td> <td>arr</td> <td><</td> <td></td> <td>0 All</td> </tr> <tr> <td>MyMachin</td> <td>arr</td> <td>!=</td> <td></td> <td>0 Max</td> </tr> <tr> <td>MyMachin</td> <td>arr</td> <td>></td> <td></td> <td>0 Min</td> </tr> </tbody> </table> <p>All Stats_Name have 'Value' in Integer/Double except arr (for Avg 'Type')</p> <p>arr has the value in the <i>structured</i> form. Here '0' and '2' signifies the indexes of the array.</p>	Block_Nar	Stats_Narr	Constraint	Value	Type	Smart_Res	Latency	>		3.05 Avg	MyMachin	idx	<		1 Avg	MyMachin	idx	>=		0 All	MyMachin	idx	<=		0 Max	MyMachin	idx	!=		0 Min	MyMachin	arr	>	{ 0=10; 2=20; default=5 }	Avg	MyMachin	arr	<		0 All	MyMachin	arr	!=		0 Max	MyMachin	arr	>		0 Min
Block_Nar	Stats_Narr	Constraint	Value	Type																																															
Smart_Res	Latency	>		3.05 Avg																																															
MyMachin	idx	<		1 Avg																																															
MyMachin	idx	>=		0 All																																															
MyMachin	idx	<=		0 Max																																															
MyMachin	idx	!=		0 Min																																															
MyMachin	arr	>	{ 0=10; 2=20; default=5 }	Avg																																															
MyMachin	arr	<		0 All																																															
MyMachin	arr	!=		0 Max																																															
MyMachin	arr	>		0 Min																																															

While '10' and '20' signifies the threshold values for indexes 0 and 2, and the other indexes have the threshold value as the value mentioned against **default** value.

For **Correlate** structured value :

Block_Nar	Stats_Nar	Constraint	Value	Type	Correlate
Pack_1_la	prioArr	>=	{ 0x13 = 5 ; 0x15 = 6 ; default = 5 }	All	id_arr
Buff_1_ch	idx	>=		0 Min	
Buff_1_ch	idy	>=		0 Avg	

Input File

Model : Pa Input file : Patch-1-3.csv

BLOCK	VARIABLE	VALUE	CORRELATE	TRACKER(<Index/Correlate>_<value>)	TYPE	RESULT
Pack_1_la	prioArr	{ 6.0 }	{ 0x13 }	{ 0x13_6.0 }	All	TRUE
Pack_1_la	prioArr	{ 6.0 1.0 }	{ 0x13 0x10 }	{ 0x13_6.0 }	All	TRUE
Pack_1_la	prioArr	{ 6.0 1.0 8.0 }	{ 0x13 0x10 0x15 }	{ 0x13_6.0 0x20_8.0 }	All	TRUE

Output File

So from the above **Output** file, we can see the value '6.0' correlated to '0x13' present in *id_arr* variable. According to this we create the Structure value in the **Input** file with the threshold values.





	Column Name	Type
5	Description	<p>Specifies the type of calculation we have to do. Supported values:</p> <ol style="list-style-type: none"> 1. Max 2. Min 3. Avg 4. All

"All" simply means that we will be monitoring instantaneous value of a variable or a stat (Latency/Buffer Occupancy/Utilization).

Example

Block_Nar	Stats_Nam	Constraint	Value	Type
Smart_Res	Latency	>	3.05	All
Smart_Res	Latency	>	3.05	Avg
MyMachin	idx	<	1	Avg
MyMachin	idx	>=	0	All
MyMachin	idx	<=	0	Max
MyMachin	idx	!=	0	Min
MyMachin	arr	>	{ 0=10; 2=	Avg
MyMachin	arr	<	0	All
MyMachin	arr	!=	0	Max
MyMachin	arr	>	0	Min

Results generated :

 Diagnostic_Stats_Resource_All_Patch-1-2	7/21/2021 5:41 PM	Microsoft Excel Co...	1 KB
 Diagnostic_Stats_Resource_Type_Patch-1-2	7/21/2021 5:41 PM	Microsoft Excel Co...	1 KB
 Diagnostic_Stats_Script_Array_Patch-1-2	7/21/2021 5:41 PM	Microsoft Excel Co...	1 KB
 Diagnostic_Stats_Script_Non-Array_Patch...	7/21/2021 5:41 PM	Microsoft Excel Co...	1 KB

1. Results -> Resource with Type set to be "All"

Model : Pa Input file : Patch-1-2.csv							
BLOCK	SOURCE	TIME	ID	Buffer_Oc	Buffer_Ca	Utilization	Latency
Smart_Res	Traffic2	9.7	61	{9 0 9 0	{30 30 30	0	3.7
Smart_Res	Traffic2	9.9	66	{10 0 8 0	{30 30 30	0	3.4

2. Results -> Resource with Type set to be "Max", "Min" or "Avg"

Model : Pa Input file : Patch-1-2.csv				
BLOCK	STATS_NAME	VALUE	TYPE	RESULT
Smart_Res	Latency	0.732927	Avg	FALSE

3. Results -> Script variables (no array variable) with Type set to be "Max", "Min", "Avg" or "All"

Model : Pa Input file : Patch-1-2.csv				
BLOCK	VARIABLE	VALUE	TYPE	RESULT
MyMachin idx		0	All	TRUE
MyMachin idx		1	All	TRUE
MyMachin idx		2	All	TRUE
MyMachin idx		3	All	TRUE
MyMachin idx		4	All	TRUE
MyMachin idx		5	All	TRUE
MyMachin idx		5	Max	FALSE
MyMachin idx		2.5	Avg	FALSE
MyMachin idx		0	Min	FALSE

4. Results -> Script variables (including array variables) with Type set to be "Max", "Min", "Avg" or "All"

		<table border="1"> <thead> <tr> <th>BLOCK</th> <th>VARIABLE</th> <th>VALUE</th> <th>TRACKER(<Index/Correlate>_<value>)</th> <th>TYPE</th> <th>RESULT</th> </tr> </thead> <tbody> <tr> <td>MyMachin arr</td> <td></td> <td>{ 0.5 1.6666666666666667 { }</td> <td></td> <td>Avg</td> <td>FALSE</td> </tr> <tr> <td>MyMachin arr</td> <td></td> <td>{ 0.0 0.0 0.0 0.0 0 { }</td> <td></td> <td>Min</td> <td>FALSE</td> </tr> <tr> <td>MyMachin arr</td> <td></td> <td>{ 1.0 4.0 4.0 4.0 0 { 0_1.0 1_4.0 2_4.0 3_4.0 }</td> <td></td> <td>Max</td> <td>TRUE</td> </tr> </tbody> </table>	BLOCK	VARIABLE	VALUE	TRACKER(<Index/Correlate>_<value>)	TYPE	RESULT	MyMachin arr		{ 0.5 1.6666666666666667 { }		Avg	FALSE	MyMachin arr		{ 0.0 0.0 0.0 0.0 0 { }		Min	FALSE	MyMachin arr		{ 1.0 4.0 4.0 4.0 0 { 0_1.0 1_4.0 2_4.0 3_4.0 }		Max	TRUE																											
BLOCK	VARIABLE	VALUE	TRACKER(<Index/Correlate>_<value>)	TYPE	RESULT																																																
MyMachin arr		{ 0.5 1.6666666666666667 { }		Avg	FALSE																																																
MyMachin arr		{ 0.0 0.0 0.0 0.0 0 { }		Min	FALSE																																																
MyMachin arr		{ 1.0 4.0 4.0 4.0 0 { 0_1.0 1_4.0 2_4.0 3_4.0 }		Max	TRUE																																																
6	Column Name	Correlate																																																			
	Description	<p>Used only for an array variable monitoring.</p> <p>Example: Latency array variable only stores the latency value, but to correlate it with id array we need to specify the id array.</p> <p>For an array, if we don't specify the correlate variable, then the array index will be used for correlation.</p>																																																			
	Example	<table border="1"> <thead> <tr> <th>Block_Nar</th> <th>Stats_Nam</th> <th>Constraint</th> <th>Value</th> <th>Type</th> <th>Correlate</th> </tr> </thead> <tbody> <tr> <td>Pack_1_la</td> <td>prioArr</td> <td>>=</td> <td>{ 0x13 = 5 ; 0x15 = 6 ; default = 5 }</td> <td>All</td> <td>id_arr</td> </tr> <tr> <td>Buff_1_ch</td> <td>idx</td> <td>>=</td> <td></td> <td>0 Min</td> <td></td> </tr> <tr> <td>Buff_1_ch</td> <td>idy</td> <td>>=</td> <td></td> <td>0 Avg</td> <td></td> </tr> </tbody> </table> <p style="text-align: center;"><u>Input File</u></p> <table border="1"> <thead> <tr> <th>BLOCK</th> <th>VARIABLE</th> <th>VALUE</th> <th>CORRELATE</th> <th>TRACKER(<Index/Correlate>_<value>)</th> <th>TYPE</th> <th>RESULT</th> </tr> </thead> <tbody> <tr> <td>Pack_1_la</td> <td>prioArr</td> <td>{ 6.0 }</td> <td>{ 0x13 }</td> <td>{ 0x13_6.0 }</td> <td>All</td> <td>TRUE</td> </tr> <tr> <td>Pack_1_la</td> <td>prioArr</td> <td>{ 6.0 1.0 }</td> <td>{ 0x13 0x10 }</td> <td>{ 0x13_6.0 }</td> <td>All</td> <td>TRUE</td> </tr> <tr> <td>Pack_1_la</td> <td>prioArr</td> <td>{ 6.0 1.0 8.0 }</td> <td>{ 0x13 0x10 0x20 }</td> <td>{ 0x13_6.0 0x20_8.0 }</td> <td>All</td> <td>TRUE</td> </tr> </tbody> </table> <p style="text-align: center;"><u>Output File</u></p> <p>TRACKER column will list out the values which pass the threshold condition (<i>only for array</i>).</p> <p>Format:</p>	Block_Nar	Stats_Nam	Constraint	Value	Type	Correlate	Pack_1_la	prioArr	>=	{ 0x13 = 5 ; 0x15 = 6 ; default = 5 }	All	id_arr	Buff_1_ch	idx	>=		0 Min		Buff_1_ch	idy	>=		0 Avg		BLOCK	VARIABLE	VALUE	CORRELATE	TRACKER(<Index/Correlate>_<value>)	TYPE	RESULT	Pack_1_la	prioArr	{ 6.0 }	{ 0x13 }	{ 0x13_6.0 }	All	TRUE	Pack_1_la	prioArr	{ 6.0 1.0 }	{ 0x13 0x10 }	{ 0x13_6.0 }	All	TRUE	Pack_1_la	prioArr	{ 6.0 1.0 8.0 }	{ 0x13 0x10 0x20 }	{ 0x13_6.0 0x20_8.0 }	All
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		{<array index (if correlate column is empty) or correlate array corresponding value>_<variable value which we are monitoring> <>_<> }
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Examples for Resource Block –

Number	Heading	Content																																																							
1	Stats_Name	Latency																																																							
	Type	All																																																							
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Description	Outputs the details of all the data packets which have Latency > 2																																																								
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	Block_Nar	Stats_Nar	Constraint	Value	Type											
	Smart_Res	Latency	>=	3.05	<input type="text"/> Avg Max Min											
Description	Outputs a single value - Avg/Max/Min, for the Latencies of all the data packets and gives a Result - TRUE, if the value satisfies the given constraint ,else FALSE															
Output File	<table border="1"> <thead> <tr> <th>Model : Di</th> <th>Input file : Latency_Type.csv</th> <th></th> <th></th> <th></th> </tr> <tr> <th>BLOCK</th> <th>STATS_NA</th> <th>VALUE</th> <th>TYPE</th> <th>RESULT</th> </tr> </thead> <tbody> <tr> <td>Smart_Res</td> <td>Latency</td> <td>3.035141</td> <td>Avg</td> <td>FALSE</td> </tr> </tbody> </table>	Model : Di	Input file : Latency_Type.csv				BLOCK	STATS_NA	VALUE	TYPE	RESULT	Smart_Res	Latency	3.035141	Avg	FALSE
Model : Di	Input file : Latency_Type.csv															
BLOCK	STATS_NA	VALUE	TYPE	RESULT												
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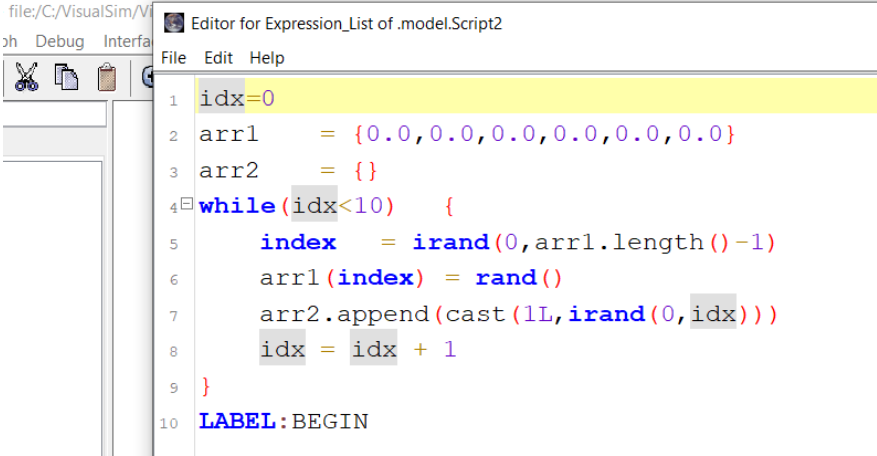
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		Smart_Resource	Buffer_Occup	>=	3.05	All																																																	
	Description	<p>Outputs the details of all the data packets which have Buffer_Occupancy >= 3.05</p> <p>In this case the Buffer_Occupancy is an array. So, we check if any element of the array has a value >= 3.05. If it does, we print the details of that packet.</p>																																																					
Output File	<table border="1"> <thead> <tr> <th>BLOCK</th> <th>SOURCE</th> <th>TIME</th> <th>ID</th> <th>Buffer_Occupancy</th> <th>Buffer_Capacity</th> <th>Utilization</th> <th>Latency</th> </tr> </thead> <tbody> <tr> <td>Smart_Resource</td> <td>Traffic</td> <td>1.3</td> <td>14</td> <td>{0 5 0 0 0}</td> <td>{30 30 30}</td> <td>0</td> <td>0</td> </tr> <tr> <td>Smart_Resource</td> <td>Traffic</td> <td>1.5</td> <td>16</td> <td>{1 5 0 0 0}</td> <td>{30 30 30}</td> <td>0</td> <td>0</td> </tr> <tr> <td>Smart_Resource</td> <td>Traffic</td> <td>1.6</td> <td>17</td> <td>{1 5 0 0 0}</td> <td>{30 30 30}</td> <td>0</td> <td>0</td> </tr> <tr> <td>Smart_Resource</td> <td>Traffic</td> <td>1.6</td> <td>4</td> <td>{1 4 0 0 0}</td> <td>{30 30 30}</td> <td>0</td> <td>1.3</td> </tr> <tr> <td>Smart_Resource</td> <td>Traffic</td> <td>1.8</td> <td>18</td> <td>{2 4 0 0 0}</td> <td>{30 30 30}</td> <td>0</td> <td>0.1</td> </tr> </tbody> </table>							BLOCK	SOURCE	TIME	ID	Buffer_Occupancy	Buffer_Capacity	Utilization	Latency	Smart_Resource	Traffic	1.3	14	{0 5 0 0 0}	{30 30 30}	0	0	Smart_Resource	Traffic	1.5	16	{1 5 0 0 0}	{30 30 30}	0	0	Smart_Resource	Traffic	1.6	17	{1 5 0 0 0}	{30 30 30}	0	0	Smart_Resource	Traffic	1.6	4	{1 4 0 0 0}	{30 30 30}	0	1.3	Smart_Resource	Traffic	1.8	18	{2 4 0 0 0}	{30 30 30}	0	0.1
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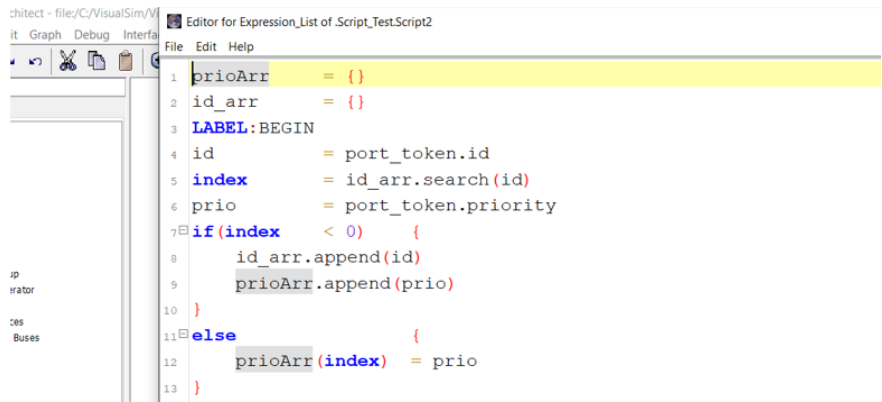
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8	Stats_Name	<p align="center"><i>Combined</i> (Latency, Buffer_Occupancy, Utilization)</p>																																																																
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	Input File	<table border="1"> <tr> <td>Block_Name</td> <td>Stats_Name</td> <td>Constraint</td> <td>Value</td> <td>Type</td> </tr> <tr> <td>Smart_Resource</td> <td>Latency</td> <td>>=</td> <td>3.05</td> <td>Max</td> </tr> <tr> <td>Smart_Resource</td> <td>Buffer_Occupancy</td> <td>>=</td> <td>3.05</td> <td>Min</td> </tr> <tr> <td>Smart_Resource</td> <td>Utilization</td> <td>>=</td> <td>3.05</td> <td>Avg</td> </tr> </table>	Block_Name	Stats_Name	Constraint	Value	Type	Smart_Resource	Latency	>=	3.05	Max	Smart_Resource	Buffer_Occupancy	>=	3.05	Min	Smart_Resource	Utilization	>=	3.05	Avg																																												
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Description	<p>Outputs a single value for each Stats_Name, for all the data packets and gives Result - TRUE, if the value satisfies the given constraint else, FALSE</p>																																																																	
Output File	<table border="1"> <tr> <td colspan="2">Model : Di</td> <td colspan="2">Input file : Combined_Type.csv</td> <td></td> </tr> <tr> <td>BLOCK</td> <td>STATS_NA</td> <td>VALUE</td> <td>TYPE</td> <td>RESULT</td> </tr> <tr> <td>Smart_Res</td> <td>Latency</td> <td>9.2</td> <td>Max</td> <td>TRUE</td> </tr> <tr> <td>Smart_Res</td> <td>Buffer_Oc</td> <td>0</td> <td>Min</td> <td>FALSE</td> </tr> <tr> <td>Smart_Res</td> <td>Utilization</td> <td>0</td> <td>Avg</td> <td>FALSE</td> </tr> </table>	Model : Di		Input file : Combined_Type.csv			BLOCK	STATS_NA	VALUE	TYPE	RESULT	Smart_Res	Latency	9.2	Max	TRUE	Smart_Res	Buffer_Oc	0	Min	FALSE	Smart_Res	Utilization	0	Avg	FALSE																																								
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Examples for Script Block –

Number	Heading	Content															
1	Stats_Name (Data Type)	Int / Double															
	Type	All															
	Correlate (Optional Column)	Absent															
	Input File	<table border="1" data-bbox="592 961 1453 1113"> <thead> <tr> <th>Block_Name</th> <th>Stats_Nam</th> <th>Constraint</th> <th>Value</th> <th>Type</th> </tr> </thead> <tbody> <tr> <td>S2_Test_Case</td> <td>idx</td> <td>>=</td> <td>0</td> <td>All</td> </tr> <tr> <td>S2_Test_Case</td> <td>index</td> <td>>=</td> <td>0</td> <td>All</td> </tr> </tbody> </table>	Block_Name	Stats_Nam	Constraint	Value	Type	S2_Test_Case	idx	>=	0	All	S2_Test_Case	index	>=	0	All
	Block_Name	Stats_Nam	Constraint	Value	Type												
S2_Test_Case	idx	>=	0	All													
S2_Test_Case	index	>=	0	All													
Description	<p>Outputs all the values stored by each Stats_Name (idx and index, in this case) that passes the given constraint, for the entire simulation.</p> <p>So here we get all the values of idx which are ≥ 0 and all the values of index which are ≥ 0</p>																

Output File	<table border="1"> <tr><td>10</td><td>S2_Test_C index</td><td>4</td><td>All</td><td>TRUE</td></tr> <tr><td>11</td><td>S2_Test_C index</td><td>0</td><td>All</td><td>TRUE</td></tr> <tr><td>12</td><td>S2_Test_C index</td><td>1</td><td>All</td><td>TRUE</td></tr> <tr><td>13</td><td>S2_Test_C index</td><td>3</td><td>All</td><td>TRUE</td></tr> <tr><td>14</td><td>S2_Test_C idx</td><td>0</td><td>All</td><td>TRUE</td></tr> <tr><td>15</td><td>S2_Test_C idx</td><td>1</td><td>All</td><td>TRUE</td></tr> <tr><td>16</td><td>S2_Test_C idx</td><td>2</td><td>All</td><td>TRUE</td></tr> <tr><td>17</td><td>S2_Test_C idx</td><td>3</td><td>All</td><td>TRUE</td></tr> </table>	10	S2_Test_C index	4	All	TRUE	11	S2_Test_C index	0	All	TRUE	12	S2_Test_C index	1	All	TRUE	13	S2_Test_C index	3	All	TRUE	14	S2_Test_C idx	0	All	TRUE	15	S2_Test_C idx	1	All	TRUE	16	S2_Test_C idx	2	All	TRUE	17	S2_Test_C idx	3	All	TRUE
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Stats_Name (Data Type)	Array																																								
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2	Input File	<table border="1"> <thead> <tr> <th>Block_Name</th> <th>Stats_Name</th> <th>Constraint</th> <th>Value</th> <th>Type</th> </tr> </thead> <tbody> <tr> <td>Pack_1_lat</td> <td>prioArr</td> <td>>=</td> <td>5</td> <td>All</td> </tr> </tbody> </table>	Block_Name	Stats_Name	Constraint	Value	Type	Pack_1_lat	prioArr	>=	5	All																				
Block_Name	Stats_Name	Constraint	Value	Type																												
Pack_1_lat	prioArr	>=	5	All																												
	Description	<p>Outputs all the values stored by each Stats_Name (prioArr, in this case) if any one of the values present in the array passes the given constraint, for the entire simulation.</p> <p>So here we get all the values of prioArr in which any one element of the array is ≥ 5.</p> <p>We get all the values(of the array) which passes the constraint in the TRACKER column with its <i>index</i> or <i>correlated</i> value as explained in the Columns Description Table above.</p>																														
	Output File	<table border="1"> <thead> <tr> <th>BLOCK</th> <th>VARIABLE</th> <th>VALUE</th> <th>TRACKER(<Index/Correlate>_<value>)</th> <th>TYPE</th> <th>RESULT</th> </tr> </thead> <tbody> <tr> <td>Pack_1_lat_09</td> <td>prioArr</td> <td>{ 6.0 }</td> <td>{ 0_6.0 }</td> <td>All</td> <td>TRUE</td> </tr> <tr> <td>Pack_1_lat_09</td> <td>prioArr</td> <td>{ 6.0 }</td> <td>{ 0_6.0 }</td> <td>All</td> <td>TRUE</td> </tr> <tr> <td>Pack_1_lat_09</td> <td>prioArr</td> <td>{ 6.0 }</td> <td>{ 0_6.0 2_8.0 }</td> <td>All</td> <td>TRUE</td> </tr> <tr> <td>Pack_1_lat_09</td> <td>prioArr</td> <td>{ 6.0 }</td> <td>{ 0_6.0 2_8.0 }</td> <td>All</td> <td>TRUE</td> </tr> </tbody> </table>	BLOCK	VARIABLE	VALUE	TRACKER(<Index/Correlate>_<value>)	TYPE	RESULT	Pack_1_lat_09	prioArr	{ 6.0 }	{ 0_6.0 }	All	TRUE	Pack_1_lat_09	prioArr	{ 6.0 }	{ 0_6.0 }	All	TRUE	Pack_1_lat_09	prioArr	{ 6.0 }	{ 0_6.0 2_8.0 }	All	TRUE	Pack_1_lat_09	prioArr	{ 6.0 }	{ 0_6.0 2_8.0 }	All	TRUE
BLOCK	VARIABLE	VALUE	TRACKER(<Index/Correlate>_<value>)	TYPE	RESULT																											
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	Script Block	 <pre> 1 prioArr = {} 2 id_arr = {} 3 LABEL:BEGIN 4 id = port_token.id 5 index = id_arr.search(id) 6 prio = port_token.priority 7 if(index < 0) { 8 id_arr.append(id) 9 prioArr.append(prio) 10 } 11 else { 12 prioArr(index) = prio 13 } </pre> <p style="text-align: center;">Pack_1_lat_09</p>																														

3	Stats_Name (Data Type)	Combined (<i>Int, Double & Array</i>)																																																				
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Model : m Input file : Combined_Type.csv				
BLOCK	VARIABLE	VALUE	TYPE	RESULT
S1_Test_C	idx	10	Max	TRUE
S2_Test_C	index	0	Min	TRUE
S2_Test_C	idx	10	Max	TRUE

Non-Array File

Script Block

```

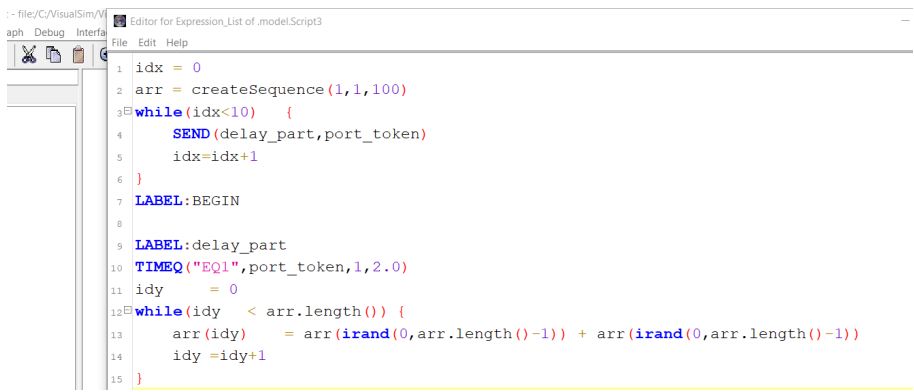
1 idx=0
2 arr = {}
3 while(idx<10) {
4     arr.append(idx)
5     SEND(delay_part,port_token)
6     idx=idx+1
7 }
8 LABEL:BEGIN
9
10 LABEL:delay_part
11 TIMEQ("EQ1",port_token,1,2.0)
12 SEND(output,port_token)
    
```

S1_Test_Case

```

1 idx=0
2 arr1 = {0.0,0.0,0.0,0.0,0.0,0.0}
3 arr2 = {}
4 while(idx<10) {
5     index = irand(0,arr1.length()-1)
6     arr1(index) = rand()
7     arr2.append(cast(1L,irand(0,idx)))
8     idx = idx + 1
9 }
10 LABEL:BEGIN
    
```

S2_Test_Case

		 <p style="text-align: center;">S1_Test_Case_3</p>																							
4	Stats_Name (Data Type)	Combined (<i>Int, Double & Array</i>)																							
	Type	All																							
	Correlate (Optional Column)	Present																							
	Input File	<table border="1" data-bbox="609 1260 1437 1428"> <thead> <tr> <th>Block_Nar</th> <th>Stats_Nam</th> <th>Constraint</th> <th>Value</th> <th>Type</th> <th>Correlate</th> </tr> </thead> <tbody> <tr> <td>Pack_1_la</td> <td>prioArr</td> <td>>=</td> <td>0</td> <td>All</td> <td>id_arr</td> </tr> <tr> <td>Buff_1_ch</td> <td>arr</td> <td>>=</td> <td>0</td> <td>All</td> <td></td> </tr> <tr> <td>Buff_1_ch</td> <td>idx</td> <td>>=</td> <td>0</td> <td>All</td> <td></td> </tr> </tbody> </table>	Block_Nar	Stats_Nam	Constraint	Value	Type	Correlate	Pack_1_la	prioArr	>=	0	All	id_arr	Buff_1_ch	arr	>=	0	All		Buff_1_ch	idx	>=	0	All
Block_Nar	Stats_Nam	Constraint	Value	Type	Correlate																				
Pack_1_la	prioArr	>=	0	All	id_arr																				
Buff_1_ch	arr	>=	0	All																					
Buff_1_ch	idx	>=	0	All																					
	Description	<p>Outputs all the values stored by each Stats_Name for the entire simulation based on the respective method for Int/Double/Array data types, as explained above.</p>																							

Here we have an additional **CORRELATE** column for **Arrays**. It gives the value stored by the corresponding **Correlate** array at the same time.

So, when **prioArr** stored {6.0}, **id_arr** stored {0x13} etc.

Output File

Model : Script Input file : Combined.csv

BLOCK	VARIABLE	VALUE	CORRELATE	TRACKER	TYPE	RESULT
Pack_1_lat	prioArr	{ 6.0 }	{ 0x13 }	{ 0x13_6.0	All	TRUE
Pack_1_lat	prioArr	{ 6.0	{ 0x13	{ 0x13_6.0	All	TRUE
Pack_1_lat	prioArr	{ 6.0	{ 0x13	{ 0x13_6.0	All	TRUE
Pack_1_lat	prioArr	{ 6.0	{ 0x13	{ 0x13_6.0	All	TRUE


Array File

Model : Script Input file : Combined_All_Correlate.csv

BLOCK	VARIABLE	VALUE	TYPE	RESULT
Buff_1_ch	idx	0	All	TRUE
Buff_1_ch	idx	1	All	TRUE
Buff_1_ch	idx	2	All	TRUE
Buff_1_ch	idx	3	All	TRUE
Buff_1_ch	idx	4	All	TRUE
Buff_1_ch	idx	5	All	TRUE

Non - Array File

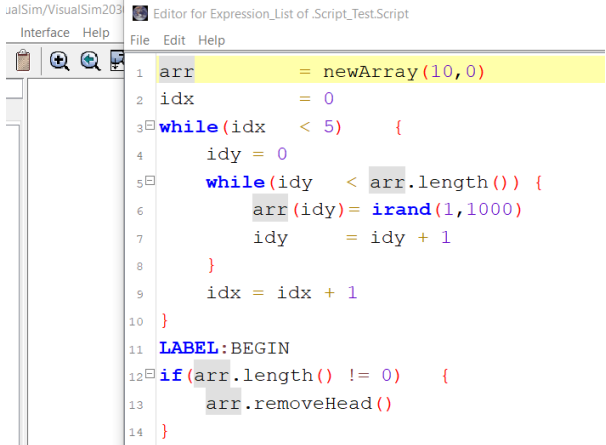
Script Block




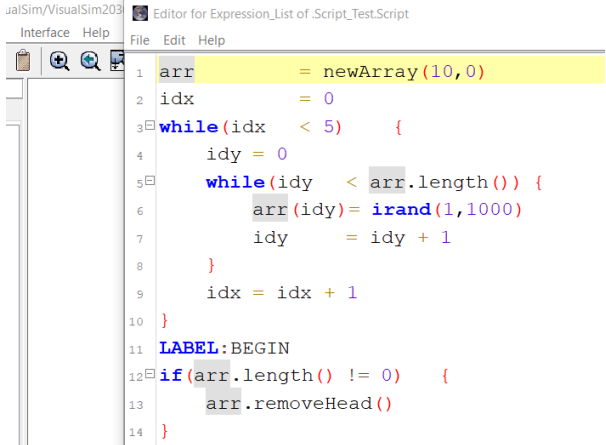
```

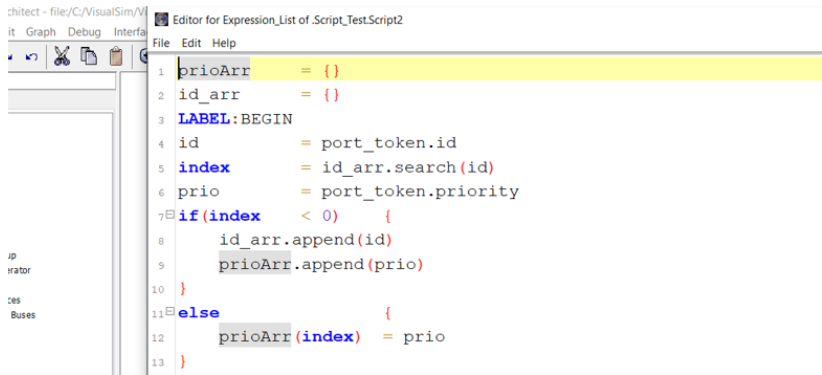
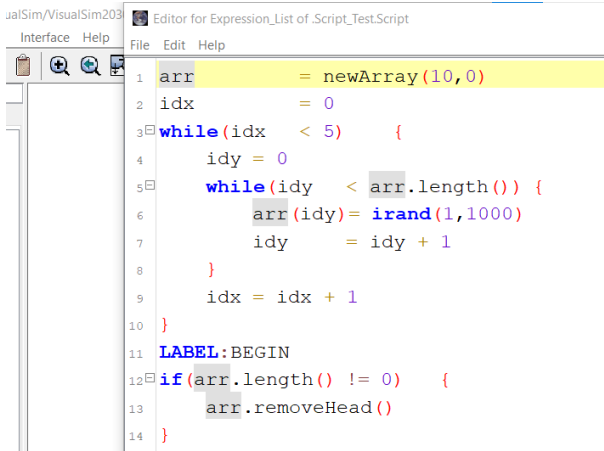
1 prioArr = {}
2 id_arr = {}
3 LABEL: BEGIN
4 id = port_token.id
5 index = id_arr.search(id)
6 prio = port_token.priority
7 if(index < 0) {
8     id_arr.append(id)
9     prioArr.append(prio)
10 }
11 else {
12     prioArr(index) = prio
13 }
    
```

Pack_1_lat_09

		 <p style="text-align: center;">Buff_1_ch_2</p>																								
5	Stats_Name (Data Type)	Combined (Int, Double & Array)																								
	Type	Max / Min / Avg																								
	Correlate (Optional Column)	Present																								
	Input File	<table border="1" data-bbox="625 1333 1421 1501"> <thead> <tr> <th>Block_Nar</th> <th>Stats_Nar</th> <th>Constraint</th> <th>Value</th> <th>Type</th> <th>Correlate</th> </tr> </thead> <tbody> <tr> <td>Pack_1_la</td> <td>prioArr</td> <td>>=</td> <td>0</td> <td>Avg</td> <td>id_arr</td> </tr> <tr> <td>Buff_1_ch</td> <td>arr</td> <td>>=</td> <td>0</td> <td>Avg</td> <td></td> </tr> <tr> <td>Buff_1_ch</td> <td>idx</td> <td>>=</td> <td>0</td> <td>Avg</td> <td></td> </tr> </tbody> </table>	Block_Nar	Stats_Nar	Constraint	Value	Type	Correlate	Pack_1_la	prioArr	>=	0	Avg	id_arr	Buff_1_ch	arr	>=	0	Avg		Buff_1_ch	idx	>=	0	Avg	
	Block_Nar	Stats_Nar	Constraint	Value	Type	Correlate																				
Pack_1_la	prioArr	>=	0	Avg	id_arr																					
Buff_1_ch	arr	>=	0	Avg																						
Buff_1_ch	idx	>=	0	Avg																						
Description	<p>Outputs a single value - Avg/Max/Min, for each Stats_Name for the entire simulation, along with the CORRELATE column and gives, Result - TRUE if the value satisfies the given constraint,</p>																									

	else FALSE																																													
Output File	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="6">Model : Sc Input file : Combined_Type_Correlate.csv</th> </tr> <tr> <th>BLOCK</th> <th>VARIABLE</th> <th>VALUE</th> <th>CORRELATE</th> <th>TRACKER(<Index/C</th> <th>TYPE</th> <th>RESULT</th> </tr> </thead> <tbody> <tr> <td>Buff_1_ch</td> <td>arr</td> <td>{ 441.4 465</td> <td></td> <td>{ 0_441.4 1_4</td> <td>Avg</td> <td>TRUE</td> </tr> <tr> <td>Pack_1_la</td> <td>prioArr</td> <td>{ 4.5714285714;</td> <td>{ 0x13 0x1</td> <td>{ 0x13_4.5714285</td> <td>Avg</td> <td>TRUE</td> </tr> </tbody> </table> <p style="text-align: center;"><u>Array File</u></p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 20px;"> <thead> <tr> <th colspan="6">Model : Sc Input file : Combined_Type_Correlate.csv</th> </tr> <tr> <th>BLOCK</th> <th>VARIABLE</th> <th>VALUE</th> <th>TYPE</th> <th>RESULT</th> <th></th> </tr> </thead> <tbody> <tr> <td>Buff_1_ch</td> <td>idx</td> <td></td> <td>2.5 Avg</td> <td>TRUE</td> <td></td> </tr> </tbody> </table> <p style="text-align: center;"><u>Non-Array File</u></p>	Model : Sc Input file : Combined_Type_Correlate.csv						BLOCK	VARIABLE	VALUE	CORRELATE	TRACKER(<Index/C	TYPE	RESULT	Buff_1_ch	arr	{ 441.4 465		{ 0_441.4 1_4	Avg	TRUE	Pack_1_la	prioArr	{ 4.5714285714;	{ 0x13 0x1	{ 0x13_4.5714285	Avg	TRUE	Model : Sc Input file : Combined_Type_Correlate.csv						BLOCK	VARIABLE	VALUE	TYPE	RESULT		Buff_1_ch	idx		2.5 Avg	TRUE	
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BLOCK	VARIABLE	VALUE	TYPE	RESULT																																										
Buff_1_ch	idx		2.5 Avg	TRUE																																										
Script Block	 <pre> 1 prioArr = {} 2 id_arr = {} 3 LABEL:BEGIN 4 id = port_token.id 5 index = id_arr.search(id) 6 prio = port_token.priority 7 if(index < 0) { 8 id_arr.append(id) 9 prioArr.append(prio) 10 } 11 else { 12 prioArr(index) = prio 13 } </pre> <p style="text-align: center;">Pack_1_lat_09</p>																																													

	 <p style="text-align: center;">Buff_1_ch_2</p>																		
<p>Stats_Name (Data Type)</p>	<p>Array</p>																		
<p>Type</p>	<p>Max / Min / Avg</p>																		
<p>Correlate (Optional Column)</p>	<p>Present</p>																		
<p>6 Input File</p>	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Block_Name</th> <th>Stats_Narr</th> <th>Constraint</th> <th>Value</th> <th>Type</th> <th>Correlate</th> </tr> </thead> <tbody> <tr> <td>Pack_1_lat_09</td> <td>prioArr</td> <td>>=</td> <td>{ 0x13=2 ; 0x10 = 1 ; 0x20=2 ; 0x14=1 ; default=10 }</td> <td>Avg</td> <td>id_arr</td> </tr> <tr> <td>Buff_1_ch_2</td> <td>arr</td> <td><</td> <td>{ 0=500 ; 1=450; 2=500; 3=400; default=600 }</td> <td>Avg</td> <td></td> </tr> </tbody> </table>	Block_Name	Stats_Narr	Constraint	Value	Type	Correlate	Pack_1_lat_09	prioArr	>=	{ 0x13=2 ; 0x10 = 1 ; 0x20=2 ; 0x14=1 ; default=10 }	Avg	id_arr	Buff_1_ch_2	arr	<	{ 0=500 ; 1=450; 2=500; 3=400; default=600 }	Avg	
Block_Name	Stats_Narr	Constraint	Value	Type	Correlate														
Pack_1_lat_09	prioArr	>=	{ 0x13=2 ; 0x10 = 1 ; 0x20=2 ; 0x14=1 ; default=10 }	Avg	id_arr														
Buff_1_ch_2	arr	<	{ 0=500 ; 1=450; 2=500; 3=400; default=600 }	Avg															
<p>Description</p>	<p>Outputs a single value - Avg/Max/Min, for each Stats_Name for the entire simulation, along with the CORRELATE column and gives, Result - TRUE if the value satisfies the given constraint else FALSE</p>																		

	<p>For the Arrays, you can enter the value in the structured form as explained in the Column Description Table.</p>																					
<p>Output File</p>	<table border="1"> <thead> <tr> <th>Block Name</th> <th>Variable</th> <th>Value</th> <th>Correlate</th> <th>Tracker</th> <th>Type</th> <th>Result</th> </tr> </thead> <tbody> <tr> <td>Pack_1_lat</td> <td>prioArr</td> <td>{ 4.571428571428571 4.6</td> <td>{ 0x13 0x10 0x20</td> <td>{ 0x13_4.571428571428571</td> <td>Avg</td> <td>TRUE</td> </tr> <tr> <td>Buff_1_ch</td> <td>arr</td> <td>{ 441.4 465.0 415.84€</td> <td></td> <td>{ 0_441.4 2_415.84615384</td> <td>Avg</td> <td>TRUE</td> </tr> </tbody> </table>	Block Name	Variable	Value	Correlate	Tracker	Type	Result	Pack_1_lat	prioArr	{ 4.571428571428571 4.6	{ 0x13 0x10 0x20	{ 0x13_4.571428571428571	Avg	TRUE	Buff_1_ch	arr	{ 441.4 465.0 415.84€		{ 0_441.4 2_415.84615384	Avg	TRUE
Block Name	Variable	Value	Correlate	Tracker	Type	Result																
Pack_1_lat	prioArr	{ 4.571428571428571 4.6	{ 0x13 0x10 0x20	{ 0x13_4.571428571428571	Avg	TRUE																
Buff_1_ch	arr	{ 441.4 465.0 415.84€		{ 0_441.4 2_415.84615384	Avg	TRUE																
<p>Script Block</p>	 <pre> 1 prioArr = {} 2 id_arr = {} 3 LABEL:BEGIN 4 id = port_token.id 5 index = id_arr.search(id) 6 prio = port_token.priority 7 if(index < 0) { 8 id_arr.append(id) 9 prioArr.append(prio) 10 } 11 else { 12 prioArr(index) = prio 13 } </pre> <p style="text-align: center;">Pack_1_lat_09</p>  <pre> 1 arr = newArray(10,0) 2 idx = 0 3 while(idx < 5) { 4 idy = 0 5 while(idy < arr.length()) { 6 arr(idy) = irand(1,1000) 7 idy = idy + 1 8 } 9 idx = idx + 1 10 } 11 LABEL:BEGIN 12 if(arr.length() != 0) { 13 arr.removeHead() 14 } </pre> <p style="text-align: center;">Buff_1_ch_2</p>																					

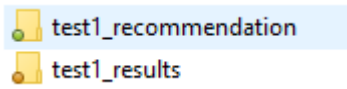
NOTE:

- a) The contents of the CSV file specified are *CASE SENSITIVE* except the **Type** column.
- b) The columns should be entered in the same order as shown above, in the Input.csv file.
- c) The **"Type"** should be the 5th column in the input file with any one of the following values :
 - i) **All** - Outputs all the values for the *Stats_name* which pass the given constraint.
 - ii) **Avg** - Outputs a single *Average* value for all the values stored in *Stats_name*.
 - iii) **Min** - Outputs a single *Minimum* value for all the values stored in *Stats_name*.
 - iv) **Max** - Outputs a single *Maximum* value for all the values stored in *Stats_name*.
- d) **"Correlate"** is an **optional** column, should be added after the **"Type"** column.
- e) The format shown in the last example for *Script Block* for comparing **array** values for the index/correlated value comparison needs to be followed strictly. Any deviation from the given format will lead to errors.

47.3 Output File

Two output files are generated by this block-

- 1) Recommendation file –
- 2) Result file -







Recommendation file will contain the warning conditions like –

- a) if the packet doesn't enter in the Queue block or if the packet doesn't exit from the block. It captures any anomaly if present, inside the block.
- b) if any of the block name specified in the CSV file doesn't match the Block_Name parameter of particular resource block then no constraint evaluation will be performed for that block.

Block_Recommendation 0.0 ps

Queue Number 1, 2, 4, 5 of Smart_Resource is not being used at 0.0 ps
 Queue Number 1, 2, 4, 5 of Smart_Resource is not sending out any transaction. Check the pop or the priority of the queue to make sure the logic is correct at 0.0 ps
 Queue Number 1, 2, 5 of Smart_Resource is not being used at 100.0000000000 ms
 Queue Number 1, 2, 5 of Smart_Resource is not sending out any transaction. Check the pop or the priority of the queue to make sure the logic is correct at 100.0000000000 ms
 Queue Number 2, 5 of Smart_Resource is not being used at 200.0000000000 ms
 Queue Number 2, 5 of Smart_Resource is not sending out any transaction. Check the pop or the priority of the queue to make sure the logic is correct at 200.0000000000 ms
 Queue Number 5 of Smart_Resource is not being used at 400.0000000000 ms
 Queue Number 5 of Smart_Resource is not sending out any transaction. Check the pop or the priority of the queue to make sure the logic is correct at 400.0000000000 ms
 The data from Queue Number 1 is going out slower than it is entering in Smart_Resource at 15.000000000000000 sec
 The data from Queue Number 1 is going out slower than it is entering in Smart_Resource at 18.000000000000000 sec
 The data from Queue Number 1, 2, 3, 4 is going out slower than it is entering in Smart_Resource at 21.000000000000000 sec
 The data from Queue Number 1, 2, 3, 4, 5 is going out slower than it is entering in Smart_Resource at 24.000000000000000 sec

Result file will contain the statistics from the resource block & script blocks (according to the given constraints in the Input file) :

	Diagnostic_Stats_Resource_All_Patch-1-2	7/21/2021 5:41 PM	Microsoft Excel Co...	1 KB
	Diagnostic_Stats_Resource_Type_Patch-1-2	7/21/2021 5:41 PM	Microsoft Excel Co...	1 KB
	Diagnostic_Stats_Script_Array_Patch-1-2	7/21/2021 5:41 PM	Microsoft Excel Co...	1 KB
	Diagnostic_Stats_Script_Non-Array_Patch...	7/21/2021 5:41 PM	Microsoft Excel Co...	1 KB

- i) **Diagnostic_Stats_Resource_All_<Model Name>** - Contains statistics for the Resource Blocks with 'All' in the "Type" column.
- ii) **Diagnostic_Stats_Resource_Type_<Model Name>** - Contains statistics for the Resource Blocks with 'Max / Min / Avg' in the "Type" column.
- iii) **Diagnostic_Stats_Script_Array_<Model Name>** - Contains statistics for the Script Block's variables of 'Array' data type.
- iv) **Diagnostic_Stats_Script_Non_Array_<Model Name>** - Contains statistics for the Script Block's of 'Int / Double' data type.

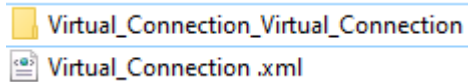
47.4 VisualSim Blocks Supported

- a) Queue
- b) Server
- c) SystemResource
- d) SystemResource_Extend

47.5 Virtual Connection in Diagnostic Block

- *How to use?*

- Drag and Drop Diagnostic block from Library.
- Run the model.
- Save the model to generate Output file.



- Output file demo:

- The .txt file will contain the list of block sending data from *Source* to *Destination*

```
Packet sent from Source .Virtual_Connection_.Script to Destination .Virtual_Connection_.Script2 ( Value : Processor_Script )
Packet sent from Source .Virtual_Connection_.ExpressionList to Destination .Virtual_Connection_.Script ( Value : MyMachine )
Packet sent from Source .Virtual_Connection_.ExpressionList3 to Destination .Virtual_Connection_.Script2 ( Value : Processor_Script )
Packet sent from Source .Virtual_Connection_.ExpressionList3 to Destination .Virtual_Connection_.Script ( Value : MyMachine )
```

- *Supported block*

- IN
- OUT
- MUX
- DEMUX
- Script
- Expression List

48 Qemu Guide

For Ubuntu 18.04

48.1 Steps to install qemu on Ubuntu

- 1) Download and install QEMU from source code.
- 2) Site referred - [https://wiki.qemu.org/Hosts/Linux#Getting the source code](https://wiki.qemu.org/Hosts/Linux#Getting_the_source_code).

```
sudo apt-get install git libglib2.0-dev libfdt-dev libpixman-1-dev zlib1g-dev
sudo apt-get install git-email
sudo apt-get install libaio-dev libbluetooth-dev libbrlapi-dev libbz2-dev
sudo apt-get install libcap-dev libcap-ng-dev libcurl4-gnutls-dev libgtk-3-dev
sudo apt-get install libibverbs-dev libjpeg8-dev libncurses5-dev libnuma-dev
sudo apt-get install librbd-dev librdmacm-dev
sudo apt-get install libsasl2-dev libssl1.2-dev libseccomp-dev libsnappy-dev libssh2-1-dev
sudo apt-get install libvde-dev libvdeplug-dev libvte-2.91-dev libxen-dev libzoo2-dev
sudo apt-get install valgrind xfslibs-dev
sudo apt-get install libnfs-dev libiscsi-dev
```

- 3) git clone [git://git.qemu-project.org/qemu.git](https://git.qemu-project.org/qemu.git)
- 4) # Switch to the QEMU root directory.
- 5) cd qemu
- 6) # Prepare a native debug build.
- 7) mkdir -p bin/debug/native
- 8) cd bin/debug/native
- 9) # Configure QEMU and start the build. This will build for all the target list – ARM, x86-64, RISC-V, PowerPC , SPARC etc.
- 10) ../.././configure --enable-debug
- 11) make
- 12) # Return to the QEMU root directory.
- 13) cd ../../..

-----*****-----

48.2 Download benchmark to run the program

- 1) Download the STREAM benchmarking suite:
 - a. Download stream.c from here: <https://www.cs.virginia.edu/stream/FTP/Code/stream.c>
 - b. Download mysecond.c from here (not required, but just to be safe): <https://www.cs.virginia.edu/stream/FTP/Code/mysecond.c>
- 2) Or create your own C program and run against the different architectures in the next steps.

-----*****-----

48.3 Steps to compile and Run C program for x86 and ARM

- *Test Code used – **stream.c** -download from the above or create your own test code*
- *Connect to the test code directory*
- *Create log-file for either of the architectures –x86 or ARM*

1) x86

a) Compile the program

```
elc1@ubuntu:~/QEMU/tests$ gcc stream.c -o stream-x86
```

user defined test code: gcc filename.c -o filename

b) Run the program

```
elc1@ubuntu:~/QEMU/tests$ ./ stream -x86
```

```
-----
STREAM version $Revision: 5.10 $
-----
```

```
This system uses 8 bytes per array element.
-----
```

```
Array size = 10000000 (elements), Offset = 0 (elements)
```

```
Memory per array = 76.3 MiB (= 0.1 GiB).
```

```
Total memory required = 228.9 MiB (= 0.2 GiB).
```

```
Each kernel will be executed 10 times.
```

```
The *best* time for each kernel (excluding the first iteration)
will be used to compute the reported bandwidth.
```

Your clock granularity/precision appears to be 1 microseconds.
Each test below will take on the order of 197978 microseconds.
(= 197978 clock ticks)

Increase the size of the arrays if this shows that
you are not getting at least 20 clock ticks per test.

WARNING -- The above is only a rough guideline.
For best results, please be sure you know the
precision of your system timer.

Function Best Rate MB/s Avg time Min time Max time
Copy: 5549.6 0.029829 0.028831 0.032965
Scale: 5217.2 0.031839 0.030668 0.033178
Add: 7839.0 0.032011 0.030616 0.034741
Triad: 7401.3 0.033327 0.032427 0.033997

Solution Validates: avg error less than 1.000000e-13 on all three arrays

c) Check the type of the binary thus generated (output is shown below)

```
elc1@ubuntu:~/QEMU/tests$ file stream-x86
```

```
stream-x86: ELF 64-bit LSB shared object, x86-64, version 1 (SYSV), dynamically  
linked, interpreter /lib64/ld-linux-x86-64.so.2, for GNU/Linux 3.2.0,  
BuildID[sha1]=7ff9b39569aef2b4fea79b0913eb1674335d11f3, not stripped
```

d) Generate the instruction trace along with running the executable on emulated x86 architecture.

-d flag specifies the type of logs required (it will help to generate the log). The entire list can be obtained by specifying -d help. We will use -d strace.

For assembly code – in_asm

-D flag specifies the location where the logs should be written.

Use the following command (It will generate the logfile-x86-64)

The entire list can be obtained by specifying -d help


```
elc1@ubuntu:~/QEMU/tests$ /home/elc1/QEMU/qemu/bin/debug/native/x86_64-  
linux-user/qemu-x86_64 -d help  
Log items (comma separated):  
out_asm      show generated host assembly code for each compiled TB  
in_asm       show target assembly code for each compiled TB  
op           show micro ops for each compiled TB  
op_opt       show micro ops after optimization  
op_ind       show micro ops before indirect lowering  
int          show interrupts/exceptions in short format  
exec         show trace before each executed TB (lots of logs)  
cpu          show CPU registers before entering a TB (lots of logs)  
fpu          include FPU registers in the 'cpu' logging  
mmu          log MMU-related activities  
pcall        x86 only: show protected mode far calls/returns/exceptions  
cpu_reset    show CPU state before CPU resets  
unimp        log unimplemented functionality  
guest_errors log when the guest OS does something invalid (eg accessing a  
non-existent register)  
page         dump pages at beginning of user mode emulation  
nochain      do not chain compiled TBs so that "exec" and "cpu" show  
complete traces  
strace       log every user-mode syscall, its input, and its result  
trace:PATTERN enable trace events
```

Use "-d trace:help" to get a list of trace events.

```
elc1@ubuntu:~/QEMU/tests$
```

```
/home/elc1/QEMU/qemu/bin/debug/native/x86_64-linux-user/qemu-x86_64 -d  
strace -D /home/elc1/QEMU/tests/logfile-stream-x86_64 ./stream-x86
```

Explanation on the above command

Path to qemu-x86_64: /home/elc1/QEMU/qemu/bin/debug/native/x86_64-linux-user/qemu-x86_64

Type of Log: -d strace

Path to Output file: -D /home/elc1/QEMU/tests/logfile-stream-x86_64

*This will create the logfile in the given location. For example here -
/home/elc1/QEMU/tests/*

Output file name: logfile-stream-x86_64

Executable file name: ./stream-x86

2) ARM -32bit

Install arm compiler: `sudo apt-get install gcc-arm-none-eabi`

a) Compile the program

```
elc1@ubuntu:~/QEMU/tests$ arm-none-eabi-gcc --specs=rdimon.specs  
filename.c -o filename-arm -static
```

b) Check the type of the binary thus generated (output is shown below)

```
elc1@ubuntu:~/QEMU/tests$ file filename-arm  
filename-arm: ELF 32-bit LSB executable, ARM, EABI5 version 1 (SYSV),  
statically linked, with debug_info, not stripped
```

c) (not necessary – if want to see the output)Execute the binary on emulated ARM architecture using qemu

```
/home/elc1/QEMU/qemu/bin/debug/native/arm-linux-user/qemu-arm ./filename -  
arm
```

d) Generate the instruction trace along with running the executable on emulated x86 architecture.

-d flag specifies the type of logs required (it will help to generate the log). The entire list can be obtained by specifying **-d help**. We will use **-d in_asm**.

-D flag specifies the location where the logs should be written.

Use the following command(It will generate the logfile-arm)

```
elc1@ubuntu:~/QEMU/tests$ /home/elc1/QEMU/qemu/bin/debug/native/arm-  
linux-user/qemu-arm -d in_asm -D /home/elc1/QEMU/tests/logfilename  
./filename-arm
```

Explanation on the above command

Path to qemu-arm: `/home/elc1/QEMU/qemu/bin/debug/native/arm-linux-user/qemu-arm`

Type of Log: `-d in_asm`

Path to Output file: `/home/elc1/QEMU/tests/`

*this will create the logfile in the given location. For example here -
/home/elc1/QEMU/tests/*

Output file name: logfilename
Executable file name: ./filename-arm

3) ARM -64bit

Install arm-64bit compiler: `sudo apt-get install gcc-aarch64-linux-gnu g++-aarch64-linux-gnu`

I. compile the program

```
elc1@ubuntu:~/QEMU/tests$ aarch64-linux-gnu-gcc hello.c -o hello
```

II. Check the type of the binary thus generated (output is shown below)

a. compile the program *dynamically* – (already done in step I.)

```
elc1@ubuntu:~/QEMU/tests$ file hello
```

```
64-bit LSB executable, ARM aarch64, version 1 (SYSV), dynamically  
linked, interpreter /lib/ld-linux-aarch64.so.1, for GNU/Linux 3.7.0,  
BuildID[sha1]=0a161541c986a6a5ea1cea24eb19579ce9f64fdb, not  
stripped
```

b. compile the program *statically*

```
elc1@ubuntu:~/QEMU/tests$ aarch64-linux-gnu-gcc hello.c -o hello -  
static
```

```
elc1@ubuntu:~/QEMU/tests$ file hello
```

```
hello: ELF 64-bit LSB executable, ARM aarch64, version 1 (SYSV),  
statically linked, for GNU/Linux 3.7.0,  
BuildID[sha1]=dc9c2aac0c174d49749a1b3b47175f7a759547da, not  
stripped
```

III. (not necessary – if want to see the output)Execute the binary on emulated ARM architecture using qemu

```
$ /home/elc1/QEMU/qemu/bin/debug/native/aarch64-linux-user /qemu-  
aarch64./hello
```

IV. Generate the instruction trace along with running the executable on emulated x86 architecture.

-d flag specifies the type of logs required (it will help to generate the log). The entire list can be obtained by specifying -d help. We will use -d in_asm.

**-D flag specifies the location where the logs should be written.
Use the following command(It will generate the logfile-arm)**

```
elc1@ubuntu:~/QEMU/tests$  
/home/elc1/QEMU/qemu/bin/debug/native/aarch64-linux-user /qemu-aarch64  
-d in_asm -D /home/elc1/QEMU/tests/logfile-arm64 ./hello  
Hello world! - this will create the logfile in the given location.For example here -  
/home/elc1/QEMU/tests/
```

4) PowerPc -32bit

Install arm compiler: `sudo apt-get install gcc-4.8-powerpc-linux-gnu`

I. compile the program

```
elc1@ubuntu:~/QEMU/tests$ powerpc-linux-gnu-gcc-4.8 hello.c -o hello
```

II. Check the type of the binary thus generated (output is shown below)

a. compile the program *dynamically* – *already done in above step*

```
elc1@ubuntu:~/QEMU/tests$ file hello  
hello: ELF 32-bit MSB executable, PowerPC or cisco 4500, version 1  
(SYSV), dynamically linked, interpreter /lib/ld.so.1, for GNU/Linux 3.2.0,  
BuildID[sha1]=2d8db2bb6dc97b29db5527e284bb0d56cf71f3b6, not  
stripped
```

b. compile the program *statically*

```
elc1@ubuntu:~/QEMU/tests$ powerpc-linux-gnu-gcc-4.8 hello.c -o  
hello -static  
elc1@ubuntu:~/QEMU/tests$ file hello  
hello: ELF 32-bit MSB executable, PowerPC or cisco 4500, version 1  
(SYSV), statically linked, for GNU/Linux 3.2.0,  
BuildID[sha1]=081f2652a0604602668cecf1f1011f0bd17b5756, not  
stripped
```

III. (not necessary – if want to see the output)Execute the binary on emulated architecture using qemu

```
$ /home/elc1/QEMU/qemu/bin/debug/native/ppc-linux-user/qemu-ppc ./hello
```

IV. **Generate the instruction trace along with running the executable on emulated x86 architecture.**

-d flag specifies the type of logs required (it will help to generate the log). The entire list can be obtained by specifying **-d help**. We will use **-d in_asm**.

-D flag specifies the location where the logs should be written.

Use the following command(It will generate the logfile-arm)

```
elc1@ubuntu:~/QEMU/tests$ /home/elc1/QEMU/qemu/bin/debug/native/ppc-  
linux-user/qemu-ppc -d in_asm -D /home/elc1/QEMU/tests/logfile-pp32  
./hello
```

Hello world! - *this will create the logfile in the given location. For example here - /home/elc1/QEMU/tests/*

5) PowerPc -64bit

Install arm compiler: `sudo apt-get install gcc-4.8-powerpc64le-linux-gnu`

I. **compile the program**

```
elc1@ubuntu:~/QEMU/tests$ powerpc64le-linux-gnu-gcc-4.8 hello.c -o hello-  
ppc64
```

II. **Check the type of the binary thus generated (output is shown below)**

a. **compile the program *dynamically*- (already done in above step)**

```
elc1@ubuntu:~/QEMU/tests$ file hello-ppc64
```

```
hello-ppc64: ELF 64-bit LSB executable, 64-bit PowerPC or cisco 7500,  
version 1 (GNU/Linux), dynamically linked for GNU/Linux 3.2.0,  
BuildID[sha1]=1a89598dc9ecc38b264d9a0e22741e422866dbd, not  
stripped
```

b. **compile the program *statically***

```
elc1@ubuntu:~/QEMU/tests$ powerpc64le-linux-gnu-gcc-4.8 hello.c -o  
hello-ppc64 -static
```

```
elc1@ubuntu:~/QEMU/tests$ file hello-ppc64
```

```
hello-ppc64: ELF 64-bit LSB executable, 64-bit PowerPC or cisco 7500,  
version 1 (GNU/Linux), statically linked, for GNU/Linux 3.2.0,  
BuildID[sha1]=1a89598dc9ecc38b264d9a0e22741e422866dbd, not  
stripped
```

III. (not necessary – if want to see the output)Execute the binary on emulated ARM architecture using qemu

```
$ /home/elc1/QEMU/qemu/bin/debug/native/ppc64le-linux-user/qemu-ppc64le . /  
hello-ppc64
```

IV. Generate the instruction trace along with running the executable on emulated x86 architecture.

-d flag specifies the type of logs required (it will help to generate the log). The entire list can be obtained by specifying -d help. We will use -d in_asm.

-D flag specifies the location where the logs should be written.

Use the following command(It will generate the logfile-arm)

```
elc1@ubuntu:~/QEMU/tests$ /home/elc1/QEMU/qemu/bin/debug/native/  
ppc64le-linux-user/qemu-ppc64le -d in_asm -D  
/home/elc1/QEMU/tests/logfile-ppc64 ./hello-ppc64  
Hello world! - this will create the logfile in the given location.For example  
here - /home/elc1/QEMU/tests/
```

49 VisualSim Gem5-Arm Integration

Note: To build gem5, you will need the following software:

- *git*
- *gcc/g++ (version >=5)*
- *Python (3.6+),*
- *SCons(3.0 or greater),*
- *SWIG,*
- *zlib,*
- *m4, and lastly*
- *protobuf (2.1+) if you want trace capture and playback support.*

Please see http://www.gem5.org/documentation/general_docs/building for more details concerning the minimum versions of the aforementioned tools.

The below information specify the gem5 version and the gem5 build on OS

Gem5 - :
Branches: stable - v21.0.0.0
package - git clone <https://gem5.googlesource.com/public/gem5>
OS - Centos-8.3
python version - python 3.6
gcc version - gcc 8.3

49.1 Installation steps for Ubuntu OS

Assumption: The user has installed Java version 14 or later and VisualSim Architect.

1. \$ sudo apt install git
2. \$ sudo apt install build-essential git m4 scons zlib1g zlib1g-dev libprotobuf-dev protobuf-compiler libprotoc-dev libgoogle-perftools-dev python3-dev python python3-six python-is-python3 libboost-all-dev pkg-config
3. \$ sudo apt-get install swig
4. Connect to gem5 directory and type
 - a. \$ scons build/ARM/gem5.opt -j2

49.2 Installation steps for CentOS 8.3

Assumption: The user has installed Java version 14 or later and VisualSim Architect.

1. \$ sudo yum groupinstall "Development Tools"

2. \$ sudo dnf update
3. \$ sudo dnf config-manager --set-enabled powertools
4. \$ sudo yum install swig
5. \$ sudo yum install zlib-devel
6. \$ python --version
7. Python 3.6.8
8. Note: *(optional) If python --version does not points to python3.6 or more, then create a symbolic links as follow -:*
 - a. \$ which python
/usr/bin/python
 - b. \$ which python3.6
/usr/bin/python3.6
 - c. \$ sudo ln -s /usr/bin/python3.6 /usr/bin/python
9. \$ sudo yum install python3-devel
10. \$ sudo python -m pip install scon
11. \$ sudo dnf -y install protobuf-devel

<i>On cmdline: - Installing:</i>				
a.	protobuf-devel	x86_64	3.5.0-13.el8	powertools 357 k
<i>Installing dependencies:</i>				
b.	protobuf	x86_64	3.5.0-13.el8	appstream 892 k
c.	protobuf-compiler	x86_64	3.5.0-13.el8	powertools 789 k
12. \$ sudo dnf install https://extras.getpagespeed.com/release-el8-latest.rpm
13. \$ sudo dnf install gperftools-devel
14. \$ sudo yum install libpng-devel
15. \$ sudo yum -y install hdf5-devel
16. Connect to gem5 directory and type
 - a. \$ scon build/ARM/gem5.opt -j2

49.3 Run the Gem5 with Visualsim

- 1) Connect to gem5 directory on terminal and type
\$./interactive_sim.py

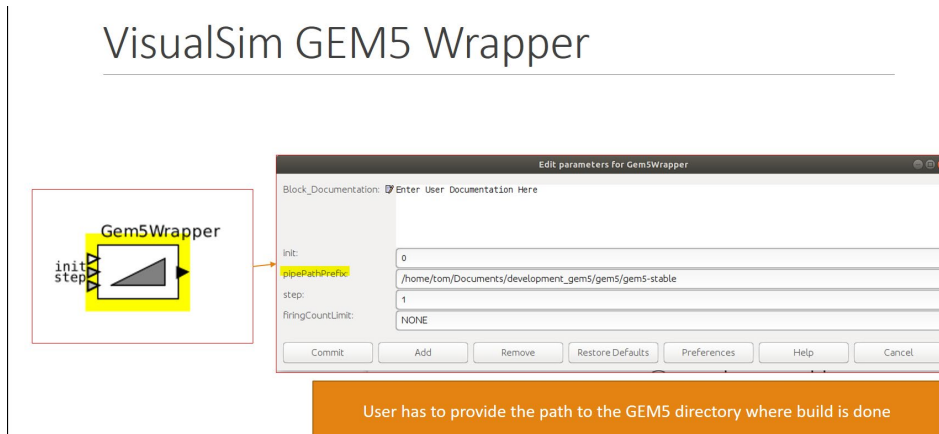
```
[elc@localhost gem5]$ ./interactive_sim.py
starting the simulation!!!
gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 21.0.0.0
gem5 compiled Apr 23 2021 11:17:02
gem5 started Apr 30 2021 03:44:49
gem5 executing on localhost.localdomain, pid 3124
command line: ./build/ARM/gem5.opt --debug-start=1 --debug-flags=DRAM --interactive ./configs/example/se_vs.py --c
pu-type=TimingSimpleCPU --cpu-clock=1GHz --sys-clock=1GHz --caches --l1i_size=16kB --l1d_size=16kB --mem-type=DDR3
_1600 8x8 -c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt -outfile ../MiBench/consumer/jp
eg/output_large_encode.jpeg ../MiBench/consumer/jpeg/input_large.ppm'

warn: membus.slave is deprecated. `slave' is now called `cpu_side_ports'
warn: membus.slave is deprecated. `slave' is now called `cpu_side_ports'
warn: membus.slave is deprecated. `slave' is now called `cpu_side_ports'
warn: membus.slave is deprecated. `slave' is now called `cpu_side_ports'
warn: membus.slave is deprecated. `slave' is now called `cpu_side_ports'
Global frequency set at 1000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote.gdb: listening for remote gdb on port 7000
Redirecting stdout
```

- 2) Now open the model from VisualSim - [demo/interfaces/gem5/gem5_demo.xml](#)

- Specify the gem5 folder path in *GEM5Wrapper* parameter *pipePathPrefix* in the model.



- Run the model.

-----*****-----

49.4 Trace Generation from Gem5:

- Generate trace using debug flags – In gem5 these are the flags used
 - DRAM** debug flag – gives memory details
 - Exec** debug flag - based on the exact instruction the CPU is executing, shows details of how each instruction is executed by the simulated CPU.
- Edit *interactive_sim.py*. Enable the **Exec** flag as shown below (**DRAM** flag is enabled by default).

- Now run the *interactive_sim.py* again (same steps as described in section 49.3)
- The output is generated in file *temp_pipe*, in gem5 directory.

-----*****-----

49.5 Debug Gem5 using gdb:

- \$ `gdb --args ./build/ARM/gem5.opt`
- (gdb) `run --debug-break=1000 --debug-flags=DRAM --interactive ./configs/example/se_vs.py --cpu-type=TimingSimpleCPU --cpu-clock=1GHz --sys-clock=1GHz --caches --l1i_size=16kB --l1d_size=16kB --mem-`

```
type=DDR3_1600_8x8 -c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o ' -dct int -progressive -opt -outfile
../MiBench/consumer/jpeg/output_large_encode.jpeg ../MiBench/consumer/jpeg/input_large.ppm'
```

- 3) Run the visualsim model
- 4) Debug the code using gdb commands such as (n, p, f, bt, step, b main, c)
- 5) After debugging type **continue** or **c** on the terminal, for rest of iteration to finished up
- 6) Plots will be displayed.
- 7) For more information refer:

https://www.gem5.org/documentation/general_docs/debugging_and_testing/debugging/debugger_based_debugging

command line

```
elc1@ubuntu:~/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03$ gdb --args
./build/ARM/gem5.opt
Reading symbols from ./build/ARM/gem5.opt...done.
(gdb) run --debug-break=1000 --debug-flags=DRAM --interactive
./configs/example/interactive_se.py --cpu-type=TimingSimpleCPU --cpu-clock=1GHz --
sys-clock=1GHz --caches --l1_size=16kB --l1d_size=16kB --mem-type=DDR3_1600_x64 -c
../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o ' -dct int -progressive -opt -outfile
../MiBench/consumer/jpeg/output_large_encode.jpeg
../MiBench/consumer/jpeg/input_large.ppm'
Starting program: /home/elc1/gem5/gem5-ptolemy-master/gem5-
stable_2015_09_03/build/ARM/gem5.opt --debug-break=1000 --debug-flags=DRAM --
interactive ./configs/example/interactive_se.py --cpu-type=TimingSimpleCPU --cpu-
clock=1GHz --sys-clock=1GHz --caches --l1_size=16kB --l1d_size=16kB --mem-
type=DDR3_1600_x64 -c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o ' -dct int -
progressive -opt -outfile ../MiBench/consumer/jpeg/output_large_encode.jpeg
../MiBench/consumer/jpeg/input_large.ppm'
```

[Thread debugging using libthread_db enabled]
Using host libthread_db library "/lib/x86_64-linux-gnu/libthread_db.so.1".
gem5 Simulator System. <http://gem5.org>
gem5 is copyrighted software; use the --copyright option for details.

gem5 compiled Sep 22 2020 19:37:46
gem5 started Sep 23 2020 00:46:20

```
gem5 compiled Sep 22 2020 19:37:46
gem5 started Sep 23 2020 00:46:20
gem5 executing on ubuntu
command line: /home/elc1/gem5/gem5-ptolemy-master/gem5-
stable_2015_09_03/build/ARM/gem5.opt --debug-break=1000 --debug-flags=DRAM --
interactive ./configs/example/interactive_se.py --cpu-type=TimingSimpleCPU --cpu-
clock=1GHz --sys-clock=1GHz --caches --l1_size=16kB --l1d_size=16kB --mem-
type=DDR3_1600_x64 -c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o ' -dct int -
progressive -opt -outfile ../MiBench/consumer/jpeg/output_large_encode.jpeg
../MiBench/consumer/jpeg/input_large.ppm'
```

```
warn: need to stop all queues
Global frequency set at 1000000000000 ticks per second
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned
(512 Mbytes)
0: system.mem_ctrls: Memory capacity 536870912 (536870912) bytes
0: system.mem_ctrls: Row buffer size 8192 bytes with 128 columns per row buffer
0: system.remote_gdb.listener: listening for remote gdb #0 on port 7000
Redirecting stdout
```

s range

es

per row buffer

0

---Now run the VisualSim here

49.6 Deb

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Reference Guide

```
Redirecting stdout
iteration: 0

Program received signal SIGTRAP, Trace/breakpoint trap.
0x00007ffff5e5a237 in kill () at ../sysdeps/unix/syscall-template.S:78
78      ../sysdeps/unix/syscall-template.S: No such file or directory.
(gdb) b main
Breakpoint 1 at 0x555555de69e0: file build/ARM/sim/main.cc, line 42.
(gdb) n
kill () at ../sysdeps/unix/syscall-template.S:79
79      in ../sysdeps/unix/syscall-template.S
(gdb) n
GlobalEvent::BarrierEvent::process (this=0x555555845280) at
build/ARM/sim/global_event.cc:136
136      globalBarrier();
(gdb) n
137      }
(gdb)
EventQueue::serviceOne (this=this@entry=0x5555558498320) at
build/ARM/sim/eventq.cc:229
229      if (event->isExitEvent()) {
(gdb) p eventQueue
No symbol "eventQueue" in current context.
(gdb) n
238      if (event->flags.isSet(Event::AutoDelete) && !event-
>scheduled())
```

```
238      if (event->flags.isSet(Event::AutoDelete) && !event-
!event->scheduled())
(gdb) print SimObject::find("system.cpu")
$1 = (SimObject *) 0x5555558bedb80
(gdb) print (BaseCPU *) SimObject::find("system.cpu")
$2 = (BaseCPU *) 0x5555558bedb80
(gdb) $3p instCnt
Undefined command: "$3p". Try "help".
(gdb) p $3->instCnt
History has not yet reached $3.
(gdb) print (BaseCPU *) SimObject::find("system.cpu")
$3 = (BaseCPU *) 0x5555558bedb80
(gdb) p $3->instCnt
$4 = 0
(gdb)
```

(gdb) c
Continuing.

To continue the execution

```
(gdb) c
Continuing.
iteration 0 finished
iteration: 1
iteration 1 finished
iteration: 2
iteration 2 finished
iteration: 3
iteration 3 finished
iteration: 4
iteration 4 finished
iteration: 5
iteration 5 finished
iteration: 6
iteration 6 finished
iteration: 7
iteration 7 finished
iteration: 8
iteration 8 finished
iteration: 9
iteration 9 finished
iteration: 10
iteration 10 finished
```

Show plots

graphical gdb:

- 1) \$ gdb -tui --args ./build/ARM/gem5.opt
- 2) (gdb) run --debug-break=1000 --debug-flags=DRAM --interactive ./configs/example/se_vs.py --cpu-type=TimingSimpleCPU --cpu-clock=1GHz --sys-clock=1GHz --caches --li_size=16kB --l1d_size=16kB --mem-type=DDR3_1600_8x8 -c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt -outfile ../MiBench/consumer/jpeg/output_large_encode.jpeg ../MiBench/consumer/jpeg/input_large.ppm'
- 3) Run the visualsim model
- 4) Debug the code using gdb commands such as (n, p, f, bt, step, b main, c)
- 5) After debugging type **continue** or **c** on the terminal, for rest of iteration to finished up
- 6) Plots will be displayed.
- 7) For more information refer the site : <http://beej.us/guide/bggdb/#qref>
- 8) **NOTE:** All the normal **gdb** commands will work in GUI mode, and additionally the arrow keys and pgup/pgdown keys will scroll the source window (when it has focus, which it does by default).

Graphical gdb

```
elc1@ubuntu:~/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03$ gdb -tui --args ./build/ARM/gem5.opt
```

```
File Edit View Search Terminal Help
build/ARM/sim/main.cc
42 {
43     int ret;
44
45     // Initialize m5 special signal handling.
46     initSignals();
47
48     Py_SetProgramName(argv[0]);
49
50     // initialize embedded Python interpreter
51     Py_Initialize();
52
53     // Initialize the embedded m5 python library
54     ret = initM5Python();
55
56     if (ret == 0) {
57         // start m5
58         ret = m5Main(argc, argv);
59     }
60 }
```

```
elc1@ubuntu: ~/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03
File Edit View Search Terminal Help
59 }
60 }
multi-thre Thread 0x7ffff7fdd4 In: L?? PC: ??
(gdb)
(gdb) run --debug-break=1000 --debug-flags=DRAM --interactive ./configs/example/interactive_se.py --cpu-type=TimingSimpleCPU --cpu-clock=1GHz --sys-clock=1GHz --caches --li_size=16kB --l1d_size=16kB --mem-type=DDR3_1600_X64 -c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt -outfile ../MiBench/consumer/jpeg/output_large_encode.jpeg ../MiBench/consumer/jpeg/input_large.ppm' Starting program: /home/elc1/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03/build/ARM/gem5.opt --debug-break=1000 --debug-flags=DRAM --interactive ./configs/example/interactive_se.py --cpu-type=TimingSimpleCPU --cpu-clock=1GHz --sys-clock=1GHz --caches --li_size=16kB --l1d_size=16kB --mem-type=DDR3_1600_X64 -c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt -outfile ../MiBench/consumer/jpeg/output_large_encode.jpeg ../MiBench/consumer/jpeg/input_large.ppm'
[Thread debugging using libthread_db enabled]
Using host libthread_db library "/lib/x86_64-linux-gnu/libthread_db.so.1".
gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 compiled Sep 22 2020 19:37:46
gem5 started Sep 23 2020 01:26:24
gem5 executing on ubuntu
command line: /home/elc1/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03/build/ARM/gem5.opt --debug-break=1000 --debug-flags=DRAM --interactive ./configs/example/interactive_se.py --cpu-type=TimingSimpleCPU --cpu-clock=1GHz --sys-clock=1GHz --caches --li_size=16kB --l1d_size=16kB --mem-type=DDR3_1600_X64 -c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt -outfile ../MiBench/consumer/jpeg/output_large_encode.jpeg ../MiBench/consumer/jpeg/input_large.ppm'

warn: need to stop all queues
Global frequency set at 1000000000000 ticks per second
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.mem_ctrls: Memory capacity 536870912 (536870912) bytes
0: system.mem_ctrls: Row buffer size 8192 bytes with 128 columns per row buffer
0: system.remote_gdb.listener: listening for remote gdb #0 on port 7001
Redirecting stdout
```

```

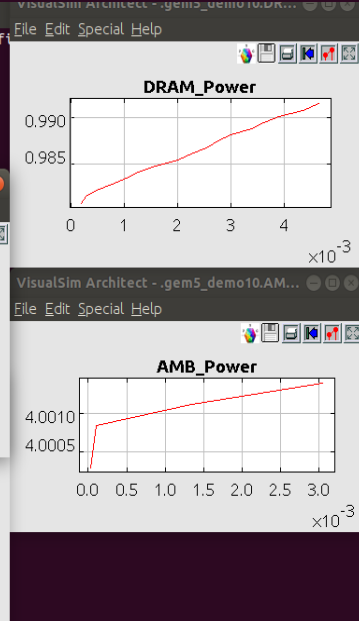
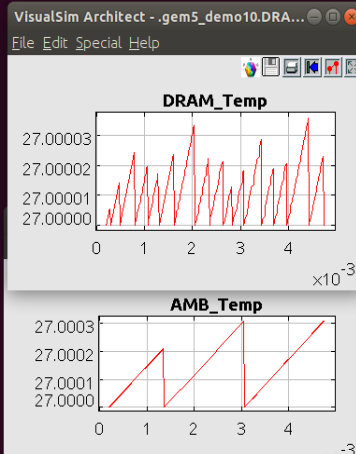
elc1@ubuntu: ~/gem5/ptolemy-master/gem5-stable_2015_09_03
File Edit View Search Terminal Help
60 build/ARM/sim/eventq.cc
221 }
222
223 // handle action
224 if (!event->squashed()) {
225 // forward current cycle to the time when this event occurs.
226 setCurTick(event->when());
227
228 event->process();
229 } if (event->isExitEvent()) {
230 assert(!event->flags.isSet(Event::AutoDelete) ||
231 !event->flags.isSet(Event::IsMainQueue)); // would be silly
232 return event;
233 }
234 } else {
235 event->flags.clear(Event::Squashed);
236 }
237
238 if (event->flags.isSet(Event::AutoDelete) && !event->scheduled())
239 delete event;
e ./configs/example/interactive_se.py --cpu-type=TimingSimpleCPU --cpu-clock=1GHz --sys-clock=1GHz --caches --l1i_size=16kB --l1d_size=16kB --
mem-type=DDR3_1600_x64 -c ./MiBenchEventQueue::serviceOne -dct int -progressive -opt -outfile ./MiBench/d/229 PC: 0x55555616b2b1e
kill () at ./sysdeps/unix/syscall-template.S:79
(gdb) n
GlobalEvent::BarrierEvent::process (this=0x5555584a5280) at build/ARM/sim/global_event.cc:136
(gdb) f
#0 GlobalEvent::BarrierEvent::process (this=0x5555584a5280) at build/ARM/sim/global_event.cc:136
(gdb) n
(gdb) n
EventQueue::serviceOne (this=this@entry=0x555558498320) at build/ARM/sim/eventq.cc:229
(gdb) p event

```

```

File Edit View Search Terminal Help
mem-type=DDR3_1600_x64 -c ./MiBenchEventQueue::serviceOne -dct int -progressive -opt -outfile ./MiBench/d/229 PC: 0x55555616b2b1e
(gdb) f
#0 GlobalEvent::BarrierEvent::process (this=0x5555584a5280) at build/ARM/sim/global_event.cc:136
(gdb) n
(gdb) n
EventQueue::serviceOne (this=this@entry=0x555558498320) at build/ARM/sim/eventq.cc:229
(gdb) p event
$1 = (Event *) 0x5555584a5280
(gdb) c
Continuing.
iteration 0 finished
iteration 1 finished
iteration 2 finished
iteration 3 finished
iteration 4 finished
iteration 5 finished
iteration 6 finished
iteration 7 finished
iteration 8 finished
iteration 9 finished
iteration 10 finished

```



49.7 Running the Gem5 in System Call Emulation (SE) Mode

The SE mode simulation focuses on the CPU and memory system, and does not emulate the entire system. In this mode, one only needs to specify the binary file to be simulated. This binary file can be statically/dynamically linked. `configs/examples/se.py` is used for configuring and running simulations in this mode. What follows is probably the simplest example of how to use `se.py`. The binary file to simulate is specified with option `-c`.

- 1) `cd` to the `gem5` directory on terminal and use the below command to run the hello arm executable.

```
a) $ ./build/ARM/gem5.opt ./configs/example/se.py -c ./tests/test-progs/hello/bin/arm/linux/hello
gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.
gem5 compiled Mar  2 2014 00:06:39
gem5 started Mar  4 2014 10:52:10
gem5 executing on $
command line: ./build/ARM/gem5.opt ./configs/example/se.py -c ./tests/test-progs/hello/bin/arm/linux/hello
Global frequency set at 1000000000000 ticks per second
O: system.remote_gdb.listener: listening for remote gdb #0 on port 7000
**** REAL SIMULATION ****
info: Entering event queue @ 0. Starting simulation...
info: Increasing stack size by one page.
Hello world!
Exiting @ tick 3233000 because target called exit()
```

- 2) For statistics refer to this location → `/home/elc1/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03/m5out/stats.txt`
- 3) Detailed Information - http://mail.gem5.org/Running_gem5
- 4) Create your own executable for arm (additional information for trying out more experiments)

Install ARM compiler \$ `sudo apt-get install gcc-arm-linux-gnueabi gcc-aarch64-linux-gnu`

- a. Compile the C program : \$ `arm-linux-gnueabi-gcc filename.c -o filename-arm -static`
- b. \$ `file filename`
- c. Run the gem5 \$ `./build/ARM/gem5.opt ./configs/example/se.py -c path to the arm executables`

-----*****-----

49.8 Run the Gem5 (SE mode) in Multi-Core

- 1) cd to the gem5 directory on terminal and use the below command to run the hello arm executable.

```

elc1@ubuntu:~/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03$ ./build/ARM/gem5.opt
configs/example/se.py --num-cpus=2 -c './tests/test-progs/hello/bin/arm/linux/hello;./tests/test-
progs/hello/bin/arm/linux/hello'
gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 compiled Sep 22 2020 19:37:46
gem5 started Nov 6 2020 00:42:37
gem5 executing on ubuntu
command line: ./build/ARM/gem5.opt configs/example/se.py --num-cpus=2 -c './tests/test-
progs/hello/bin/arm/linux/hello;./tests/test-progs/hello/bin/arm/linux/hello'
Global frequency set at 1000000000000 ticks per second
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
O: system.remote_gdb.listener: listening for remote gdb #0 on port 7000
O: system.remote_gdb.listener: listening for remote gdb #1 on port 7001
*** REAL SIMULATION ***
info: Entering event queue @ 0. Starting simulation...
Hello world!
Hello world!
Exiting @ tick 2924500 because target called exit()

```

- 2) For statistics refer → m5_out/Stats.txt
- 3) Create your own executable for arm (additional information for trying out more experiments)

```

Install ARM compiler
$ sudo apt-get install gcc-arm-linux-gnueabi gcc-aarch64-linux-gnu

```

- a. Compile the C program : `$ arm-linux-gnueabi-gcc filename.c -o filename-arm -static`
- b. `$ file filename`
- c. Run the gem5

```

$ ./build/ARM/gem5.opt configs/example/se.py --num-cpus=2 -c 'path to the testcode; path to the testcode '

```

-----*****-----

49.9 Running the Gem5 in Full System (FS) Mode

In the FS mode, the complete system can be modeled in an OS-based simulation environment. In order to simulate using the FS mode, For full system mode, you can use the file `configs/example/fs.py` for configuration and simulation.. After downloading and extracting ARM full system files, we let gem5 know the location of our disks and binaries directories, i.e. the path to the `aarch-system-2014-10` directory.

49.9.1.1 Booting Linux

- Detailed information :

https://www.youtube.com/watch?v=gd_DtxQD5kc&feature=youtu.be&ab_channel=BenPayne

- http://mail.gem5.org/Running_gem5

49.9.1.1.1 Steps to download the full system file

- 1) Connect to gem5 directory
- 2) `elc1@ubuntu:~/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03$ mkdir full_system_images`
- 3) `elc1@ubuntu:~/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03$ cd full_system_images/`
- 4) `elc1@ubuntu:~/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03/full_system_images$ wget http://www.m5sim.org/dist/current/arm/aarch-system-2014-10.tar.bz2`

```
--2020-10-09 06:27:43-- http://www.m5sim.org/dist/current/arm/aarch-system-2014-10.tar.bz2
Resolving www.m5sim.org (www.m5sim.org)... 141.212.113.198
Connecting to www.m5sim.org (www.m5sim.org)|141.212.113.198|:80... connected.
HTTP request sent, awaiting response... 200 OK
Length: 280811500 (268M) [application/x-bzip2]
Saving to: 'aarch-system-2014-10.tar.bz2'
aarch-system-2014-10. 100%[=====>] 267.80M 4.36MB/s in 50s
2020-10-09 06:28:35 (5.30 MB/s) - 'aarch-system-2014-10.tar.bz2' saved [280811500/280811500]
```
- 5) `elc1@ubuntu:~/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03/full_system_images$ tar jxf aarch-system-2014-10.tar.bz2`
- 6) `echo "export M5_PATH=/home/elc1/gem5/gem5-ptolemy-master/gem5stable_2015_09_03/full_system_images/"`
`>> ~/.bashrc`
- 7) **Note: M5_PATH=path to the full system image directory**
- 8) `elc1@ubuntu:~/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03/full_system_images$ source ~/.bashrc`
-to refresh it
- 9) `elc1@ubuntu:~/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03/full_system_images$ echo $M5_PATH`
`/home/elc1/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03/full_system_images`

-----*****-----

49.9.1.1.2 Steps to boot Linux on gem5

- 1) \$ cd /home/elc1/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03
- 2) \$./build/ARM/gem5.opt configs/example/fs.py --disk-image=/home/elc1/full_system_image/disks/aarch32-ubuntu-natty-headless.img

gem5 Simulator System

Copyright (c) 2001-2006
 The Regents of The University of Michigan
 All Rights Reserved

```
gem5 compiled Aug 16 2006 18:51:57
gem5 started Wed Aug 16 21:53:38 2006
gem5 executing on zeeb
command line: ./build/ARM/gem5.debug configs/example/fs.py
  0: system.tsunami.io.rtc: Real-time clock set to Sun Jan  1 00:00:00 2006
Listening for console connection on port 3456
0: system.remote_gdb.listener: listening for remote gdb #0 on port 7000
warn: Entering event queue @ 0. Starting simulation...
<...simulation continues...>
```

Note: --disk-image=path to the full system image directory

By default, the fs.py script boots Linux and starts a shell on the system console. To keep console traffic separate from simulator input and output, this simulated console is associated with a TCP port. To interact with the console, you must connect to the port using a program such as **telnet**, for example:

Open new terminal and type

- 3) \$ telnet localhost 3456

Here 3456 is a port number on gem5 terminal

```
elc1@ubuntu:~$ telnet 127.0.0.1 3457
Trying 127.0.0.1...
Connected to 127.0.0.1.
Escape character is '^]'.
==== m5 slave terminal: Terminal 0 ====
Booting Linux on physical CPU 0x0
Initializing cgroup subsys cpuset
Linux version 3.13.0-rc2 (tony@vamp) (gcc version 4.8.2 (Ubuntu/Linaro 4.8.2-16ubuntu4) ) #1 SMP PREEMPT Mon Oct 13 15:09:23 EDT 2014
Kernel was built at commit id ''
CPU: ARMv7 Processor [410fc0f0] revision 0 (ARMv7), cr=10c53c7d
CPU: PIPT / VIPT nonaliasing data cache, VIPT aliasing instruction cache
Machine model: V2P-CA15
bootconsole [earlycon0] enabled
```


Memory policy: Data cache writealloc
kdebugv2m: Following are test values to confirm proper working
kdebugv2m: Ranges 42000000 0
kdebugv2m: Regs 30000000 1000000
kdebugv2m: Virtual-Reg f0000000
kdebugv2m: pci node addr_cells 3
kdebugv2m: pci node size_cells 2
kdebugv2m: motherboard addr_cells 2
On node 0 totalpages: 131072
free_area_init_node: node 0, pgdat 8072dcc0, node_mem_map 8078f000
Normal zone: 1024 pages used for memmap
Normal zone: 0 pages reserved
Normal zone: 131072 pages, LIFO batch:31
sched_clock: 32 bits at 24MHz, resolution 41ns, wraps every 178956969942ns
PERCPU: Embedded 8 pages/cpu @80b97000 s11648 r8192 d12928 u32768
pcpu-alloc: s11648 r8192 d12928 u32768 alloc=8*4096
pcpu-alloc: [0] 0
Built 1 zonelists in Zone order, mobility grouping on. Total pages: 130048
Kernel command line: earlyprintk=pl011,0x1c090000 console=ttyAMA0 lpj=19988480 norandmaps rw loglevel=8 mem=512MB root=/dev/sda1
PID hash table entries: 2048 (order: 1, 8192 bytes)
Dentry cache hash table entries: 65536 (order: 6, 262144 bytes)
Inode-cache hash table entries: 32768 (order: 5, 131072 bytes)
Memory: 495584K/524288K available (5248K kernel code, 249K rwdata, 1540K rodata, 295K init, 368K bss, 28704K reserved, 0K highmem)
Virtual kernel memory layout:
vector : 0xffff0000 - 0xffff1000 (4 kB)
fixmap : 0xfff00000 - 0xfffe0000 (896 kB)
vmalloc : 0xa0800000 - 0xff000000 (1512 MB)
lowmem : 0x80000000 - 0xa0000000 (512 MB)
pkmap : 0x7fe00000 - 0x80000000 (2 MB)
modules : 0x7f000000 - 0x7fe00000 (14 MB)
.text : 0x80008000 - 0x806a942c (6790 kB)
.init : 0x806aa000 - 0x806f3d80 (296 kB)
.data : 0x806f4000 - 0x80732754 (250 kB)
.bss : 0x80732754 - 0x8078e9d8 (369 kB)
SLUB: HWalign=64, Order=0-3, MinObjects=0, CPUs=1, Nodes=1
Preemptible hierarchical RCU implementation.
RCU restricting CPUs from NR_CPUS=8 to nr_cpu_ids=1.
NR_IRQS:16 nr_irqs:16 16
Architected cp15 timer(s) running at 25.16MHz (phys).
sched_clock: 56 bits at 25MHz, resolution 39ns, wraps every 2730666655744ns
Switching to timer-based delay loop
Console: colour dummy device 80x30
Calibrating delay loop (skipped) preset value.. 3997.69 BogoMIPS (lpj=19988480)
pid_max: default: 32768 minimum: 301
Mount-cache hash table entries: 512
CPU: Testing write buffer coherency: ok
CPU0: update cpu_power 1024
CPU0: thread -1, cpu 0, socket 0, mpidr 80000000
Setting up static identity map for 0x804fee68 - 0x804fee9c
Brought up 1 CPUs
SMP: Total of 1 processors activated.
CPU: All CPU(s) started in SVC mode.
VFP support v0.3: implementor 41 architecture 4 part 30 variant a rev 0
NET: Registered protocol family 16
DMA: preallocated 256 KiB pool for atomic coherent allocations
of_amba_device_create(): amba_device_add() failed (-19) for /smb/motherboard/iofpga@3,00000000/sysctl@020000
of_amba_device_create(): amba_device_add() failed (-19) for /smb/motherboard/iofpga@3,00000000/aaci@040000
of_amba_device_create(): amba_device_add() failed (-19) for /smb/motherboard/iofpga@3,00000000/mmc@050000
of_amba_device_create(): amba_device_add() failed (-19) for /smb/motherboard/iofpga@3,00000000/uart@0a0000
of_amba_device_create(): amba_device_add() failed (-19) for /smb/motherboard/iofpga@3,00000000/uart@0b0000
of_amba_device_create(): amba_device_add() failed (-19) for /smb/motherboard/iofpga@3,00000000/uart@0c0000

```
of_amba_device_create(): amba_device_add() failed (-19) for /smb/motherboard/iopfpga@3,00000000/wdt@0f0000
hw-breakpoint: Debug register access (0xee113e93) caused undefined instruction on CPU 0
hw-breakpoint: Debug register access (0xee013e90) caused undefined instruction on CPU 0
hw-breakpoint: Debug register access (0xee003e17) caused undefined instruction on CPU 0
hw-breakpoint: CPU 0 failed to disable vector catch
Serial: AMBA PL011 UART driver
1c090000.uart: ttyAMA0 at MMIO 0x1c090000 (irq = 37, base_baud = 0) is a PL011 rev3
console [ttyAMA0] enabled
console [ttyAMA0] enabled
bootconsole [earlycon0] disabled
bootconsole [earlycon0] disabled
PCI host bridge to bus 0000:00
pci_bus 0000:00: root bus resource [io 0x0000-0xffffffff]
pci_bus 0000:00: root bus resource [mem 0x00000000-0xffffffff]
pci_bus 0000:00: root bus resource [bus 00-ff]
pci 0000:00:00.0: [8086:1075] type 00 class 0x020000
pci 0000:00:00.0: reg 0x10: [mem 0x00000000-0x0001ffff]
pci 0000:00:00.0: reg 0x30: [mem 0x00000000-0x000007ff pref]
pci 0000:00:01.0: [8086:7111] type 00 class 0x010185
pci 0000:00:01.0: reg 0x10: [io 0x0000-0x0007]
pci 0000:00:01.0: reg 0x14: [io 0x0000-0x0003]
pci 0000:00:01.0: reg 0x18: [io 0x0000-0x0007]
pci 0000:00:01.0: reg 0x1c: [io 0x0000-0x0003]
pci 0000:00:01.0: reg 0x20: [io 0x0000-0x000f]
pci 0000:00:01.0: reg 0x30: [mem 0x00000000-0x000007ff pref]
PCI: bus0: Fast back to back transfers disabled
pci 0000:00:00.0: BAR 0: assigned [mem 0x40000000-0x4001ffff]
pci 0000:00:00.0: BAR 6: assigned [mem 0x40020000-0x400207ff pref]
pci 0000:00:01.0: BAR 6: assigned [mem 0x40020800-0x40020fff pref]
pci 0000:00:01.0: BAR 4: assigned [io 0x2f000000-0x2f00000f]
pci 0000:00:01.0: BAR 0: assigned [io 0x2f000010-0x2f000017]
pci 0000:00:01.0: BAR 2: assigned [io 0x2f000018-0x2f00001f]
pci 0000:00:01.0: BAR 1: assigned [io 0x2f000020-0x2f000023]
pci 0000:00:01.0: BAR 3: assigned [io 0x2f000024-0x2f000027]
pci_bus 0000:00: resource 4 [io 0x0000-0xffffffff]
pci_bus 0000:00: resource 5 [mem 0x00000000-0xffffffff]
PCI map irq: slot 0, pin 1, devslot 0, irq: 68
PCI map irq: slot 1, pin 2, devslot 1, irq: 69
bio: create slab <bio-0> at 0
vgaarb: loaded
SCSI subsystem initialized
libata version 3.00 loaded.
usbcore: registered new interface driver usbfs
usbcore: registered new interface driver hub
usbcore: registered new device driver usb
pps_core: LinuxPPS API ver. 1 registered
pps_core: Software ver. 5.3.6 - Copyright 2005-2007 Rodolfo Giometti <giometti@linux.it>
PTP clock support registered
Advanced Linux Sound Architecture Driver Initialized.
Switched to clocksource arch_sys_counter
NET: Registered protocol family 2
TCP established hash table entries: 4096 (order: 2, 16384 bytes)
TCP bind hash table entries: 4096 (order: 3, 32768 bytes)
TCP: Hash tables configured (established 4096 bind 4096)
TCP: reno registered
UDP hash table entries: 256 (order: 1, 8192 bytes)
UDP-Lite hash table entries: 256 (order: 1, 8192 bytes)
NET: Registered protocol family 1
RPC: Registered named UNIX socket transport module.
RPC: Registered udp transport module.
RPC: Registered tcp transport module.
```

RPC: Registered tcp NFSv4.1 backchannel transport module.
PCI: CLS 64 bytes, default 64
hw perfevents: enabled with ARmv7_Cortex_A15 PMU driver, 1 counters available
jffs2: version 2.2. (NAND) © 2001-2006 Red Hat, Inc.
msgmni has been set to 967
io scheduler noop registered (default)
brd: module loaded
loop: module loaded
ata_piix 0000:00:01.0: version 2.13
PCI: enabling device 0000:00:01.0 (0040 -> 0041)
scsi0 : ata_piix
scsi1 : ata_piix
ata1: PATA max UDMA/33 cmd 0x2f000010 ctl 0x2f000020 bmdma 0x2f000000 irq 69
ata2: PATA max UDMA/33 cmd 0x2f000018 ctl 0x2f000024 bmdma 0x2f000008 irq 69
e100: Intel(R) PRO/100 Network Driver, 3.5.24-k2-NAPI
e100: Copyright(c) 1999-2006 Intel Corporation
e1000: Intel(R) PRO/1000 Network Driver - version 7.3.21-k8-NAPI
e1000: Copyright (c) 1999-2006 Intel Corporation.
PCI: enabling device 0000:00:00.0 (0040 -> 0042)
ata1.00: ATA-7: M5 IDE Disk , max UDMA/66
ata1.00: 6291936 sectors, multi 0: LBA
ata1.00: configured for UDMA/33
scsi 0:0:0:0: Direct-Access ATA M5 IDE Disk n/a PQ: 0 ANSI: 5
sd 0:0:0:0: [sda] 6291936 512-byte logical blocks: (3.22 GB/3.00 GiB)
sd 0:0:0:0: [sda] Write Protect is off
sd 0:0:0:0: [sda] Mode Sense: 00 3a 00 00
sd 0:0:0:0: [sda] Write cache: disabled, read cache: enabled, doesn't support DPO or FUA
sda: sda1
sd 0:0:0:0: Attached scsi generic sg0 type 0
sd 0:0:0:0: [sda] Attached SCSI disk
e1000 0000:00:00.0 eth0: (PCI:33MHz:32-bit) 00:90:00:00:00:01
e1000 0000:00:00.0 eth0: Intel(R) PRO/1000 Network Connection
e1000e: Intel(R) PRO/1000 Network Driver - 2.3.2-k
e1000e: Copyright(c) 1999 - 2013 Intel Corporation.
igb: Intel(R) Gigabit Ethernet Network Driver - version 5.0.5-k
igb: Copyright (c) 2007-2013 Intel Corporation.
igbvf: Intel(R) Gigabit Virtual Function Network Driver - version 2.0.2-k
igbvf: Copyright (c) 2009 - 2012 Intel Corporation.
ixgbe: Intel(R) 10 Gigabit PCI Express Network Driver - version 3.15.1-k
ixgbe: Copyright (c) 1999-2013 Intel Corporation.
ixgbev: Intel(R) 10 Gigabit PCI Express Virtual Function Network Driver - version 2.11.3-k
ixgbev: Copyright (c) 2009 - 2012 Intel Corporation.
ixgb: Intel(R) PRO/10GbE Network Driver - version 1.0.135-k2-NAPI
ixgb: Copyright (c) 1999-2008 Intel Corporation.
smsc911x: Driver version 2008-10-21
smsc911x 1a000000.ethernet (unregistered net_device): couldn't get clock -2
nxp-isp1760 1b000000.usb: NXP ISP1760 USB Host Controller
nxp-isp1760 1b000000.usb: new USB bus registered, assigned bus number 1
nxp-isp1760 1b000000.usb: Scratch test failed.
nxp-isp1760 1b000000.usb: can't setup: -19
nxp-isp1760 1b000000.usb: USB bus 1 deregistered
usbcore: registered new interface driver usb-storage
mousedev: PS/2 mouse device common for all mice
rtc-pl031 1c170000.rtc: rtc core: registered pl031 as rtc0
usbcore: registered new interface driver usbhid
usbhid: USB HID core driver
ashmem: initialized
logger: created 256K log 'log_main'
logger: created 256K log 'log_events'
logger: created 256K log 'log_radio'
logger: created 256K log 'log_system'

```
oprofile: using timer interrupt.
TCP: cubic registered
NET: Registered protocol family 10
NET: Registered protocol family 17
rtc-pl031 1c170000.rtc: setting system clock to 2009-01-01 00:00:00 UTC (1230768000)
ALSA device list:
  No soundcards found.
input: AT Raw Set 2 keyboard as /devices/smb.14/motherboard.15/iofpga.17/1c060000.kmi/serio0/input/input0
input: touchkitPS/2 eGalax Touchscreen as /devices/smb.14/motherboard.15/iofpga.17/1c070000.kmi/serio1/input/input2
kjournald starting. Commit interval 5 seconds
EXT3-fs (sda1): using internal journal
EXT3-fs (sda1): mounted filesystem with writeback data mode
VFS: Mounted root (ext3 filesystem) on device 8:1.
Freeing unused kernel memory: 292K (806aa000 - 806f3000)
random: init urandom read with 14 bits of entropy available

input: AT Raw Set 2 keyboard as /devices/smb.14/motherboard.15/iofpga.17/1c060000.kmi/serio0/input/input0
input: touchkitPS/2 eGalax Touchscreen as /devices/smb.14/motherboard.15/iofpga.17/1c070000.kmi/serio1/input/input2
kjournald starting. Commit interval 5 seconds
EXT3-fs (sda1): using internal journal
EXT3-fs (sda1): mounted filesystem with writeback data mode
VFS: Mounted root (ext3 filesystem) on device 8:1.
Freeing unused kernel memory: 292K (806aa000 - 806f3000)
random: init urandom read with 14 bits of entropy available

Ubuntu 11.04 gem5sim ttySA0
```

this will take 30 mins

4) gem5sim login: root root

Welcome to Ubuntu 11.04 (GNU/Linux 3.13.0-rc2 armv7l)

* Documentation: <https://help.ubuntu.com/>

The programs included with the Ubuntu system are free software;
the exact distribution terms for each program are described in the
individual files in /usr/share/doc/*/copyright.

Ubuntu comes with ABSOLUTELY NO WARRANTY, to the extent permitted by
applicable law.

```
root@gem5sim:~#
root@gem5sim:~#
```

-----*****-----

50 GEM5 with RISCV

Download the zip file from (details of ftp or github)

Two option for the user:

- 1) Directly run the command without the build – Extract the patch *GEM5_Patch_Java_14.zip* in the Ubuntu and run commands directly from section 50.2
- 2) If the user experiences trouble while running directly without building the gem5 from scratch then follow the steps from the section 50.1

50.1 For Ubuntu 18.04 installation steps

1. Assumption: The user has installed Java 14 and VisualSim 2030.
2. mkdir gem5
3. cd gem5
4. sudo apt-get install gcc-riscv64-linux-gnu g++-riscv64-linux-gnu
5. sudo apt install build-essential git m4 scons zlib1g zlib1g-dev libprotobuf-dev protobuf-compiler libprotoc-dev libgoogle-perftools-dev python-dev python
6. sudo apt-get install libpython3.8-dev
7. sudo apt-get install swig --- if swig is not installed
8. scons build/RISCV/gem5.opt -jn -> (n = 1,2,3number of processor)
9. if there is no error on the terminal then build is complete.

50.2 Run the Gem5 <-> VisualSim (normal run without debugger)

- 1) cd to the gem5 location on terminal and type

```
$. /interactive_sim.py  
(this start the gem5 simulator)
```

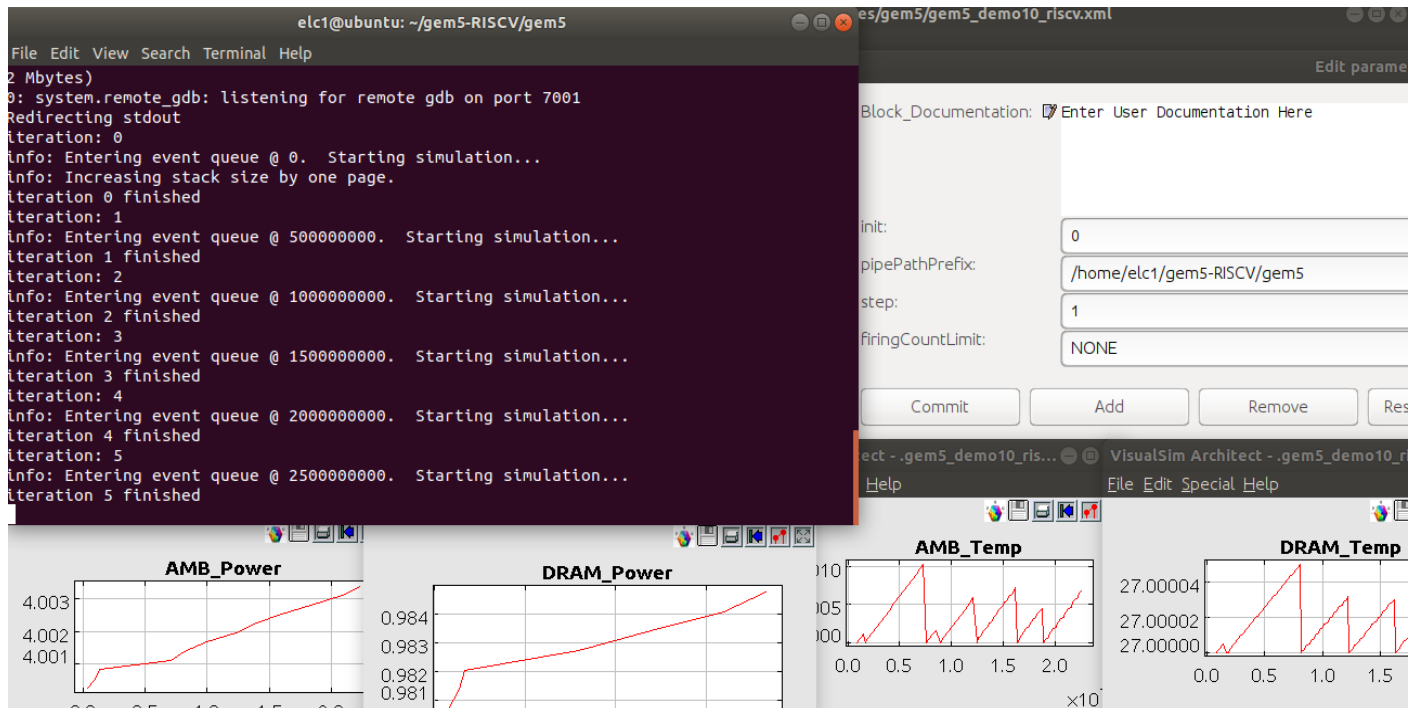
- 2) After **Redirecting Stdout** shows on terminal, run visualsim model by following below steps
- 3) Now open the model in the VisualSim under demo/interfaces/gem5/gem5_demo.xml
- 4) Give the correct path in gem5 wrapper block parameter where gem5 is located.
- 5) Provide parameter gem5iteration = integer number (of your choice)
- 6) Run the model

7) Check the plots display and below screenshots

```
e1c1@ubuntu:~/gem5-RISCV/gem5$ ./interactive_sim.py
starting the simulation!!!
gem5 Simulator System.  http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 20.1.0.0
gem5 compiled Nov  2 2020 17:05:29
gem5 started Nov  6 2020 14:07:36
gem5 executing on ubuntu, pid 4214
command line: ./build/RISCV/gem5.opt --debug-start=1 --debug-flags=DRAM --interac
tive ./configs/example/se_vs.py --cpu-type=TimingSimpleCPU --cpu-clock=1GHz --s
ys-clock=1GHz --caches --l1i_size=16kB --l1d_size=16kB --mem-type=DDR3_1600_8x8
-c ./MiBench/consumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt -outfil
e ./MiBench/consumer/jpeg/output_large_encode.jpeg ./MiBench/consumer/jpeg/inp
ut_large.ppm'

warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.master is deprecated. `master` is now called `mem_side_ports`
Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and p
df.
warn: DRAM device capacity (8192 Mbytes) does not match the address range assign
ed (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
Redirecting stdout
```



50.3 Run with debugger -command line:

- 1) cd to gem5 directory \$ **`gdb --args ./build/RISCV/gem5.opt`**
- 2) wait for gdb to open up , use run command (step 3) after gdb shows
- 3) (gdb) **`run --debug-break=1000 --debug-flags=DRAM --interactive ./configs/example/se_vs.py --cpu-type=TimingSimpleCPU --cpu-clock=1GHz --sys-clock=1GHz --caches --l1i_size=16kB --l1d_size=16kB --mem-type=DDR3_1600_8x8 -c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt -outfile ../MiBench/consumer/jpeg/output_large_encode.jpeg ../MiBench/consumer/jpeg/input_large.ppm'`**
- 4) Wait for gdb() to show on terminal
- 5) After **Redirecting Stdout** shows on terminal, run visualsim model by following below steps
- 6) Run the visualsim model
- 7) Now debug the code using gdb commands such as (n, p, f, bt, step, b main, c)
- 8) After debugging type **continue** or **c** on the terminal, for rest of iteration to finished up
- 9) Plots will be displayed.

10) For more information refer:

command line



https://www.gem5.org/documentation/general/docs/debugging_and_testing/debugging/debugger_based_debugging

```

elc1@ubuntu:~/gem5-RISCV/gem5$ gdb --args build/RISCV/gem5.opt
GNU gdb (Ubuntu 8.1-0ubuntu3.2) 8.1.0.20180409-git
Copyright (C) 2018 Free Software Foundation, Inc.
License GPLv3+: GNU GPL version 3 or later <http://gnu.org/licenses/gpl.html>
This is free software: you are free to change and redistribute it.
There is NO WARRANTY, to the extent permitted by law. Type "show copying"
and "show warranty" for details.
This GDB was configured as "x86_64-linux-gnu".
Type "show configuration" for configuration details.
For bug reporting instructions, please see:
<http://www.gnu.org/software/gdb/bugs/>.
Find the GDB manual and other documentation resources online at:
<http://www.gnu.org/software/gdb/documentation/>.
For help, type "help".
Type "apropos word" to search for commands related to "word"...
Reading symbols from build/RISCV/gem5.opt...done.
(gdb) run --debug-break=1000 --debug-flags=DRAM --interactive
./configs/example/se_vs.py --cpu-type=TimingSimpleCPU --cpu-clock=1GHz --sys-
clock=1GHz --caches --l1i_size=16kB --l1d_size=16kB --mem-type=DDR3_1600_8x8
-c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt -outfile
../MiBench/consumer/jpeg/output_large_encode.jpeg
../MiBench/consumer/jpeg/input_large.ppm'

```

```

Starting program: /home/elc1/gem5-RISCV/gem5/build/RISCV/gem5.opt --debug-
break=1000 --debug-flags=DRAM --interactive ./configs/example/se_vs.py --cpu-
type=TimingSimpleCPU --cpu-clock=1GHz --sys-clock=1GHz --caches --
l1i_size=16kB --l1d_size=16kB --mem-type=DDR3_1600_8x8 -c
../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt -outfile
../MiBench/consumer/jpeg/output_large_encode.jpeg
../MiBench/consumer/jpeg/input_large.ppm'
[Thread debugging using libthread_db enabled]
Using host libthread_db library "/lib/x86_64-linux-gnu/libthread_db.so.1".
gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.
gem5 version 20.1.0.0
gem5 compiled Nov  2 2020 17:05:29
gem5 started Nov  6 2020 17:54:33
gem5 executing on ubuntu, pid 2177
command line: /home/elc1/gem5-RISCV/gem5/build/RISCV/gem5.opt --debug-break=1000 --
debug-flags=DRAM --interactive ./configs/example/se_vs.py --cpu-type=TimingSimpleCPU --cpu-
clock=1GHz --sys-clock=1GHz --caches --l1i_size=16kB --l1d_size=16kB --mem-
type=DDR3_1600_8x8 -c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt
-outfile ../MiBench/consumer/jpeg/output_large_encode.jpeg
../MiBench/consumer/jpeg/input_large.ppm'

```

comm

```

warn: need to stop all
warn: membus.slave i
warn: membus.slave i
warn: membus.slave i
warn: membus.slave i
warn: membus.slave i
warn: membus.maste
Global frequency set
warn: No dot file gene
0: system.mem ct
0: system.mem ct
0: system.mem ct
0: system.mem ct
warn: DRAM device ca
0: system.mem ct
0: system.remote
0: system.mem ct
Redirecting stdout
--- Now run the

```


command line – give gdb commands

<pre> Redirecting stdout iteration: 0 info: Entering event queue @ 0. Starting simulation... Program received signal SIGTRAP, Trace/breakpoint trap. 0x00007ffff5a4a237 in kill () at ../sysdeps/unix/syscall-template.S:78 78 ../sysdeps/unix/syscall-template.S: No such file or directory. (gdb) n kill () at ../sysdeps/unix/syscall-template.S:79 79 in ../sysdeps/unix/syscall-template.S (gdb) b main Breakpoint 1 at 0x55555564c9d0: main. (4 locations) (gdb) bt #0 kill () at ../sysdeps/unix/syscall-template.S:79 #1 0x0000555556c165a2 in GlobalEvent::BarrierEvent::process (this=0x5555589a3f00) at build/RISCV/sim/global_event.cc:131 #2 0x0000555556c0e77d in EventQueue::serviceOne (this=this@entry=0x555558981f20) at build/RISCV/sim/eventq.cc:222 #3 0x0000555556c33277 in doSimLoop (eventq=0x555558981f20) at build/RISCV/sim/simulate.cc:216 #4 0x0000555556c342ca in simulate (num_cycles=<optimized out>) at build/RISCV/sim/simulate.cc:129 #5 0x00005555569db2e1 in pybind11::detail::argument_loader<unsigned long>::call_impl<GlobalSimLoopExitEvent*, GlobalSimLoopExitEvent* (*)& (unsigned long), 0ul, pybind11::detail::void_type> (f=<optimized out>, this=<optimized out>) at ext/pybind11/include/pybind11/cast.h:1935 #6 pybind11::detail::argument_loader<unsigned long>::call<GlobalSimLoopExitEvent*, pybind11::detail::void_type, (gdb) n GlobalEvent::BarrierEvent::process (this=0x5555589a3f00) at build/RISCV/sim/global_event.cc:136 </pre>	<pre> GlobalSimLoopExitEvent* (*)& (unsigned long)>(GlobalSimLoopExitEvent* (*)& (unsigned long)) && (f=<optimized out>, this=<optimized out>) at ext/pybind11/include/pybind11/cast.h:1912 #7 void pybind11::cpp_function::initialize<GlobalSimLoopExitEvent* (*)& (unsigned long), GlobalSimLoopExitEvent*, unsigned long, 136 globalBarrier(); (gdb) n 137 } (gdb) n EventQueue::serviceOne (this=this@entry=0x555558981f20) at build/RISCV/sim/eventq.cc:223 223 if (event->isExitEvent()) { (gdb) n 232 event->release(); (gdb) n 234 return NULL; (gdb) n 232 event->release(); (gdb) n 199 std::lock_guard<EventQueue> lock(*this); (gdb) n 235 } </pre>	<pre> (gdb) c Continuing. info: Increasing stack size by one page. iteration 0 finished iteration: 1 info: Entering event queue @ 5000000000. Starting simulation... iteration 1 finished iteration: 2 info: Entering event queue @ 10000000000. Starting simulation... iteration 2 finished iteration: 3 info: Entering event queue @ 15000000000. Starting simulation... iteration 3 finished iteration: 4 info: Entering event queue @ 20000000000. Starting simulation... iteration 4 finished iteration: 5 info: Entering event queue @ 25000000000. Starting simulation... iteration 5 finished iteration: 6 info: Entering event queue @ 30000000000. Starting simulation... iteration 6 finished iteration: 7 info: Entering event queue @ 35000000000. Starting simulation... iteration 7 finished iteration: 8 info: Entering event queue @ 40000000000. Starting simulation... iteration 8 finished iteration: 9 info: Entering event queue @ 45000000000. Starting simulation... iteration 9 finished iteration: 10 info: Entering event queue @ 50000000000. Starting simulation... iteration 10 finished </pre>
---	---	---

← (gdb) c
Continuing.
To continue the
execution
↓ Show plots

50.4 Run with debugger - graphical gdb:

- 1) cd to gem directory \$ **`gdb -tui --args ./build/RISCV/gem5.opt`**
- 2) wait for gdb to open up , use run command (step 3) after gdb shows
- 3) (gdb) **`run --debug-break=1000 --debug-flags=DRAM --interactive ./configs/example/se_vs.py --cpu-type=TimingSimpleCPU --cpu-clock=1GHz --sys-clock=1GHz --caches --l1i_size=16kB --l1d_size=16kB --mem-type=DDR3_1600_8x8 -c ../MiBench/consumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt -outfile ../MiBench/consumer/jpeg/output_large_encode.jpeg ../MiBench/consumer/jpeg/input_large.ppm'`**
- 4) After **Redirecting Stdout** shows on terminal, run visualsim model by following below steps
- 5) Run the visualsim model
- 6) Now debug the code using gdb commands such as (n, p, f, bt, step, b main, c)
- 7) After debugging type **continue** or **c** on the terminal, for rest of iteration to finished up
- 8) Plots will be displayed.
- 9) For more information refer: <http://beej.us/guide/bggdb/#qref>

10) **NOTE:** All the normal **gdb** commands will work in GUI mode, and additionally the arrow keys and pgup/pgdown keys will scroll the source window (when it has focus, which it does by default).

Graphical gdb

```
elc1@ubuntu:~/gem5/gem5-ptolemy-master/gem5-stable_2015_09_03$ gdb -tui --args ./build/RISCV/gem5.opt
```



```

./build/RISCV/stn/main.cc
40 {
41     int ret;
42
43     // Initialize n5 special signal handling.
44     initSignals();
45
46     #if PY_MAJOR_VERSION >= 3
47     std::unique_ptr<wchar_t[], decltype(&PyMem_RawFree)> program(
48         Py_DecodeLocale(argv[0], NULL),
49         &PyMem_RawFree);
50     Py_SetProgramName(program.get());
51     #else
52     Py_SetProgramName(argv[0]);
53     #endif
54
55     // Register native modules with Python's init system before
56     // initializing the interpreter.
57     registerNativeModules();
58
exec: No process in:
This GDB was configured as "x86_64-linux-gnu".
Type "show configuration" for configuration details.
For bug reporting instructions, please see:
<http://www.gnu.org/software/gdb/bugs/>.
---Type <return> to continue, or q <return> to quit---
Find the GDB manual and other documentation resources online at:
<http://www.gnu.org/software/gdb/documentation/>.
For help, type "help".
Type "apropos word" to search for commands related to "word"...
Reading symbols from ./build/RISCV/gem5.opt...done.
(gdb)

```

```

gem5 version 20.1.0.0
gem5 compiled Nov  2 2020 17:05:29
gem5 started Nov  6 2020 18:34:33
gem5 executing on ubuntu, pid 2457
command line: /home/elc1/gem5-RISCV/gem5/build/RISCV/gem5.opt --debug-break=1000 --debug-flags=DRAM --interactive ./configs/example/se_vs.py -
-cpu-type=TimingSimpleCPU --cpu-clock=1GHz --sys-clock=1GHz --caches --l1i_size=16kB --l1d_size=16kB --mem-type=DDR3_1600_8x8 -c ./MiBench/co
nsumer/jpeg/jpeg-6a/cjpeg -o '-dct int -progressive -opt -outfile ./MiBench/consumer/jpeg/output_large_encode.jpeg ./MiBench/consumer/jpeg/i
nput_large.ppm'

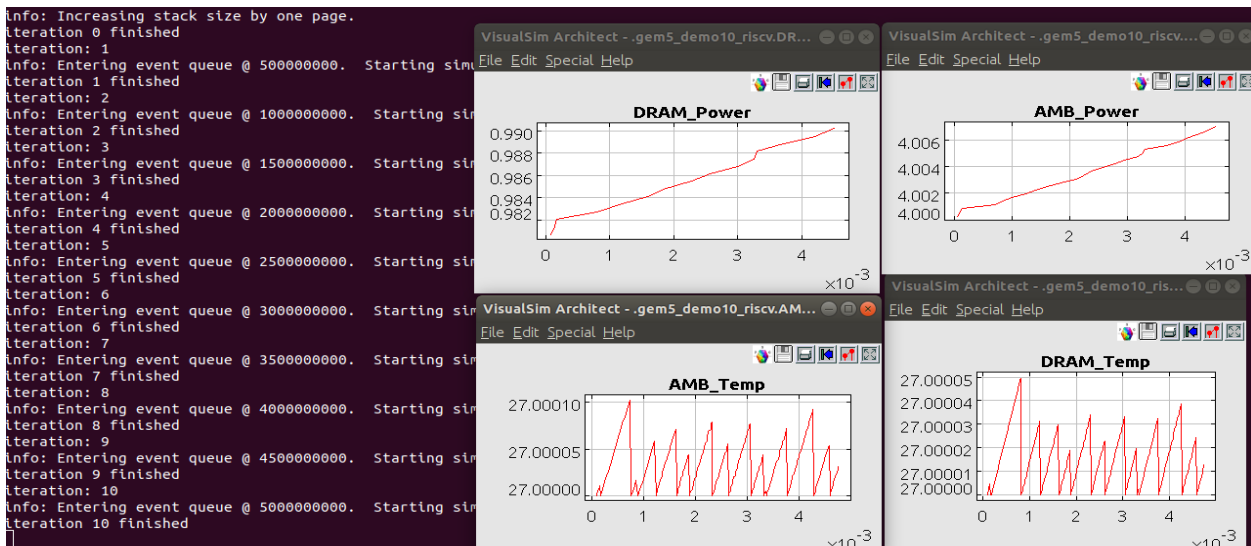
warn: need to stop all queues
warn: membus.slave is deprecated. 'slave' is now called 'cpu_side_ports'
warn: membus.slave is deprecated. 'slave' is now called 'cpu_side_ports'
warn: membus.slave is deprecated. 'slave' is now called 'cpu_side_ports'
warn: membus.slave is deprecated. 'slave' is now called 'cpu_side_ports'
warn: membus.slave is deprecated. 'slave' is now called 'cpu_side_ports'
warn: membus.master is deprecated. 'master' is now called 'mem_side_ports'
Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
0: system.mem_ctrls.dram: Setting up DRAM Interface
0: system.mem_ctrls.dram: Creating DRAM rank 0
0: system.mem_ctrls.dram: Creating DRAM rank 1
0: system.mem_ctrls.dram: Memory capacity 536870912 (536870912) bytes
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.mem_ctrls.dram: Row buffer size 8192 bytes with 128 bursts per row buffer
0: system.remote_gdb: listening for remote gdb on port 7002
0: system.mem_ctrls.port: Pushing DRAM ranges to port
Redirecting stdout

```

```

gem5 build/RISCV/sim/eventq.cc
215
216     // handle action
217     if (!event->squashed()) {
218         // forward current cycle to the time when this event occurs.
219         setCurTick(event->when());
220         if (DTRACE(Event))
221             event->trace("executed");
222         event->process();
223     }
224     if (event->isExitEvent()) {
225         assert(!event->flags.isSet(Event::Managed) ||
226             !event->flags.isSet(Event::IsMainQueue)); // would be silly
227         return event;
228     } else {
229         event->flags.clear(Event::Squashed);
230     }
231     event->release();
232
233
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
0: system.mem_ctrls.dram: SetEventQueue::serviceOne
(gdb) ../sysdeps/unix/syscall-template.S:1: No such file or directory.
(gdb) n
kill () at ../sysdeps/unix/syscall-template.S:79
(gdb) n
GlobalEvent::BarrierEvent::process (this=0x5555589a3f00) at build/RISCV/sim/global_event.cc:136
(gdb) n
(gdb) n
EventQueue::serviceOne (this=this@entry=0x555558981f20) at build/RISCV/sim/eventq.cc:223
(gdb) p event
$1 = (Event *) 0x5555589a3f00
(gdb)

```



50.5 Running the Gem5 in System Call Emulation (SE) Mode

The SE mode simulation focuses on the CPU and memory system, and does not emulate the entire system. In this mode, one only needs to specify the binary file to be simulated. This binary file can be statically/dynamically linked. `configs/examples/se.py` is used for configuring and running simulations in this mode. What follows is probably the simplest example of how to use `se.py`. The binary file to simulated is specified with option `-c`.

- 1) cd to the gem5 location on terminal and use the below command to run the hello arm executable.

```
$ elc1@ubuntu:~/gem5-RISCV/gem5$ ./build/RISCV/gem5.opt
./configs/example/se.py -c ./tests/test-progs/hello/bin/riscv/linux/hello
```

- 2) For statistics refer → /gem5/m5out /stats.txt

50.6 Running the Gem5 (SE mode) in Multi-core

- 1) cd to the gem5 location on terminal and use the below command to run the hello arm executable.

```
$ elc1@ubuntu:~/gem5-RISCV/gem5$ ./build/RISCV/gem5.opt configs/example/se.py
--num-cpus=2 -c './tests/test-progs/hello/bin/riscv/linux/hello;./tests/test-
progs/hello/bin/riscv/linux/hello'
```

```
elc1@ubuntu:~/gem5-RISCV/gem5$ ./build/RISCV/gem5.opt configs/example/se.py --num-cpus=2 -c
 './tests/test-progs/hello/bin/riscv/linux/hello;./tests/test-progs/hello/bin/riscv/linux/hello'
gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.
```

```
gem5 version 20.1.0.0
gem5 compiled Nov  2 2020 17:05:29
gem5 started Nov  6 2020 18:52:21
gem5 executing on ubuntu, pid 2526
command line: ./build/RISCV/gem5.opt configs/example/se.py --num-cpus=2 -c './tests/test-progs/hello/bin/riscv/linux/hello;./tests/test-
progs/hello/bin/riscv/linux/hello'
```

```
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.master is deprecated. `master` is now called `mem_side_ports`
Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7003
0: system.remote_gdb: listening for remote gdb on port 7004
**** REAL SIMULATION ****
info: Entering event queue @ 0. Starting simulation...
info: Increasing stack size by one page.
info: Increasing stack size by one page.
Hello world!
Hello world!
Exiting @ tick 3339000 because exiting with last active thread context
```

When number of cores = 4

```
./build/RISCV/gem5.opt configs/example/se.py --num-cpus=4 -c './tests/test-progs/hello/bin/riscv/linux/hello;./tests/test-progs/hello/bin/riscv/linux/hello;./tests/test-progs/hello/bin/riscv/linux/hello;./tests/test-progs/hello/bin/riscv/linux/hello'
```

2) For statistics refer -> `/gem5/m5out /stats.txt`

50.7 Running the Gem5 in Full System (FS) Mode

As currently gem5 supports the RISC-V ISA only in SE mode,

51 SysML to VisualSim

Cameo Systems Modeler is an industry-leading cross-platform collaborative Model-Based Systems Engineering (MBSE) environment, which provides smart, robust, and intuitive tools to define, track, and visualize all aspects of systems in the most standard-compliant SysML models and diagrams.

One can create an activity diagram in the Cameo System Modeler, which contains a sequence of tasks that needs to be executed on a hardware platform. By importing this diagram to VisualSim environment we map it with the hardware platform & we can perform the Hardware- Software simulation.

Cameo System Modeler generates an XML file similar to VisualSim XML files but the format differs in both of them.

So, to import is successfully a SysML to VisualSim converter named "**Xml_Convertor**" is used. It analyses the generated XML file (Cameo System Modeler) & generates an XML file in the format supported by VisualSim.

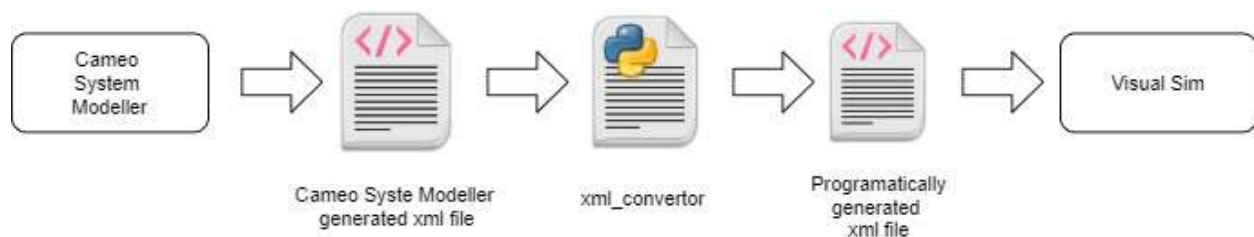


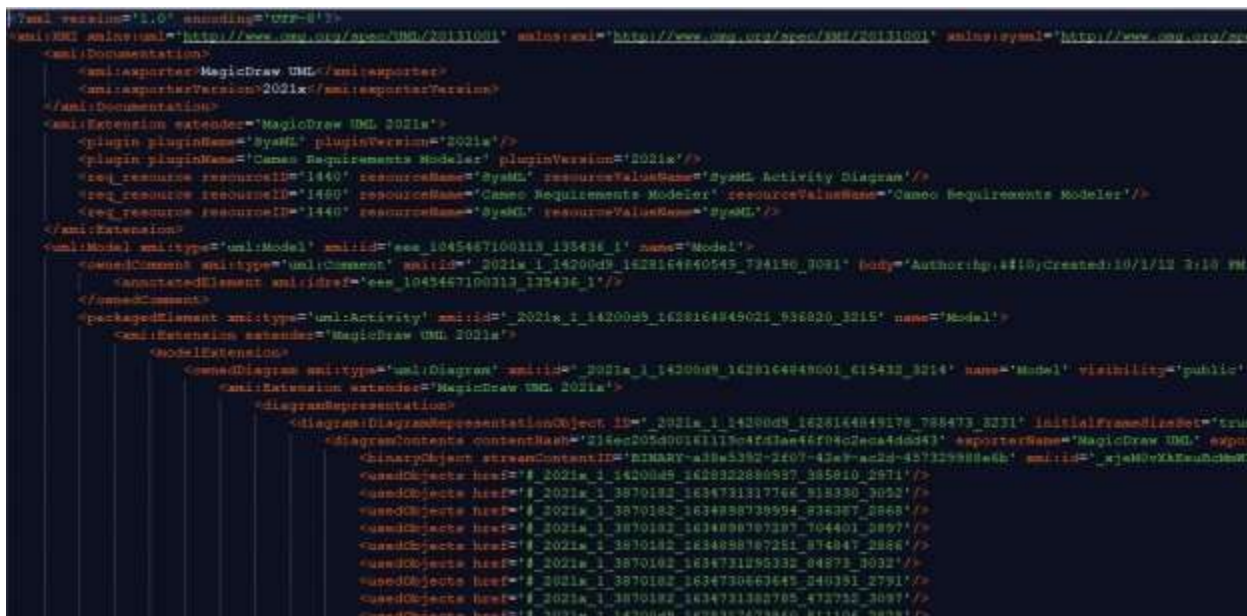
Fig1: SysML to VisualSim

51.1 Pre-Requisite:

- 1) Python 3 or higher
- 2) Input file (i.e. Cameo generated XML file)

51.2 Features supported by XML Converter:

- 1) Conversion of Activity Diagram.
- 2) Conversion of Requirement Diagram.
- 3) Conversion of Package Diagram.
- 4) Conversion of Single block & Multiple block hierarchical diagram.



```

<?xml version='1.0' encoding='UTF-8'?>
<xml:lang xmlns:xml='http://www.w3.org/XML/20131001' xmlns:uml='http://www.omg.org/spec/UML/20131001' xmlns:xsi='http://www.w3.org/2001/XMLSchema-instance' xsi:schemaLocation='http://www.omg.org/spec/UML/20131001 http://www.omg.org/spec/UML/20131001/UML.xsd' />
<uml:Documentation>
  <uml:exporter MagicDraw UML /uml:exporter>
  <uml:exporterVersion 2021x /uml:exporterVersion>
</uml:Documentation>
<uml:Extension extender='MagicDraw UML 2021x'>
  <plugin pluginName='SysML' pluginVersion='2021x' />
  <plugin pluginName='Cameo Requirements Modeler' pluginVersion='2021x' />
  <req_resource resourceID='1440' resourceName='SysML' resourceValueName='SysML Activity Diagram' />
  <req_resource resourceID='1460' resourceName='Cameo Requirements Modeler' resourceValueName='Cameo Requirements Modeler' />
</uml:Extension>
<uml:Model smt:type='uml:Model' smt:id='see_1045467100113_135436_1' name='Model'>
  <uml:comment smt:type='uml:Comment' smt:id='2021x_1_14200d9_1628164840545_734156_3081' body='Author:hp.4410;Created:10/1/12 2:10 PM' />
  <annotatedElement smt:idref='see_1045467100113_135436_1' />
</uml:comment>
<packagedElement smt:type='uml:Activity' smt:id='2021x_1_14200d9_1628164840545_536820_3215' name='Model'>
  <uml:Extension extender='MagicDraw UML 2021x'>
    <ModelExtension>
      <uml:Diagram smt:type='uml:Diagram' smt:id='2021x_1_14200d9_1628164840545_615432_3216' name='Model' visibility='public'>
        <uml:Extension extender='MagicDraw UML 2021x'>
          <DiagramRepresentation>
            <diagramDiagramRepresentationObject ID='2021x_1_14200d9_1628164840545_738473_3231' initialFrameSizeSet='true'>
              <diagramContents contentHash='715ec205d0016117e4f43ae46f94c2eca4d0443' exporterName='MagicDraw UML' exportDate='2012-10-01 14:00:00' />
              <BinaryObject serverContentID='BINARY-a38e3382-2f07-42a7-ac2d-45731988e8d' smt:id='s_jwM0vXAEu0cbm0' />
              <usedObjects href='#2021x_1_14200d9_1628164840545_385810_2971' />
              <usedObjects href='#2021x_1_14200d9_1628164840545_385810_2971' />
              <usedObjects href='#2021x_1_14200d9_1628164840545_385810_2971' />
              <usedObjects href='#2021x_1_14200d9_1628164840545_385810_2971' />
              <usedObjects href='#2021x_1_14200d9_1628164840545_385810_2971' />
              <usedObjects href='#2021x_1_14200d9_1628164840545_385810_2971' />
              <usedObjects href='#2021x_1_14200d9_1628164840545_385810_2971' />
              <usedObjects href='#2021x_1_14200d9_1628164840545_385810_2971' />
            </diagramDiagramRepresentationObject>
          </uml:Extension>
        </ModelExtension>
      </packagedElement>
    </uml:Extension>
  </packagedElement>
</uml:Model>

```

Fig2. Format of XML file in Cameo System Modeler.


```

<?xml version="1.0" standalone="no"?>
<!DOCTYPE entity PUBLIC "-//Mirabilis Design//DTD MoMG 1//EN"
"http://www.mirabilisdesign.com/xml/dtd/MoMG_1.dtd">
<entity name="Vb_hierarchical" class="VisualSim.actor.TypedCompositeActor">
<property name="DigitalSimulator" class="VisualSim.simulators.de.kernel.BEDirector">
<property name="digitalDebugger" class="VisualSim.kernel.util.StringAttribute" value="Off">
<property name="style" class="VisualSim.actor.gui.style.ChoiceStyle">
<property name="Off" class="VisualSim.kernel.util.StringAttribute" value="Off"/>
<property name="Pause" class="VisualSim.kernel.util.StringAttribute" value="Pause"/>
<property name="Run" class="VisualSim.kernel.util.StringAttribute" value="Run"/>
<property name="Summary_Only" class="VisualSim.kernel.util.StringAttribute" value="Summary_Only"/>
</property>
</property>
<property name="stopTime" class="VisualSim.data.expr.Parameter" value="10"/>
<property name="timeResolution" class="VisualSim.mcmi.SharedParameter" value="1E-12">
<property name="style" class="VisualSim.actor.gui.style.NotEditableLineStyle"/>
</property>
<property name="_location" class="VisualSim.kernel.util.Location" value="[1129.0, 25.0]"/>
</property>
<property name="_location" class="VisualSim.kernel.util.Location" value="[108.0,250.0]"/>
<entity name="initial code" class="VisualSim.actor.lib.DB_Source" >
<property name="_location" class="VisualSim.kernel.util.Location" value="[220.0,250.0]"/>
</entity>
<entity name="transfer[]" class="dams.Software_Devel.software_methodology.transfer" >
<property name="_location" class="VisualSim.kernel.util.Location" value="[340.0,250.0]"/>
<property name="Time" class="VisualSim.data.expr.Parameter" value="[14,14,14]"/>
</property>
<property name="Exec" class="VisualSim.data.expr.Parameter" value="{&quot;Bus1&quot;,&quot;Bridge&quot;,&quot;Bus2&quot;}">
</property>
</entity>
<entity name="task2" class="dams.Software_Devel.software_methodology.process" >
<property name="_location" class="VisualSim.kernel.util.Location" value="[460.0,250.0]"/>
<property name="Device_Name" class="VisualSim.data.expr.Parameter" value="{&quot;CPU&quot;}">
</property>
<property name="Device_Time" class="VisualSim.data.expr.Parameter" value="220" >
</property>

```

Fig3. Format of XML file in VisualSim Architect.

51.3 Activity and Requirement Diagram

51.3.1 Steps to import Activity Diagram in VisualSim

Step 1: Open Cameo System Modeler then create the requirement & Activity diagram in it. As shown in Fig 4.1 & Fig 4.2. Then click on save project to save. Now the xml file will be created.

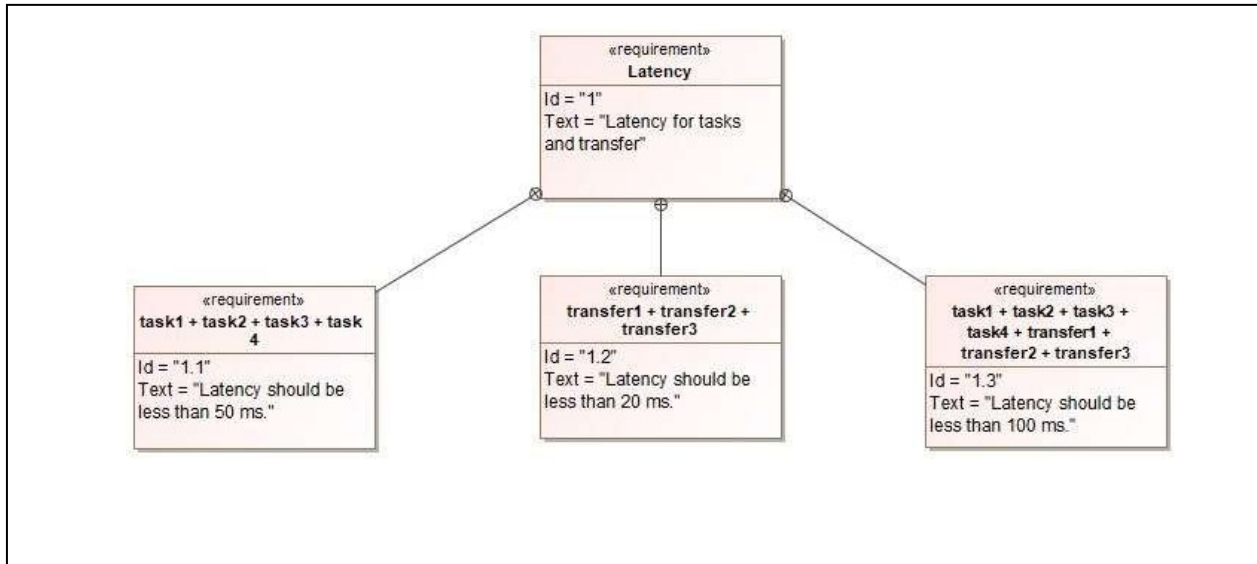


Fig 4.1: Requirement Diagram

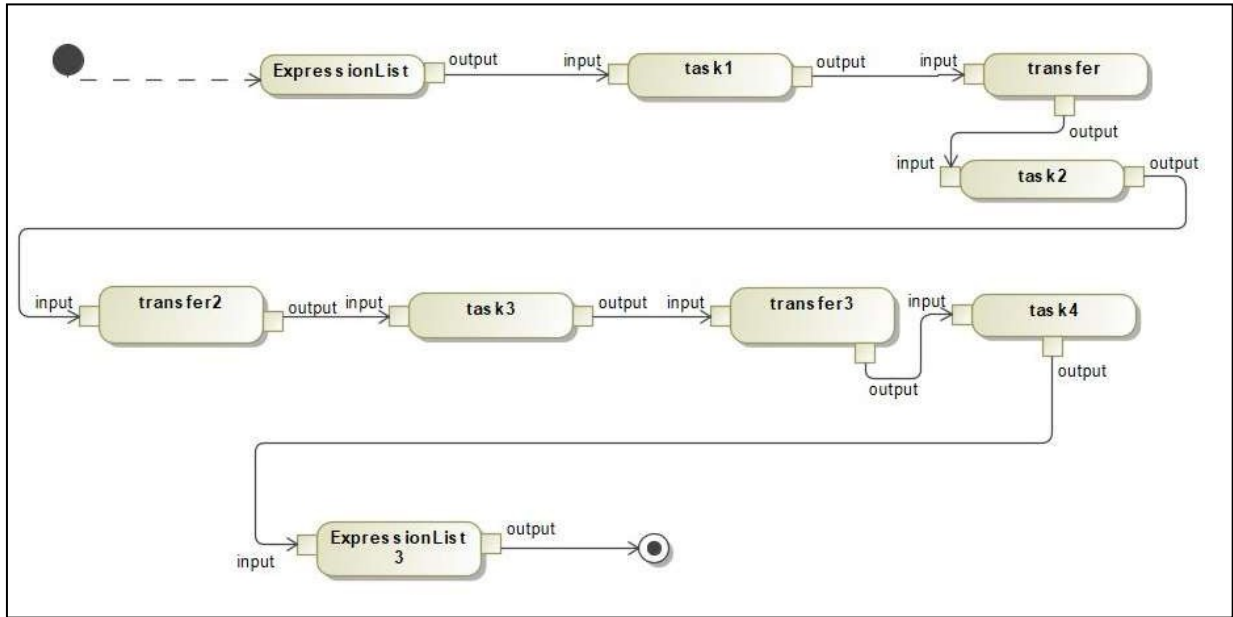


Fig 4.2: Activity Diagram

When you double click on any block in the diagram then a window appears. In the Document/Comment section, you need to specify the parameters. As shown in the Fig 5.

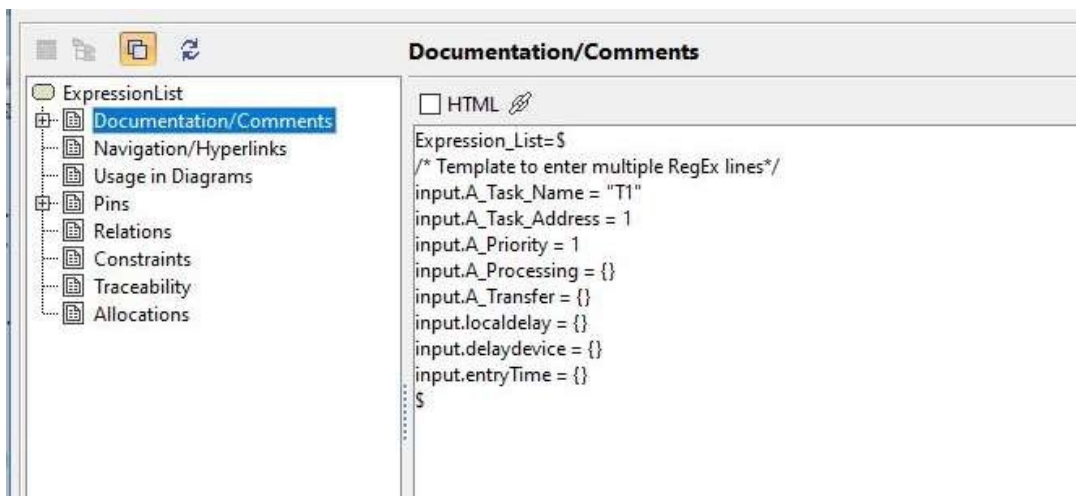


Fig 5: Parameters with multiline values

Expression_List is the name of the parameter & after “=” the value portion starts.

Note: If the value is multiline then you need to enclose the value part by symbol “\$”, as shown in Fig 5.

If there are multiple parameters then you can write each parameter in next line as shown in Fig 6.

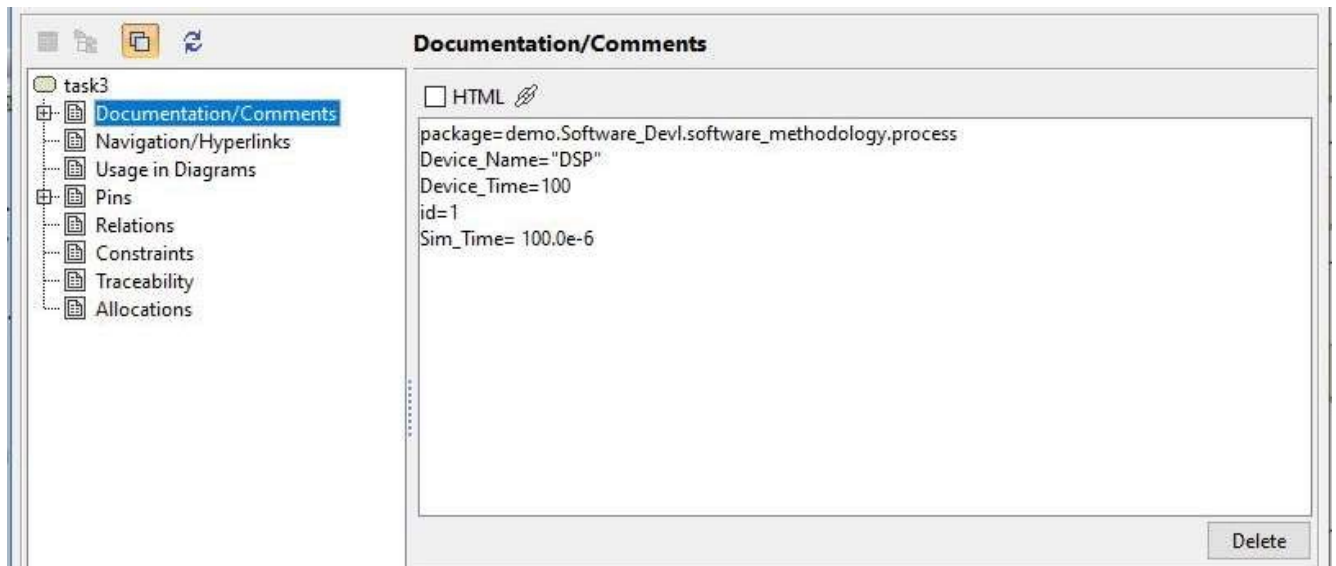


Fig 6: Multiple Parameters with single line values.

Step 2: Execute the python script “xml_convertor.py” & Enter the necessary details about the input and the output file. As shown in Fig7. If everything is correct then the XML file for visualSim will be generated.

```
E:\updated_sysml\final>py xml_convertor.py
Enter input file name:CM_Activity_Diagram_with_object_multiple.xml
Enter outupt file name:Activity_diagram_for_visualsim.xml
Activity_diagram_for_visualsim.xml generated successfully
```

Fig 7: Exection of xml_convertor.py

Here “CM_Activity_Diagram_with_object_multiple.xml” is the name of the input file, which is generated by Cameo System Modeler & “Activity_diagram_for_visualsim.xml” is the name of the output file, which will be generated by the tool.

NOTE : If there is requirement diagram, then one more file is generated programatically, i.e “data.csv” file. Contents of “data.csv” is shown in figure below.

	A	B	C	D	E	F	G
1	BLOCK	METRICS	CONSTRAINT	CONSTRAINT VALUE	STATISTIC TYPE	REFERENCE VARIABLE	
2	1.1	task1 + task2 + task3 + task 4	<		50 Max		
3	1.2	transfer1 + transfer2 + transfer3	<		20 Max		
4	1.3	task1 + task2 + task3 + task4 + transfer1 + transfer2 + transfer3	<		100 Max		
5							

Step 3: Open the VisualSim. As shown in Fig 8.

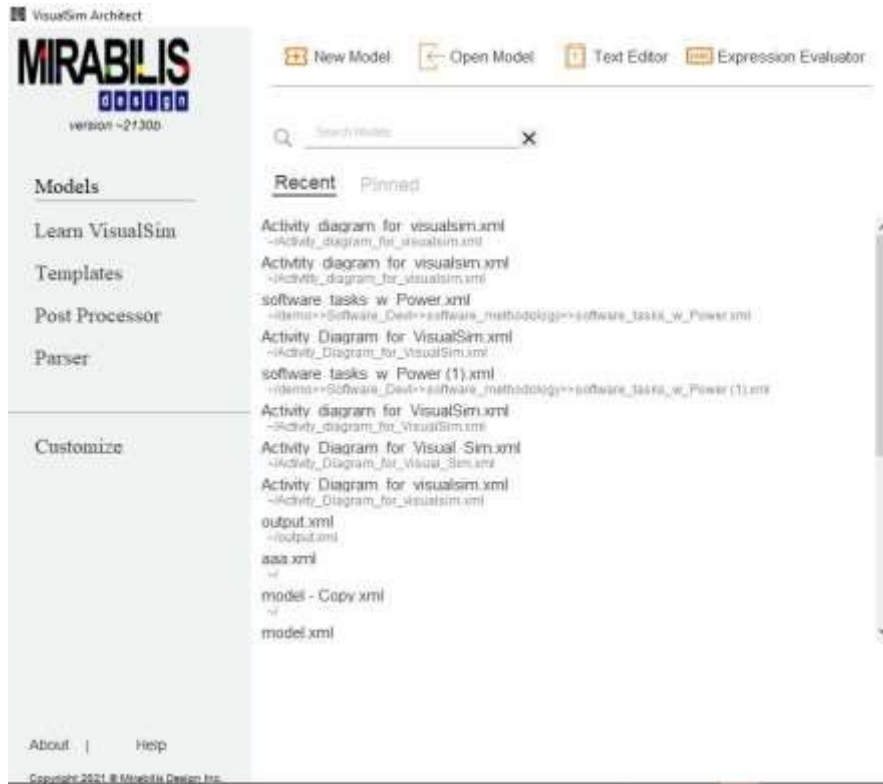


Fig 8: VisualSim

Step 4: Click on open button. Select the file which is generated programatically. As shown in Fig 9.

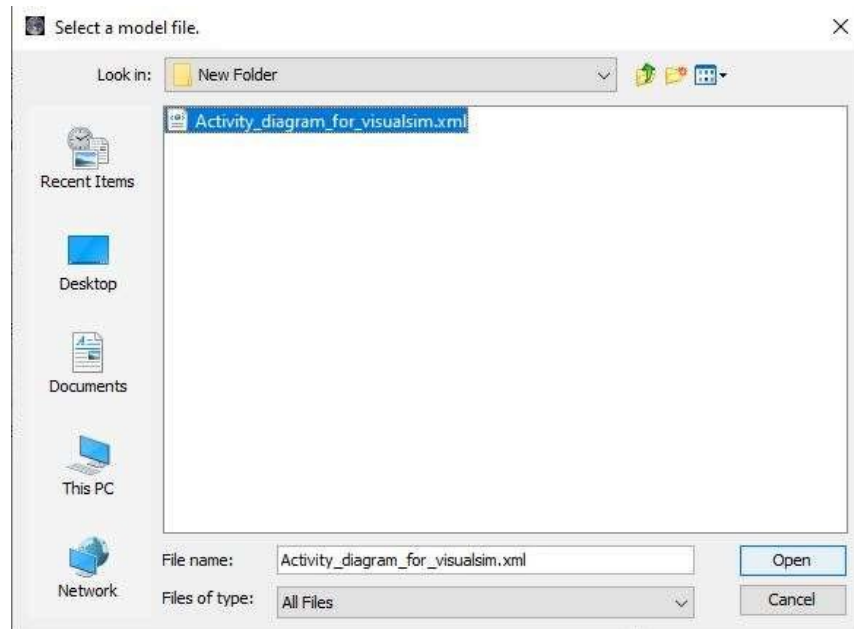
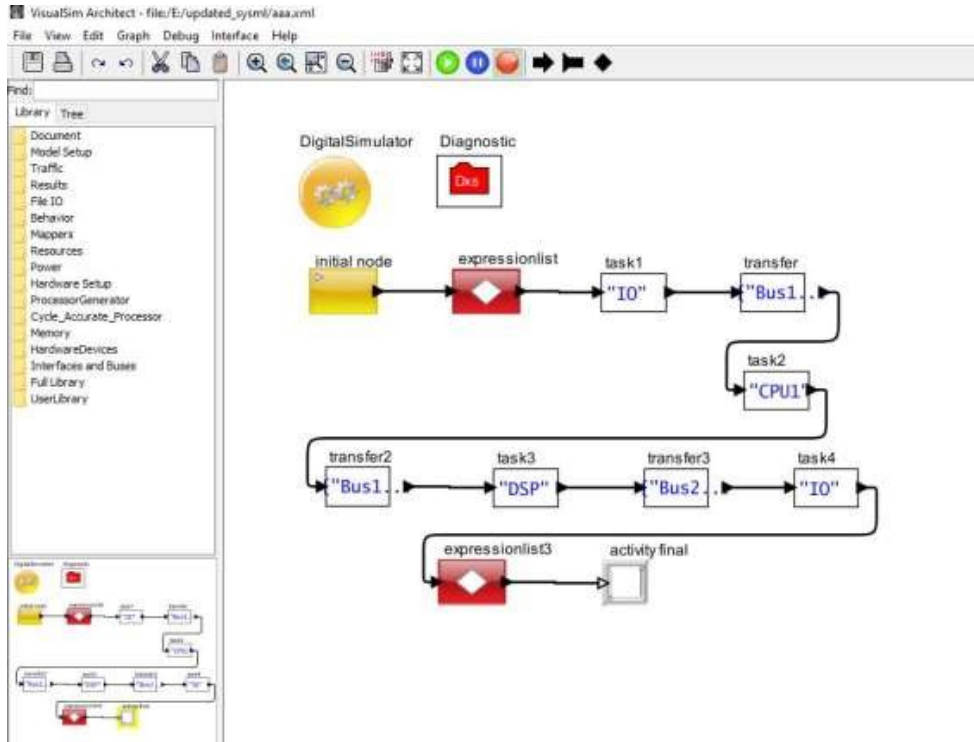


Fig 9: Browse the file

Step 5: Click on open button. Activity Diagram imported successfully to VisualSim.



When you click on any block in VisualSim then you can see the equivalent parameter we specified in Cameo System Modeler.

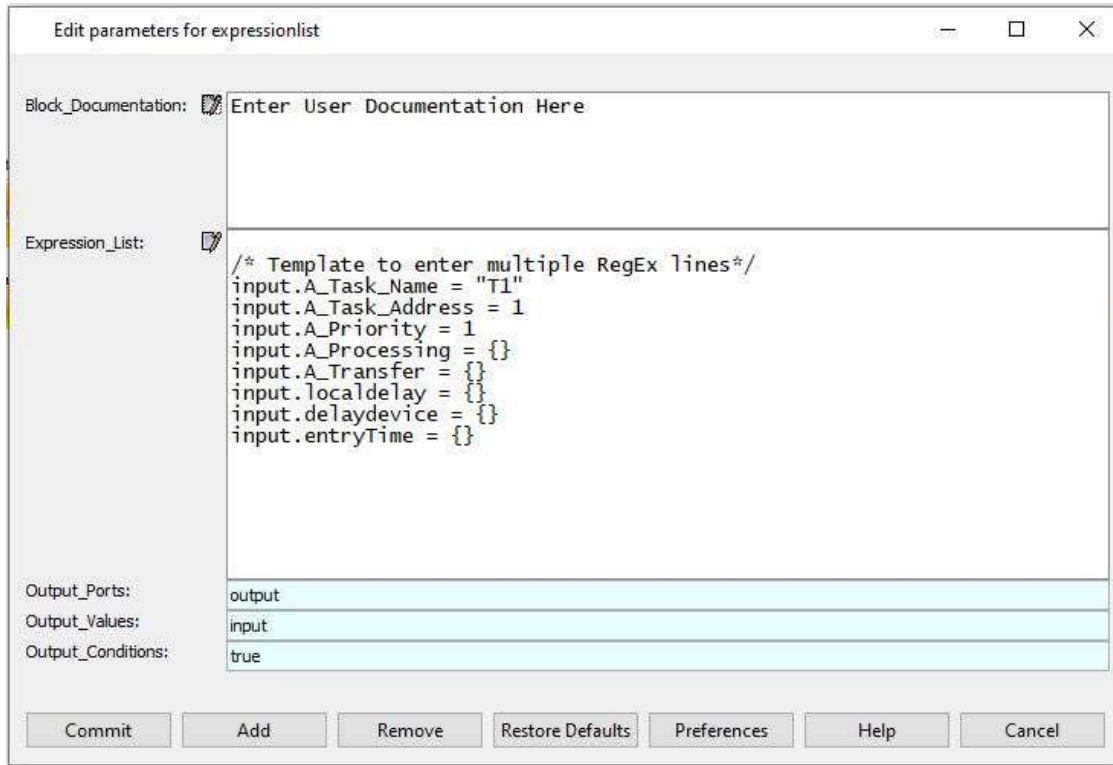


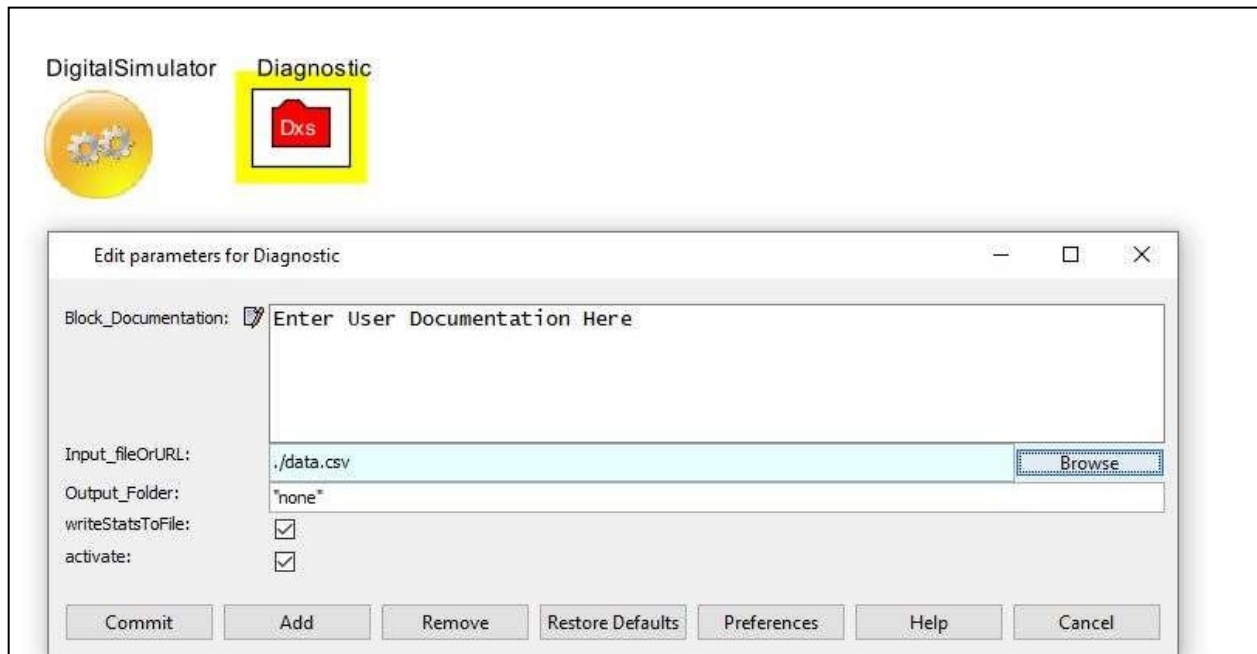
Fig 10(a): Parameters of Expression_list block

You can see in the Fig 10(a), the equivalent parameters for expression_list block listed here.



Similarly, for task3 block. As shown in Fig 10(b).

When you double click on diagnostic block, then you can see the location of csv file mentioned there.



Using this methodology, you can evaluate the performance of any SysML activity in VisualSim

51.4 Package Diagram

51.4.1 Steps to import Package Diagram in VisualSim

Step 1: Open Cameo System Modeler then create the package diagram in it. As shown in Fig 11.

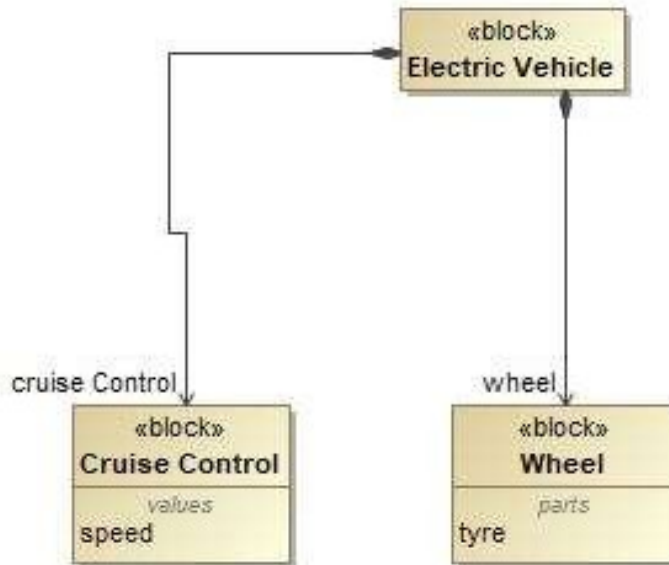


Fig 11: Package Diagram

Fig 11 shows the package diagram created in Cameo System Modeler. Speed is the attribute of Cruise Control block & type is the attribute of Wheel block.

Step 2: Execute the python script "xml_convertor.py" & Enter the necessary details about the input and the output file. If everything is correct then the XML file for visualSim will be generated. As shown in Fig 12.

```
E:\sysML_>py xml_convertor.py
Enter input file name:package_diagram_cameo.xml
Enter outupt file name:package_diagram_for_visualsim.xml
package_diagram_for_visualsim.xml generated successfully
```

Fig 12: Execution of xml_convertor.py for package diagram

Step 3: Open the VisualSim. As shown in Fig 13.

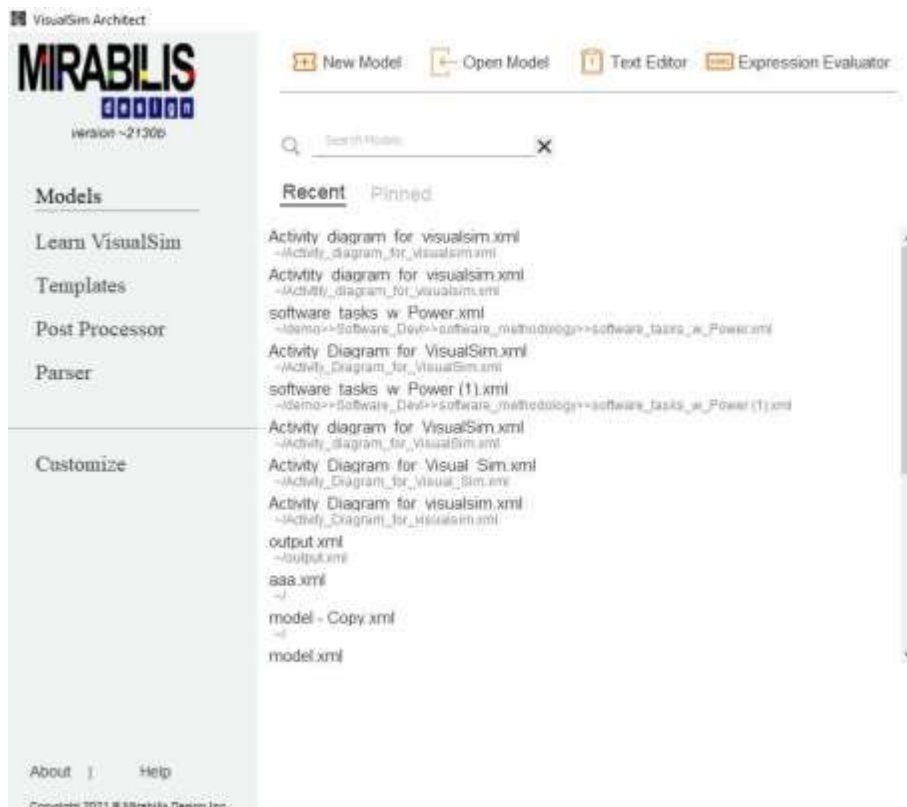


Fig 13: VisualSim

Step 4: Click on open button. Select the file which is generated programatically & open it.

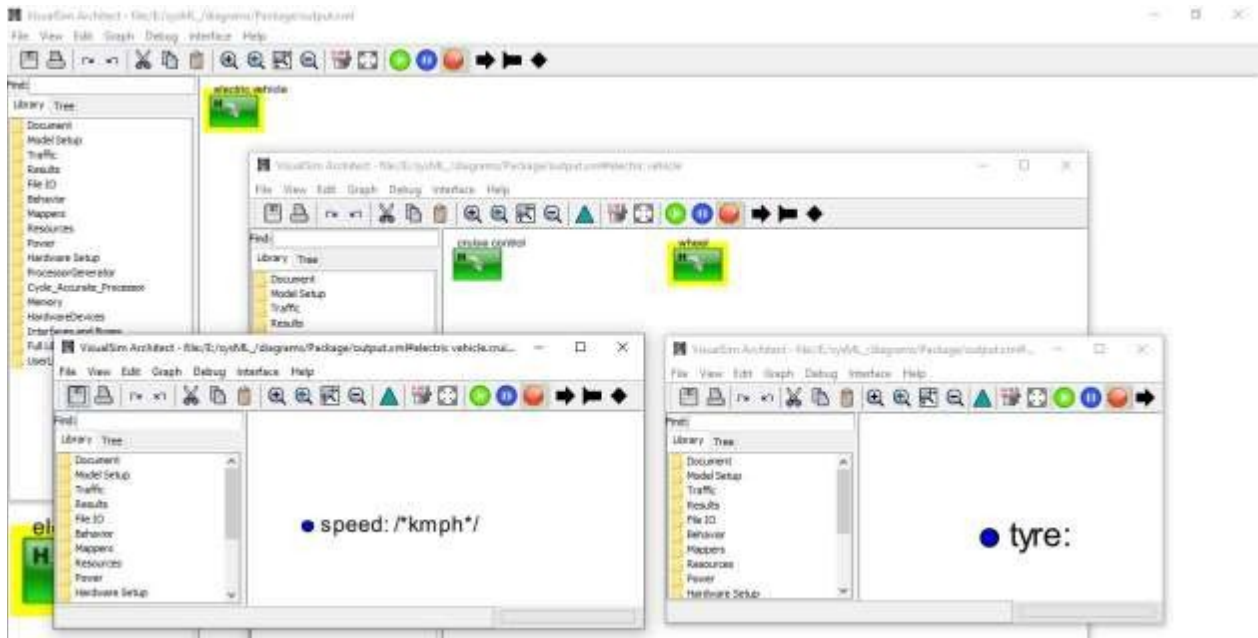


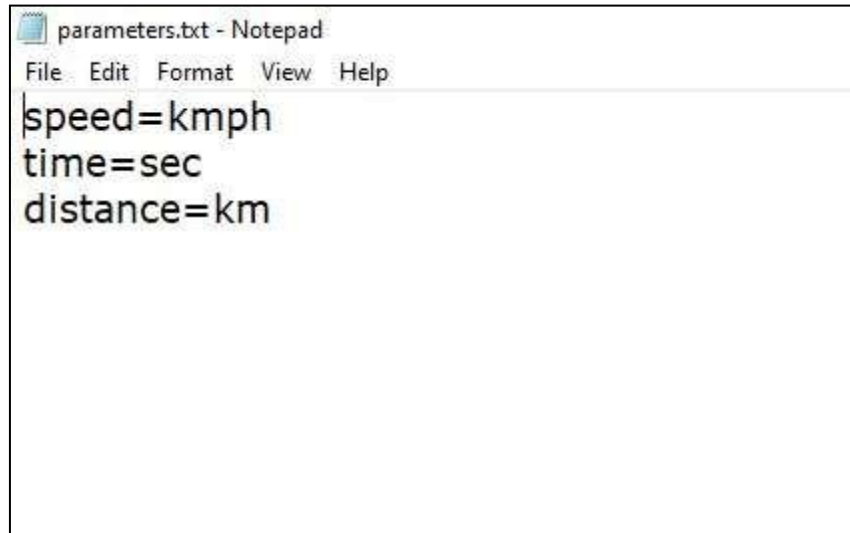
Fig 14: Package diagram in VisualSim

Note: If you see the diagram in the Cameo System Modeler, no value is specified for parameter speed. But in the VisualSim there is some default value present for parameter speed. Because the user has created the file named "parameter.txt" which contains the necessary information regarding the default value for the parameters.

The format of file "parameters.txt" should be like

```
parameter_first=default_value_for_parameter_first
parameter_second=default_value_for_parameter_second
parameter_third=default_value_for_parameter_third
```

as shown in Fig 15.

A screenshot of a Notepad window titled "parameters.txt - Notepad". The window has a menu bar with "File", "Edit", "Format", "View", and "Help". The text inside the window is:

```
speed=kmph  
time=sec  
distance=km
```

Fig 15: Format of the file parameters.txt

If the user does not create “parameters.txt” file, then no default values will be set against parameters.

51.5 Block Diagram

51.5.1 Steps to import Block Diagram in VisualSim

Step 1: Open Cameo System Modeler then create the block diagram in it. As shown in Fig 16.

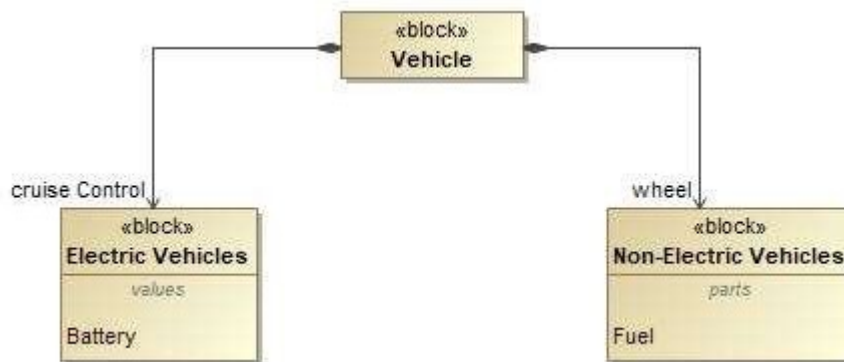


Fig 16: Package Diagram

Step 2: Execute the python script “xml_convertor.py” & Enter the necessary details about the input and the output file. If everything is correct then the XML file for visualSim will be generated. As shown in Fig 17.

```
E:\updated_sysml\block_diagram>py xml_convertor.py
Enter input file name:diagram.xml
Enter outupt file name:VS_diagram.xml
VS_diagram.xml generated successfully
```

Fig 17: Execution of xml_convertor.py for block diagram

Step 3: Open the VisualSim. As shown in Fig 18.

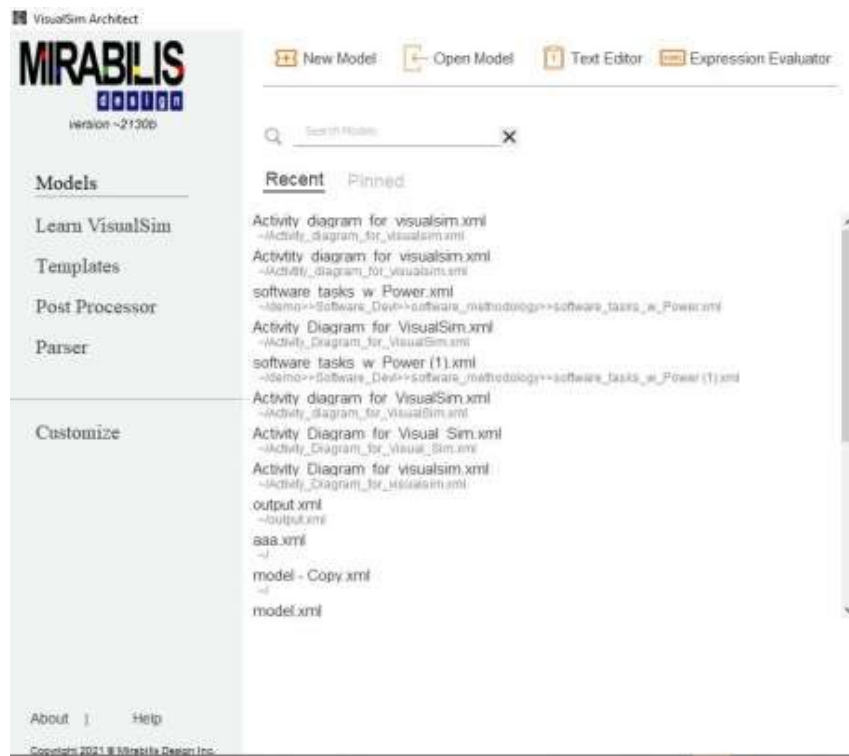


Fig 18: VisualSim

Step 4: Click on open button. Select the file which is generated programatically & open it.

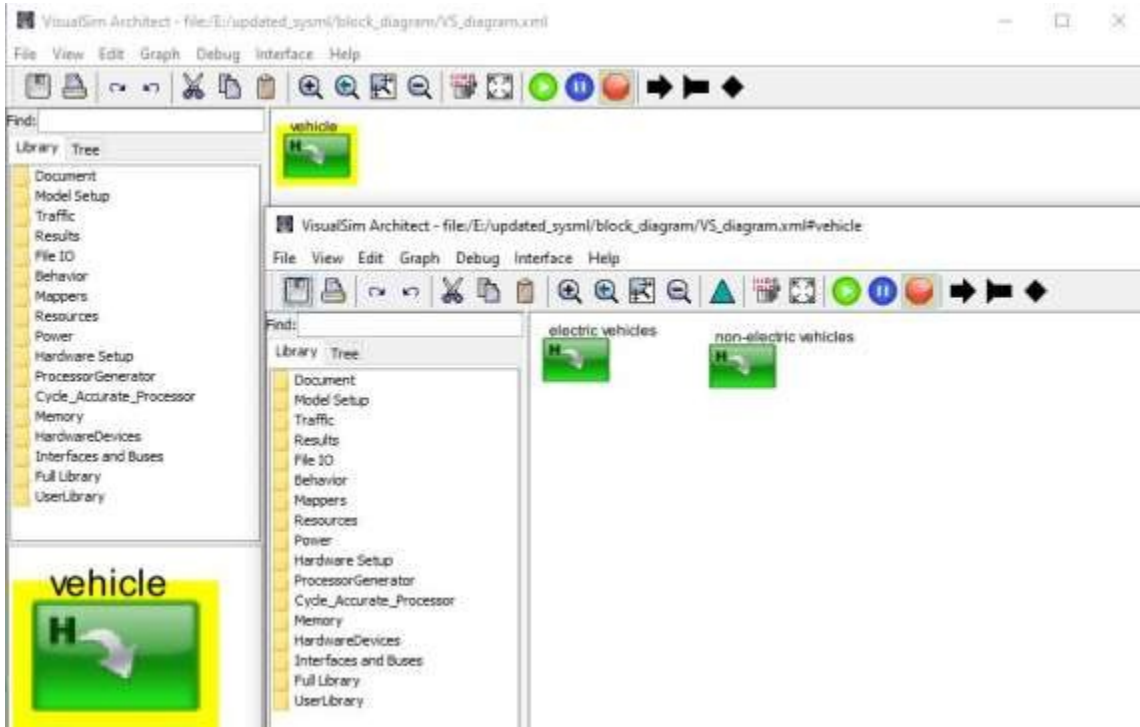


Fig 19: Package diagram in
