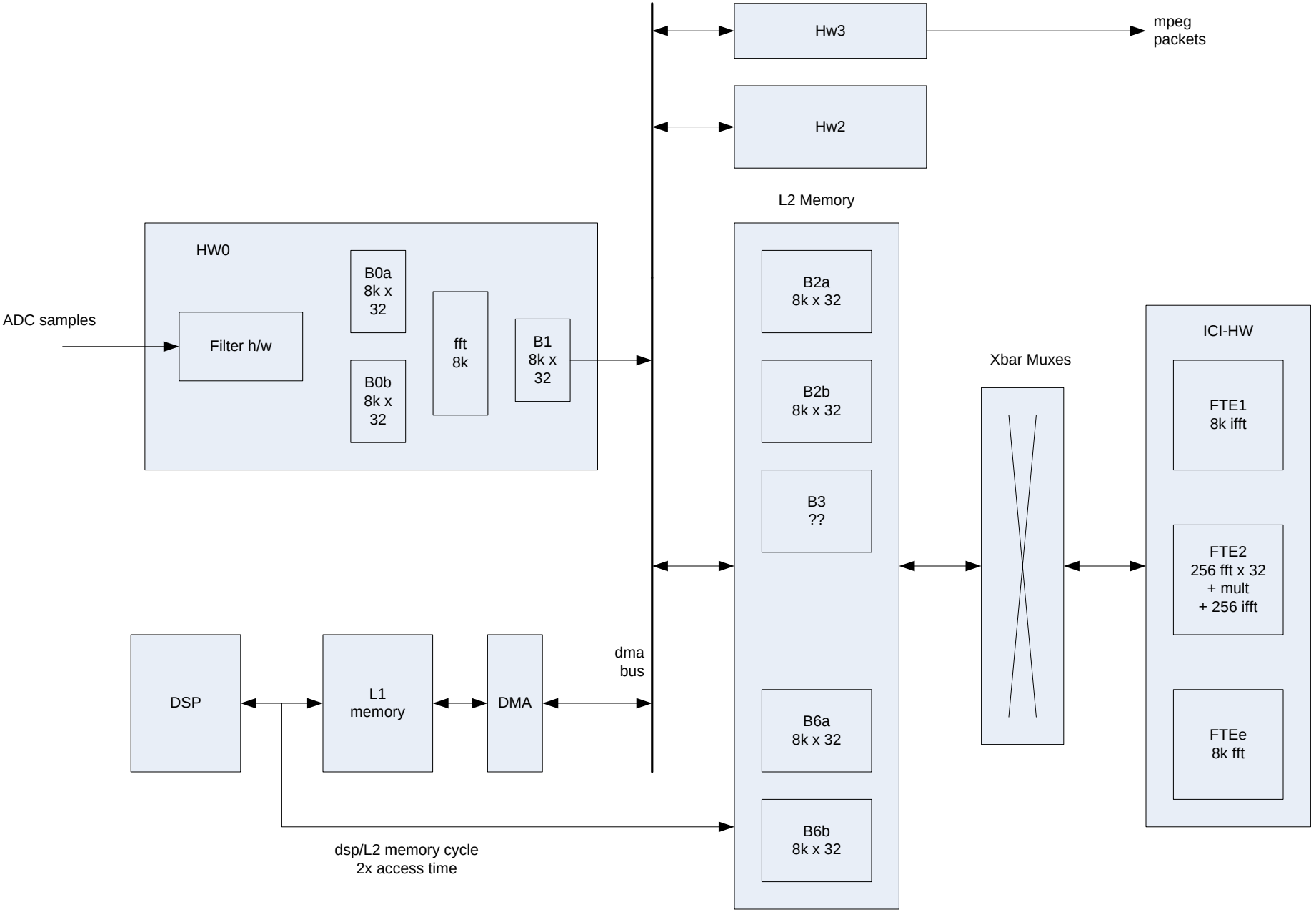
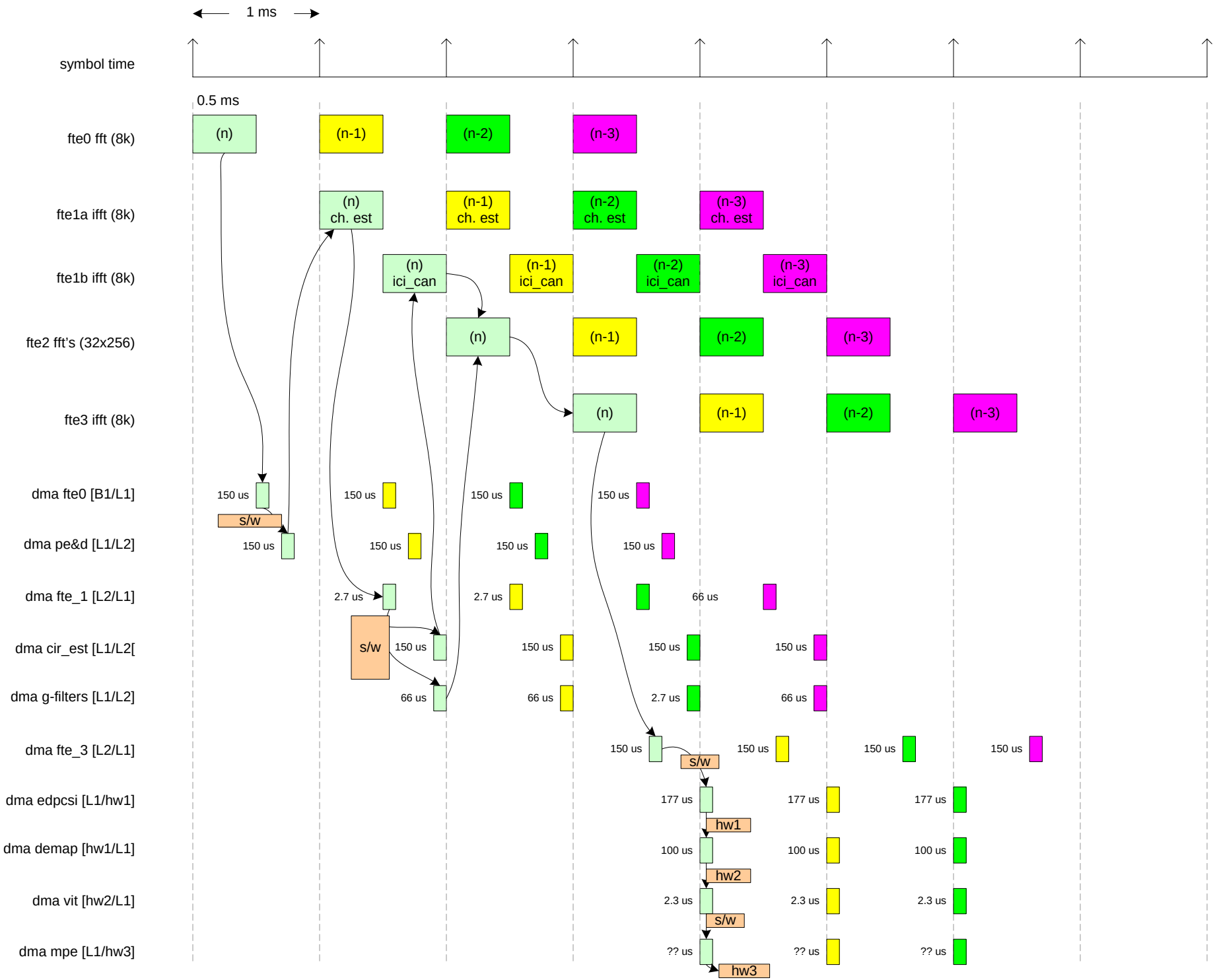
Preliminary DVBH Simple Top Level Architecture for Milibalis



Processing Timeline



DMA Analysis:

DMA_1 : fte0, 27 kB,	B1 → L1
DMA_2 : pe&d, 27 kB,	L1 → B2
DMA_3 : fte1, 0.5 kB	B2 → L1
DMA_4: cir_est, 27 kB,	L1 → B2
DMA_5: g-filters, 12 kB,	L1 → B3
DMA_6: fte3, 27 kB,	B6 → L1
DMA_7: 2nd edpcsi, 32 kB,	L1 → B7
DMA_8: demap, 18 kB,	hw1 → B8
DMA_9: vit & rs, 408 B,	hw2 → L1
DMA10: mpe, ?? B,	L1 → B10
---	---

Total: 172 kB/ symbol (symbol = 1 ms)

FRIO DMA Bandwidth = 180 mB/sec
DMA/symbol = 180 kB/symbol