Distributed System Exploration

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Design Analysis 2: Distributed System

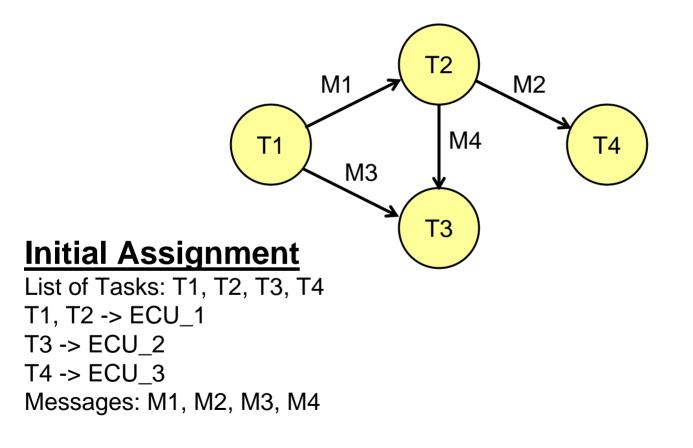
• System details

- Multi-independent processing computers
- Software tasks distributed across these computers
- Connectivity across multiple shared networks

Analysis

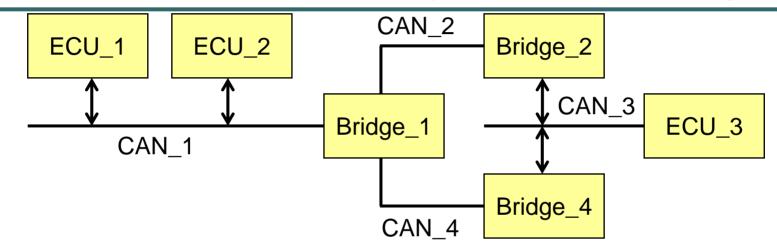
- Optimal Routing Table configuration
- Capacity planning
- Software tasks and thread distribution
- Resource allocation

MIRABILIS Example 2: Distributed System Logical Task Flow





Example 2: Distributed System uP-Computer/Bus Physical Mapping

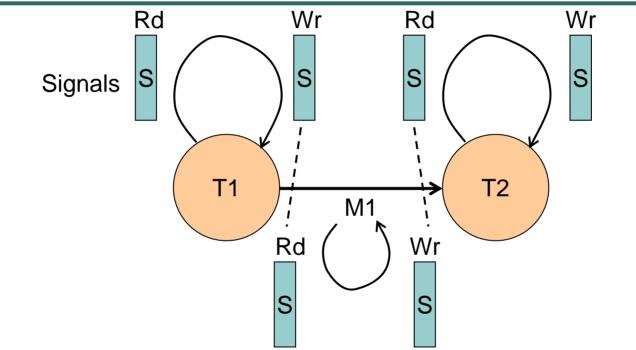


Message Assignment

- •Messages: M1, M2, M3, M4
- Internal to ECU, if Source ECU == Destination ECU
- •CAN_N bus segments selection based on Source:Destination of Task,
- •Routing is selected for shortest hops
- •Dynamic allocation based on topology selection
- •An ECU is the equivalent of a core, processor or computer.

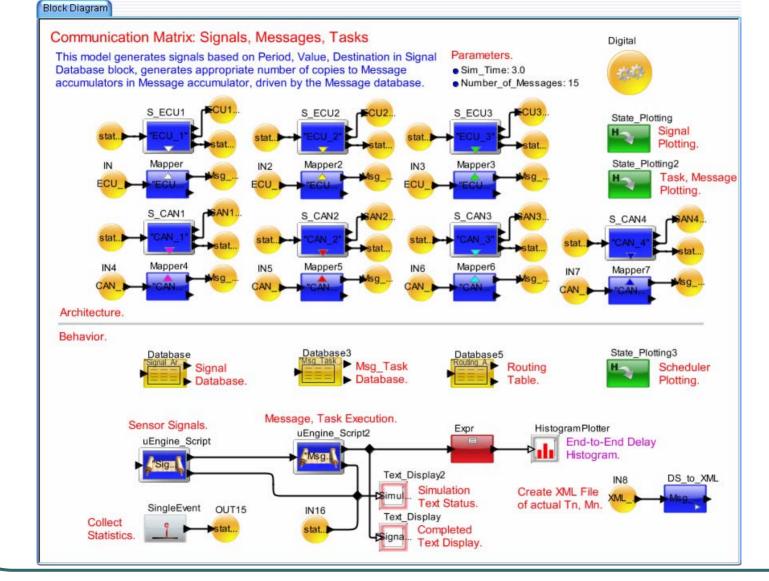


End-to-End Latency



- T1 writes latest S1(time) when task executes.
- M1 reads T1(time) via Middleware Buffer when it periodically executes, sends packet through Bus structure.
- T2 reads M1(time) from buffer when it fires via Middleware Buffer, and if the last node, outputs end-to-end latency.







Signal Table

3/	Block_Documentation:	Field Name S Signal_Name Plot_On	ummary: Signal_Value Plot_Color	Period Plot_Offset	WCET Plot_Value	Destinations				
	Linking_Name:	"Signal_Array"								
	Data_Structure_Text:	/* First row contains Field Names. */							1	
		Signal Name			WCET	Destinations	Plot On	Plot	d	
			1	1.0E-02	2.0E-2	{"M1","M2"}	true	red		
		\$2	2	2.0E-02	2.0E-2	{"M1","M2"}	true	blue		
		\$3	3	1.0E-02	2.0E-2	{"M1","M2"}	false	blue		
		54	4	1.0E-02	2.0E-2	{"M1","M2"}	false	blue		
		\$5	5	1.0E-02	2.0E-2	{"M1","M2"}	false	blue		
		S6	6	1.0E-02	2.0E-2	{"M1","M2"}	false	blue		
		\$7	7	1.0E-02	2.0E-2	{"M1","M2"}	false	blue	l	
		S 8	8	1.0E-02	2.0E-2	{"M1","M2"}	false	blue		
						\supset			•	
	Input_Fields:	"Signal_Name"								
	Lookup_Fields:	"Signal_Name"								
	Output_Expression:	output = match	" /* FORMAT outpu	ut = match.fieldb	*/				-	
	Mode:	Read								

Note: Destinations can be Tasks, or Messages



Task/Message Table

3/	Block_Documentation:	Field Name Summary:							
•			Msg_Task_Rate Plot_On	Msg_Task_Time Plot_Color	2 11 2 12 12 12 12 12 12 12 12 12 12 12	Read_Buffer Plot_Value	Write_Buff Trace		
	Linking_Name:	"Msg_Task_Array							
	Data_Structure_Text:	Msg_Task_Name	Msg_Task_Rate	Msg_Task_Time	Latency	Read_Buffer	Write_Buff		
		Ml	300.0E-03	150.0E-03	{0.0}	{"T1"}	{"T2"}		
		M2	500.0E-03	250.0E-03	{0.0}	{"T2"}	{"T4"}		
		M3	400.0E-03	200.0E-03	{0.0}	{"T1"}	{"T3"}		
		M4	600.0E-03	300.0E-03	{0.0}	{"T2"}	{"T3"}		
		Tl	100.0E-03	50.0E-03		{"S1","S2"}	{"M1","M3'		
		T2	500.0E-03	250.0E-03	{0.0}	{"M1"}	{"M2","M4'		
		Т3	700.0E-03	350.0E-03		{"M3","M4"}	{"DONE"}		
		T4	900.0E-03	450.0E-03	{0.0}	{"M2"}	{"DONE"}		
	Input_Fields:	"Msg Task Name"							
	Lookup_Fields:	"Msg_Task_Name"							
	Output_Expression:	"output = match" /* FORMAT output = match.fieldb */							
	Mode:	Read	1 orthan output				1		

Note: Read_Buffer, Write_Buffer columns can designate Tasks or Messages



Routing Table

/	Block_Documentation:	1: Architecture Resurce Mapping, Field Name Summary: Source Destination Hop						
	Linking_Name:	"Routing	Arrav"					
	Data_Structure_Text:							
			Destination					
		ECU 1	ECU 2	CAN 1	;			
		ECU_1	—	CAN_1	;			
		CAN_1	ECU_3	CAN_2	;			
		CAN_1	ECU_3	CAN_4	;			
		CAN_2	ECU_3	CAN_3	;			
		CAN_4	ECU_3	CAN_3	;			
		CAN_3	ECU_3	ECU_3	;			
		ECU_2	ECU_1	CAN_1	;			
	Input_Fields:	"Source	, Destination"					
	Lookup_Fields:	"Source	, Destination"					
	Output_Expression:	"output = match" /* FORMAT output = match.fieldb */						
	Mode:	Read						

Note: Simple Source, Destination, Hop format



Discovery Process

Discover Logical Path: M1 Source: T1 Destination: T2 Discover Physical Path: M1 Source: ECU_1 Destination: ECU_1

First Hop Array: {"NONE"}

No Further Processing Required...

Discover Logical Path: M2 Source: T2 Destination: T4 Discover Physical Path: M2 Source: ECU_1 Destination: ECU_3

First Hop Array: {"CAN_1"}

Second Hop Array: {"CAN_2", "CAN_4"}

Third Hop Array: {"CAN_3"}

Fourth Hop Array: {"NONE"} Final Hop Array: {{"CAN_1", "CAN_2", "CAN_3"} , {"CAN_1", "CAN_4", "CAN_3"} }

Discover Logical Path: M3 Source: T1 Destination: T3 Discover Physical Path: M3 Source: ECU_1 Destination: ECU_2

First Hop Array: {"CAN_1"}

No Further Processing Required...

Final Hop Array: {{"CAN_1"}

Discover Logical Path: M4 Source: T2 Destination: T3 Discover Physical Path: M4 Source: ECU_1 Destination: ECU_2

First Hop Array: {"CAN_1"}

No Further Processing Required...

Final Hop Array: {{"CAN_1"}



End-to-End Delay

- End-to-End Delay is composed of the following elements:
 - Task Signal or Message (Signal) Middleware Buffer, Periodic Task time, ECU Execution time
 - Message Task Middleware Buffer, Periodic Message time, Bus(n) Transfer time
- ECU Execution time:
 - Time due to arbitration/queueing, due to processing
- Bus Transfer time:
 - Time due to arbitration/queueing, due to transfer for each Bus segment in a path.

Note: Receive Interrupt, or Polling can be added



End-to-End Delay Equation

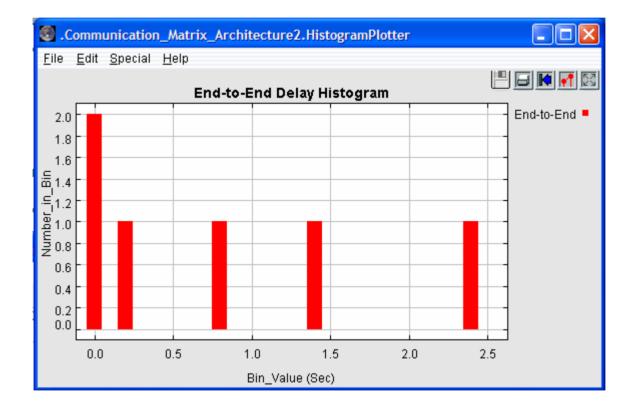
 $Latency = Task(i)s_{ample} + Task(i)_{Exec} + Msg(i+1)s_{ample} + Msg(i+1)x_{mit}$

where

 $Task(i)_{sample} = Sampling _Delay _of _Application _Software$ $Task(i)_{Exec} = Task _Exec _Time + Blocking _due _to _Higher _Priority$ $Msg(i+1)_{sample} = Sampling _Delay _of _Message$ $Msg(i+1)_{xmit} = \Sigma Message _Xmit _Time + Blocking _due _to _Higher _Priority$

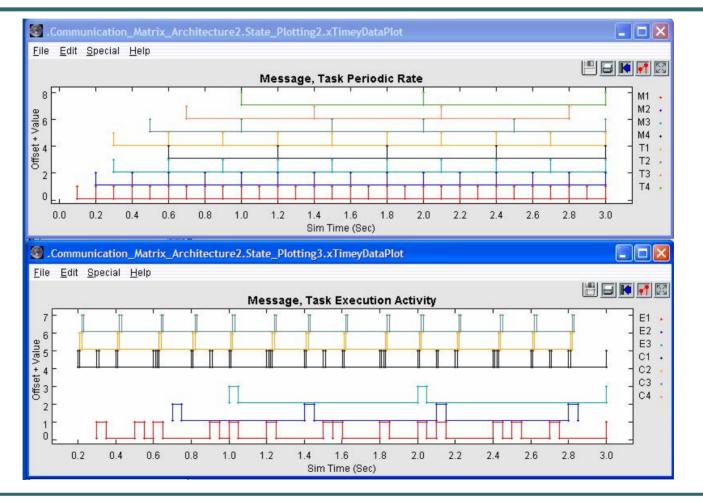


End-to-End Delay Histogram





Task, Message Execution





Model Assumptions

- Each Task will execute periodically for a specified time on an ECU, read from Middleware Buffers, or write a Signals from a prior Task from Middleware Buffers, desinated in a Table.
 - Columns: Read_Buffer Write_Buffer
- Each Message will execute periodically for a specified time, read from Middleware Buffers and send via Buses to a distant Middleware Buffer.
 - Same Columns: Read_Buffer Write_Buffer
- If a Task accepts two Middleware Buffers, each will be retained in an array to maintain proper end-to-end latency, or follow-on processing.



Model Assumptions (cont)

- Deployment of Tasks to ECUs and Messages to Buses
 - Discovery process is flexible enough to allow the specification of the mapping of tasks (t1, t2, t3, t4) to ECUs and the automatic determination of the mapping of messages (m1, m2, m3, m4) to buses.
 - User can map Tasks to ECUs in a table format.
- After Task completes, it will pass the transmit message, or receive message, through bus segments to continue the process, unless destination is "NONE".
- Model will select M1, M2, M3... paths during initialization of model and insert the shortest path into database memory for each Task.



Model Advantages

- A Table-Driven model should scale simply by modifying the table entries.
- A Table-Driven model should allow entry of physical mapping, or routing, from existing sources, some pre-processing to get into source, destination, hop format.
- User can allocate Signals, Messages, Tasks, to perform What-If scenarios.
 - A single Script-based block can support 32 independent periodic signals, tasks, or messages currently, and Mirabilis can provide 64 or 128 per block.
 - One Table might be created and allocated to different tables in a model.
- Additional Task logic could be added, either in script form, block style, or C code.
- Data structure fields can capture the internal flow with variable length arrays containing physical names in one array and timestamps in a double array.