MindTree adopts Mirabilis Design's VisualSim to deliver architecture exploration services to its semiconductor and hardware customers.
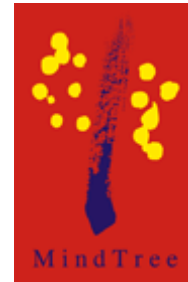
Multi-core project using VisualSim modeling libraries delivers 5X reduction in model construction and analysis time.

Bengaluru, India and Sunnyvale, USA — March 4th 2009— Mirabilis Design Inc., announced today that MindTree Ltd. has adopted VisualSim, a systems engineering software for performance analysis, power estimation and architecture exploration of electronics and real-time software, for offering early architecture exploration services to its hardware and System-on-Chip (SoC) customers.

MindTree selected VisualSim for the comprehensive modeling libraries, outstanding customer support, short learning curve and ability to conduct accurate design optimization with minimal knowledge of the implementation. VisualSim enables MindTree hardware designers to focus on design optimization and minimize the model development effort. MindTree has developed a highly optimized architecture specification for a 16-core Tensilica-based Network Processor using architecture exploration conducted in VisualSim.

 "Using VisualSim, we are able to design and validate customer specifications before scheduling any implementation," said Sridhar Perepa, General Manager, R&D Services at MindTree. "Mirabilis Design provided spontaneous modeling and application support that accelerated our learning and also a resource to discuss hardware architecture optimization. The available templates reduced our development time and the graphical environment enabled all team members to have uniform understanding of the new project. To summarize, the VisualSim model offers focused feedback and an efficient design optimization process throughout the implementation phase."

VisualSim methodology and libraries enable the project team to start with a statistical model with minimal implementation constraints. Once the static definition has been fully tested and validated, the model can be refined with implementation-specific details using the micro-architecture libraries. The graphical report generators provide feedback on key performance metrics including latency and utilization of shared resources, work queue build up and Quality of Service (QOS) efficiency throughout the SOC. The analyses validate the architecture choices at an early stage of the SOC development process and enable any ongoing refinement. VisualSim modeling libraries enables the user to vary the number of processor cores, modify the bus topologies and add new applications through parameters within a day.

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"VisualSim performance and power exploration solution has been demonstrated yet again to be mature and production-ready for high-performance and power-budgeted products," said Deepak Shankar, President of Mirabilis Design Inc. "The architecture exploration experience at MindTree clearly illustrates that the solution greatly reduces model development time, the biggest impediment to fast deployment of systems engineering solutions."

About MindTree

MindTree Limited is a global IT and R&D Services Company co-headquartered in the U.S. and India. MindTree's R&D Services business works with Technology companies to help build innovative products by providing Product Realization services. MindTree offers R&D services to a wide range of industries with its extensive experience and knowledge in diverse domains. MindTree adds functionality and helps companies bring products to market faster, through product engineering expertise and re-usable building blocks.

About Mirabilis Design

Mirabilis Design is a leading provider of System-Level Architecture Exploration software for designing electronics and real-time software. Using VisualSim, designers can architect the "right" product, i.e. one which minimizes product failures and has not been over- or under- designed. Mirabilis Design accelerates Concept Engineering by drastically reducing typical model development from months to days and overall project time by 25-30%. Benefits from the solution are a visual executable specification; easier creation of optimized and differentiated products and; corporate infrastructure enabling extremely fast design trade-offs for price, performance and power.

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