Real-Time Ray Tracing Software and Processor are successfully simulated using VisualSim

Editorial Contact
Vaishnavi Shankar
Mirabilis Design Inc.
Phone: 408-569-1103

Mirabilis Design Inc.
798 S Bernardo Ave
Sunnyvale, CA 94087
Tel: 408-245-8552
Email: info@mirabilisdesign.com

VisualSim enabled engineers to architect the software and processor to achieve 800 Teraflops for a Real-Time Ray Tracing system.

Sunnyvale, CA and Tokyo, Japan. — Nov 3rd, 2009 — Mirabilis Design Inc., today announced that VisualSim was used by a joint venture project involving TOPS Systems of Japan, to model, simulate and analyze the performance of a Real-Time Ray Tracing system with distributed software and a heterogeneous Multi-Core processor. The architecture development and software partitioning were conducted by developing performance and power models using the standard libraries in the VisualSim graphical environment. This model was used to optimize the processor architecture, application algorithms and data distribution to achieve 800 Tera floating point operations per second (TeraFLOPS).

"Perfect planning and validation of dynamic performance is absolutely essential to eliminate the considerable architectural and algorithmic risks in developing a system running at supercomputer performance. Performance of very data dependent processing such as Real-Time Ray Tracing can not be estimated without simulation", said Dr. Yukoh Matsumoto, Founder and CEO of TOPS Systems. "We completed the entire modeling effort in VisualSim in three months and achieved an 80% cost reduction for modeling compared with SystemC. Without VisualSim, the modeling would have required over 1.5 years of development effort."

Architects at TOPS Systems constructed a model of highly energy-efficient distributed processing system using VisualSim. The model of the core was built with the partitioned part of application software code. Components in the hardware platform had varying levels of details and accuracy, depending on the analysis to be performed. This modeling was used to analyze processing loads between cores and to see the bottle necks of the memory hierarchy. The design constraints of the system were the real-time performance, power consumption, and hardware resources implemented on 17mm square of silicon.

The hierarchical memories and busses model was constructed at cycle-accuracy using pre-built modeling libraries available in VisualSim. The computational model of each core was constructed based of each application code partitioned for Kahn Process Network based processing model with assertion for counting computation cycles and generating accurate bus transactions for memory accesses. The model combined over four hundred thousand (400,000) lines of algorithmic C-code with a cluster of heterogeneous Multi-Core processor to create the operating environment for Ray Tracing. The system

consists of 9 processor chips and an additional general purpose processor. Each processor chip consists of 8 clusters of heterogeneous Multi-Core processor, and a general purpose processor. Each cluster consists of 8 heterogeneous cores plus one memory management processor core. In total, 73 heterogeneous cores with hierarchical on-chip memories and interconnects running at 750 MHz per chip were included in the VisualSim model. The chip is targeted to be fabricated using 45nm manufacturing technology, by integrating 130 million gates and 24Mbit of memory into a 17mm square footprint. VisualSim was able to simulate the Multi-Core processor to achieve performance corresponding to 800 Teraflops which is required for Real-Time Ray Tracing at high-definition (HD) resolution at 1920 x 1080 pixels. The integration of the software onto the model enabled the model to dynamically compute the processing for complex software and component structures.

About Mirabilis Design

Mirabilis Design is a leading provider of System-Level Architecture Exploration software for designing electronics and real-time software. Using VisualSim, designers can architect the “right” product, i.e. one which minimizes product failures and has not been over- or under- designed. Mirabilis Design accelerates Concept Engineering by drastically reducing typical model development from months to days and overall project time by 25-30%. Benefits from the solution are a visual executable specification; easier creation of optimized and differentiated products and; corporate infrastructure enabling extremely fast design trade-offs for price, performance and power.

About TOPS Systems Corp

TOPS Systems provides a wide range of energy-efficient and scalable heterogeneous Multi-Core IP and solutions with distinct advantages from its proprietary Multi-Core and on-chip bus architecture, and optimizations through Architecture-Algorithm Co-Design and Hardware-Software Co-Design, to System Makers and SoC developers. TOPSTREAM™ - based products are used in applications ranging from battery-driven Information Appliances to High Performance Computers to break through the performance and power limits on current technologies. TOPS Systems has expert development team in Japan for a range of research and development for initial architecture definition and software development through design verification as their extension to reduce total development costs and speed time to market.

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