Mirabilis Design accelerates performance analysis and architecture exploration of FPGA and multi-FPGA systems by introducing Xilinx IP component model generators with built-in statistics

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Mirabilis Design joins the Xilinx ESL Initiative and announces VisualSim Xilinx FPGA Modeling Toolkit: Toolkit generates parameterized FPGA platform models to architect high-performance and high-availability systems

Sunnyvale, CA. — November 7th, 2006— Mirabilis Design Inc. of Sunnyvale, CA today announced that it has joined the Xilinx ESL initiative (www.xilinx.com/esl) to provide Xilinx FPGA designers with architectural exploration solutions for feasibility studies and virtual prototypes of FPGAs and multi-FPGA systems. In conjunction with its collaboration with Xilinx, Mirabilis Design also announced immediate availability of the new VisualSim Xilinx FPGA Modeling Toolkit that enables quick prototypes of new and derivative systems using parameterized models of FPGA platforms. With this virtual prototype, designers can select the right architecture by conducting rapid and extensive performance trade-offs during the product definition phase.

"Mirabilis Design's focus on providing tools for FPGA architects to increase confidence in the architecture and eliminate design bottlenecks aligns with the goals of our ESL Initiative," said Steve Lass, senior director of marketing at Xilinx. "Virtual prototyping of FPGA platforms using VisualSim can enable customers to optimize their specification to achieve the required performance, minimize system power and maximize functionality."

This VisualSim Xilinx FPGA Modeling Toolkit generates simulation models of the proposed system from user-entered information in a graphical template and spreadsheet without requiring any software programming. The Xilinx FPGA models are combined with standard and custom components from the VisualSim modeling library to create the virtual prototype of the full system. These models can be used by embedded system architects to optimize the resource allocation; partitioning into hardware and software; and experiment with functional flows.

The VisualSim Xilinx FPGA Modeling Toolkit contains parameterized generators of the processors (PowerPC™ and MicroBlaze™ cores), memories (block RAM, SDRAM and Caches), buses (CoreConnect PLB, FSL Bus and CoreConnect OPB) and communication devices (Ethernet and PCI). This toolkit contains models of the popular Xilinx Virtex™ family of FPGAs including the new Virtex-5 devices. The FPGA platform, traffic sequence and software tasks are described graphically, and simulation runs are conducted by varying different hardware attributes such as queue depths, resource speeds, bus widths, number of processors and memory sizes. Applications and algorithmic behaviors are

described as concurrent functional flows that are modeled as priority-based variable delays, instruction sequence or behavior descriptions. The virtual prototypes have built-in statistics generators that produce performance and power summaries including queue occupancy, percent utilization, effective throughput, power consumed per device, stall and idle times, cache hit-ratios, and end-to-end latencies.

You can learn more about this toolkit, the application and the technology from an article recently published in the *Xcell Journal* at: http://www.xilinx.com/publications/xcellonline/xcell_58/xc_pdf/p019-021_58-mirabalis.pdf.

Availability

The VisualSim Xilinx FPGA Modeling Toolkit is currently available on Windows, Linux and UNIX. The library requires VisualSim Architect to simulate. Annual pricing for the toolkit starts at $5000. Projects using the VisualSim Xilinx FPGA Design Toolkit are currently underway for designing embedded for defense, video broadcast and industrial applications.

About Xilinx ESL Initiative

The Xilinx ESL Initiative is a multi-faceted program aimed at proliferating high-level design methodologies and tool flows for FPGAs. The goal is to make it easier for hardware designers and software programmers to leverage Xilinx programmable devices for their next generation systems. Xilinx and participating companies are focused on improving ease of use, quality of results and interoperability standards through technical collaboration, cooperative marketing and joint educational activities. For more information about the Xilinx ESL Initiative, visit www.xilinx.com/esl.

About VisualSim

VisualSim Architect is a graphical, platform-independent design environment that accelerates performance analysis and architecture exploration. Designers construct models using pre-built parameterized construction components and use the automated statistics and run-time visualization for ad-hoc analysis. VisualSim optimizes the initial concept through a series of modeling refinement and abstraction to deliver the best architecture as an executable specification.

About Mirabilis Design

Founded in 2003, and headquartered in Sunnyvale, CA, USA, Mirabilis Design is a leading provider of System-Level Architecture Exploration software for designing electronics and real-time software. Using VisualSim, designers can architect the “right” product, i.e. one which minimizes product failures and has not been over- or under- designed. Mirabilis Design accelerates Concept Engineering by drastically reducing typical model development from months to days and overall project time by 25-30%. Benefits

from the solution are a visual executable specification; easier creation of optimized and differentiated products and; corporate infrastructure enabling extremely fast design trade-offs for price, performance and power.

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