High Performance-Low Energy Super-Computing Processor

Product

Designing the microprocessor for supercomputers

Business

A microprocessor for the exascale system to perform one billion calculations per second.

Product Overview

Mesh Network with 72 CPU cores and 68 L3 cache slice with 4x HBM2E controllers and 4-6 DDR5 controllers. The processor will target TSMC 7 nm process. The processor must exhibit high reliability and over one Terabyte of sustained memory throughput.

Team Background:

Performance architects and software developers.

Challenges

- To achieve the exascale performance at energy efficient rates
- Selection of key components in processor based on quantitative measurements.
- Cycle-accurate models of the processor, NoC and memory components are not available from their respective vendors for architecture trade-offs.

Results

- Architect was able to construct a cycle-accurate component-specific model of the exascale processor in VisualSim Architect.
- VisualSim explorations helped in reducing the average power by 30.386% and peak power by 26.67%.
- Model construction and validation took 4 man-weeks
- Initial model used traffic generators to represent the processor. Later versions used the cycle-accurate models of the ARM Neoverse N1 provided by Mirabilis Design
- VisualSim architect helped in selecting optimal configuration for shortest interconnect lengths which reduced wire delay and saved wire power. Model helped select the lowest clock speeds and reduced design complexity

VisualSim Solution

- VisualSim cycle-accurate IP libraries: ARM Cortex A77, ARM Neoverse N1, CMN600 Network-on-Chip, HBM2.0E, DDR4 DRAM, DDR5 DRAM, DMA and AMBA AXI
- VisualSim Model reports: buffer occupancy at each router; latency and throughput across each wire, task response time, routing efficiency, quality of service selection, and coherency overhead.