Flight computer

Product

Flight computer using the BAE Systems PCI-RAD Board, Xilinx FPGA and custom DMA boards.

Business

Customer focus is on robotic exploration of the Solar System. They create flight avionics systems to handle movement, instruments for planetary and earth science and space-based astronomy.

Project Overview

The project requires verification of traffic patterns and flows from multiple boards and instruments to the Central Processing board. The second task was to determine the maximum software timing deadlines to schedule all the Orbiter operations.

Team background

System Architects and Software Engineers

Challenges

- Lack of complete System view and limited information on resource utilization.
- Decisions to increase throughput and reduce memory response time by adding another cache to the PCI-RAD board. The cost of NRE would be exorbitant.
- The FPGA development would add 6-9 months and delay decisions.
- Spreadsheets cannot capture concurrency and PCI multi-level arbitration.

Results

- Digital Twin of the full Orbiter was modeled in VisualSim Architect from Mirabilis Design
- The model had seven boards which was simulated for over one week of activity. The consolidated simulation took less than one hour.
- Complete model development in VisualSim environment took 6 weeks.
- Task timing deadline and DMA responses times were provided to integration testing.

VisualSim solution

- VisualSim Architect Library: BAE Systems PCI-RAD board, DMA and traffic models
- Model parameters used for the evaluation: Master disable feature, Latency timer, multi-level priority arbitration, DMA burst size and 60X bus options
- Configuration for number of masters, L2 cache, DDR3 and sensors
- Different use-cases and processing were tested for timing, throughput and buffering occupancy