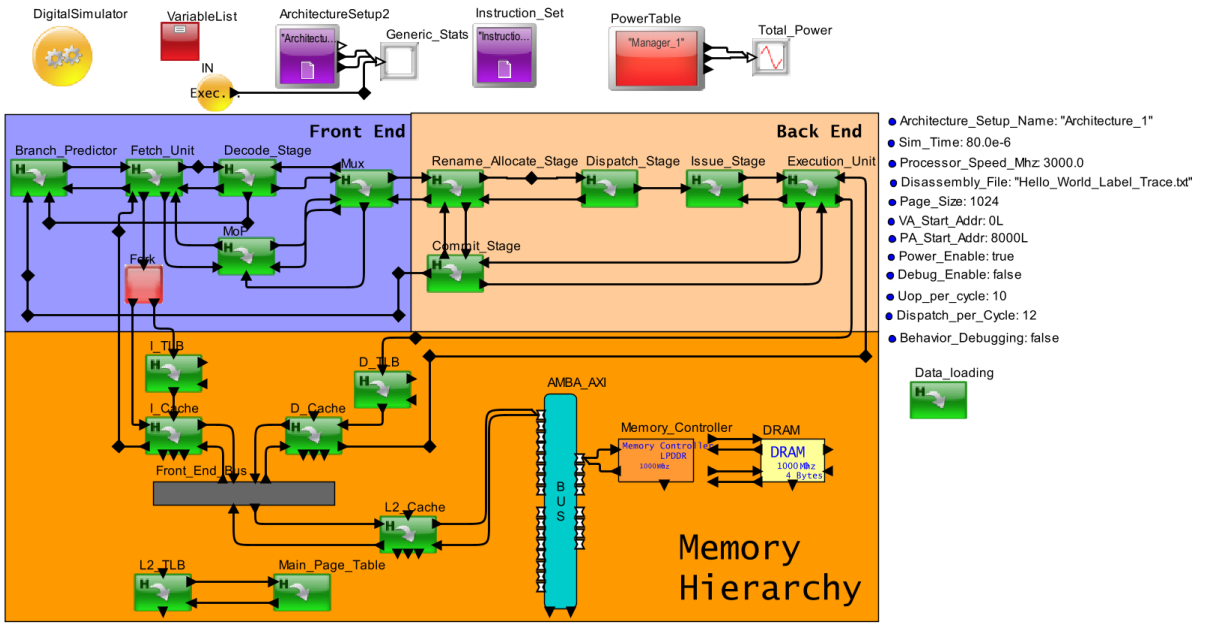
Latest in the VisualSim World



This is our sixth newsletter and the second of 2022. It has been a very satisfying search to find new information. Please drop me an email if you have special requests or alternate topics to discuss.

As more products and System-on-Chips (SoC) are integrating Artificial Intelligence (AI) Accelerators, the space on boards and semiconductors is becoming very tight. You have CPU for general applications, GPU for graphics, DSP for signal processing, Audio/MPEG for media, NPU for protocol handling, accelerators and now, AI accelerators. All these technologies are attached to an AXI Bus, Network-on-Chip, Token Ring or a proprietary interconnect.

Predicting the traffic impact and scheduling the AI tasks is a major challenge that cannot be easily understood using a spreadsheet. To complicate matters, add the impact of power consumption and capacity efficiency. Mirabilis Design's upcoming webinar in March presents the methodology and results of a system-level experiments on trade-offs between power, response time and functional obtained through AI Accelerators.

In this issue, we also bring:

- Spotlight Series - what it means to intern at Mirabilis Design
- Success Story - Virtual Prototyping of a Reconnaissance Satellite Sub-System created by a major avionics supplier
- A free-wheeling article on the role of AI in cars, defense, and infotainment
- Power modeling and estimation in early system design

Join the Webinar on Balancing Performance and Power in AI Accelerators for System-on-Chip (SoC)

The AI revolution is driving the need for an entirely new generation of accelerators in System-on-Chip (SoC). Design tools that explore the scheduling, flow control, data movement and parallelism in semiconductor devices represent the forward movement in productivity and cost optimization.

In this environment, it is important to point out some critical parameters for project success:

- Estimating the power advantage of implementing an AI algorithm on an accelerator
- Sizing the AI accelerator for existing and future AI requirements
- The latency advantage between ARM, RISC, DSP and Accelerator in deploying AI tasks

The webinar will focus on design teams transitioning to an AI accelerator in their next-generation SoC processor and the resultant benefits. If you would like to know more about these parameters and incorporate them into your environment, register for this webinar on Thursday, March 10, 2022.

Spotlight Series – 1

What do our interns think about working at Mirabilis Design? How do they learn new concepts and engage with customers? Click here and view intern Snehal Ranjan's recent experiences working at Mirabilis Design.

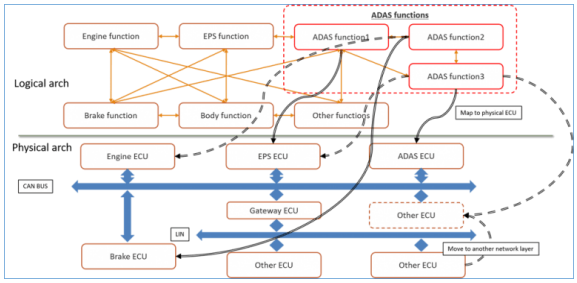
Success Story - Reconnaissance Satellite Sub-System Prototype

Mirabilis Design Inc.'s customer is a manufacturer of avionics and airplane engines with a multibillion dollar turnover. A new reconnaissance satellite required concurrent processing, large data transfers, new interfaces, multi-core processor, and communication with other satellites, aircrafts, and ground stations.

Read on to know how VisualSim was used to create the virtual prototype, and the software, hardware and network were tracked, optimized, and tested.

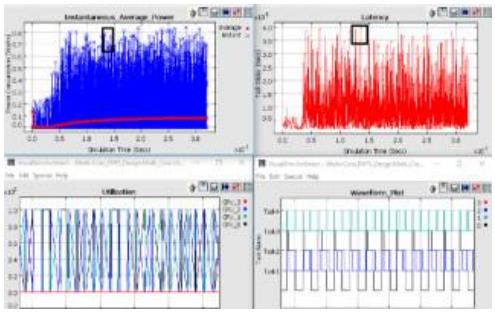
Role of AI in a Variety of Applications and the Associated Design Challenges

Rapidly build a virtual prototype with VisualSim to understand the nuances of AI hardware behavior, timing, throughput, power consumption, and quality of service trade-offs...



Read on by clicking here

Power Modeling and Estimation in Early System Design



With the increase in SoC design complexity, system-level power estimation is becoming a critical factor. This article explains why this is the case and introduces a comprehensive modeling platform for evaluating the power consumption of subsystems, chips, and entire systems.

Read on to know more

Deepak Shankar
Mirabilis Design Inc., 1159 Sonora Ct, Suite 116,
Sunnyvale, CA 94086