Conduct micro-architecture analysis before RTL is available and validate the specification

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Mirabilis Design Releases Micro-Architecture System-Level Modeling Platform

Sunnyvale, CA — February 28, 2022 — Mirabilis Design Inc, the leading provider of system-level Intellectual Property and Simulation Solutions for electronics and processors, announced today the release of VisualSim Micro-Architecture Modeler. This is the first solution to enable System-on-Chip (SoC) designers and verification engineers to verify the micro-architecture of the entire SoC at cycle-per-cycle. The semiconductor devices can be verified for timing, throughput, cycle per instructions, power consumption and functional correctness. Hardware engineers can verify the cause of a latency for a specific instruction across the entire SoC, or get the average latency for the Dhrystone, application-specific benchmark or specmark.

“Our users have always wanted to go deep into the processor core, and vendors have not been shipping cycle-accurate models for high-end cores. Until now, the VisualSim hybrid solution was the closest alternative to expensive emulators and extremely slow RTL execution to analyze the architecture”, said Deepak Shankar, Founder of Mirabilis Design Inc. “This micro-architecture is based on three years of advanced research to understand the mapping of RTL into an abstract model that runs 10000+ instructions per second and still maintain a 85-95% accuracy.”

The verification using the Micro-Architecture Modeler covers the processor core, cache, interconnect, memory controller and accelerators. The library components are used to quickly assemble cycle-accurate and architecture-accurate models, run Monte-Carlo simulation, and receive Insights into the system operations. The library covers all aspects of the micro-architecture with a set of ten parameterized IP components, pre-built ARM and RISC-V cores, and reconfigurable components to create proprietary versions.

The advantage of this solution is that every aspect does not need to be programmed. The user can quickly customize using the parameters or by modifying existing code. The simulation speed is about 10-1000X faster than RTL and is significantly faster than emulation. Moreover, the models are available very early in the design process. Each component is fully documented with the source code being available, video tutorials showing the flow of instructions, and parameters that configure the IP blocks. The IP blocks also have flexible port structure and can be connected in any configuration. Mirabilis Design has assembled over seven different SoCs; an average SoC takes about two weeks to assemble using the existing IP with no modifications.

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Features and IP libraries include In-order, out of order, branch prediction, fetch, micro-operations, macro-to-micro translators, decode, Mux, Rename stage, Commit, Dispatch, Issue, Execution Units, flow control between stages, buffers, switches, multi-level caches, registers, memories and interconnects. Standard statistics available include buffer occupancy, stall times and timing diagram of a single instruction or group of instructions, CPI, MIPS, latency, throughput, power per device, power cumulative, instant power and average power. No programming is required to use this library and the pre-built models allow for quick ramp-up and easy assembly of new systems. Complex reverse engineering is not required and the full-length code can be executed.

Who will use the cycle accurate modeling?

- Microarchitecture designers developing their own processors
- System SoC teams needing better understanding of instruction-level and hardware behavior
- Designers developing custom pipelines and accelerators.

About Mirabilis Design Inc.

Mirabilis Design is a Silicon Valley software company, providing software solutions to identify and eliminate risk in the product specification, accurately predicting the human and time resources required to develop the product, and improve communication between diverse engineering teams. VisualSim Architect combines Intellectual Property, system-level modeling, simulation, environment analysis and application templates to significantly improve model construction, simulation, analysis and RTL verification. The environment enables designers to rapidly converge to a design which meets a diverse set of interdependent time and power requirements. It is optimally used very early in the design process in parallel with (and as an aid to) the development of the product's written specification and long before an implementation (for example, RTL, software code, or schematic) of that product can even be started.

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