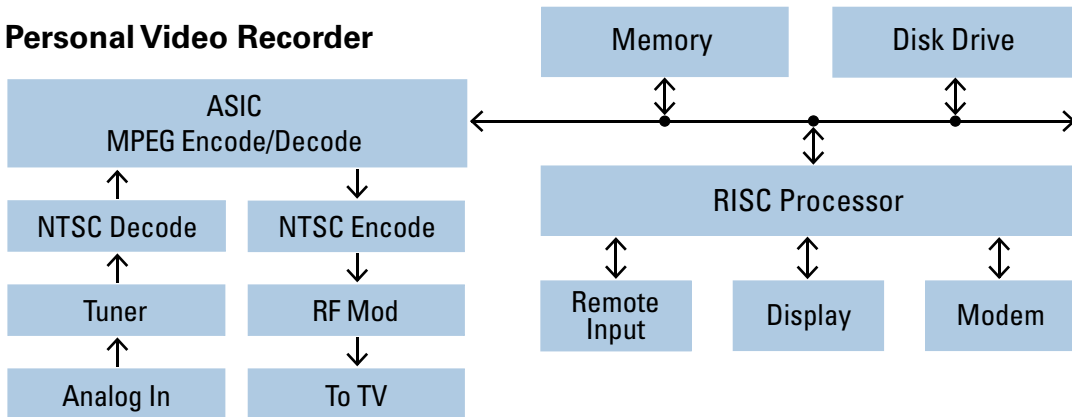


## Product Data Sheet

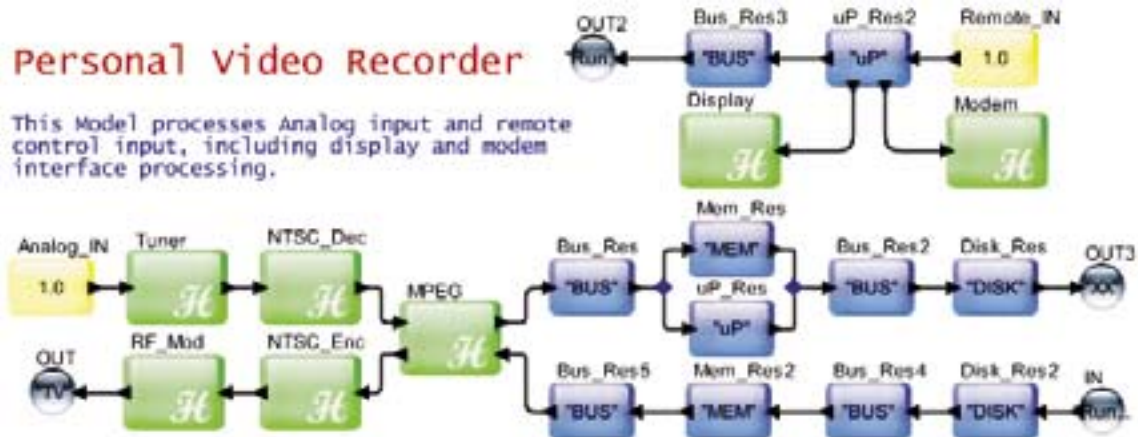


### Personal Video Recorder



### Personal video Recorder

This Model processes Analog input and remote control input, including display and modem interface processing.



Map System Specification to VisualSim Model

VisualSim Conducts	VisualSim Uniqueness	VisualSim Benefits
<ul style="list-style-type: none"> <li>• Performance Analysis</li> <li>• Architecture exploration</li> <li>• Algorithm validation</li> <li>• Hardware-software trade-off</li> <li>• Dynamic mapping of behavior to architecture</li> </ul>	<ul style="list-style-type: none"> <li>• Consolidates multiple tool requirements in one</li> <li>• Graphical blocks for both hardware and software</li> <li>• Communicate and execute models over the internet</li> <li>• Smaller block list with greater functionality</li> <li>• Alter operations with dynamic parameter changes</li> </ul>	<ul style="list-style-type: none"> <li>• Reduce modeling time from months to weeks</li> <li>• Significantly lower learning curve</li> <li>• Internet-based model sharing</li> <li>• Extensive analysis capabilities</li> <li>• Technology risk-reduction</li> <li>• Ensure reusability</li> </ul>

**V**isualSim™ is the industry's first fully integrated solution for end-to-end system-level design. The graphical nature of the product and the availability of the innovative parameterized library, SmartBlocks™, make the tool easy to use, adopt and learn, thus providing immediate benefit to the organization.

VisualSim is the first commercial software package to combine DSP, Analog, Protocols and Digital Architecture in a single simulation model.

**S**martBlocks™ are graphical representations of hardware, software and networking components at queuing, performance, transaction and cycle-accurate levels of abstraction.

VisualSim can be used for performance trade-offs using metrics such as bandwidth utilization, application response time and buffer requirements. Architecture analysis of arbitration algorithms, component sizing, software instruction optimization, hardware-software trade-offs and system coverage.

## Core Features

- Graphical modeling environment for rapid model development and presentation
- Hierarchical definitions for large model creation, reuse and easy understanding
- Platform independent (Solaris, HP/UX, Windows, Linux and Mac OS/X)
- Visual debugging including breakpoints, stop and restart, and graphical animation
- Tightly integrated html-based help, block documentation and modeling guides
- Publish models to execute within a Web Browser as Java Applets

## Modeling Features

- Schematic editor with common menu functions
- Separation of workload, behavior architecture for dynamic mapping
- Modify block parameters to define user specific operation

## Simulation Kernel

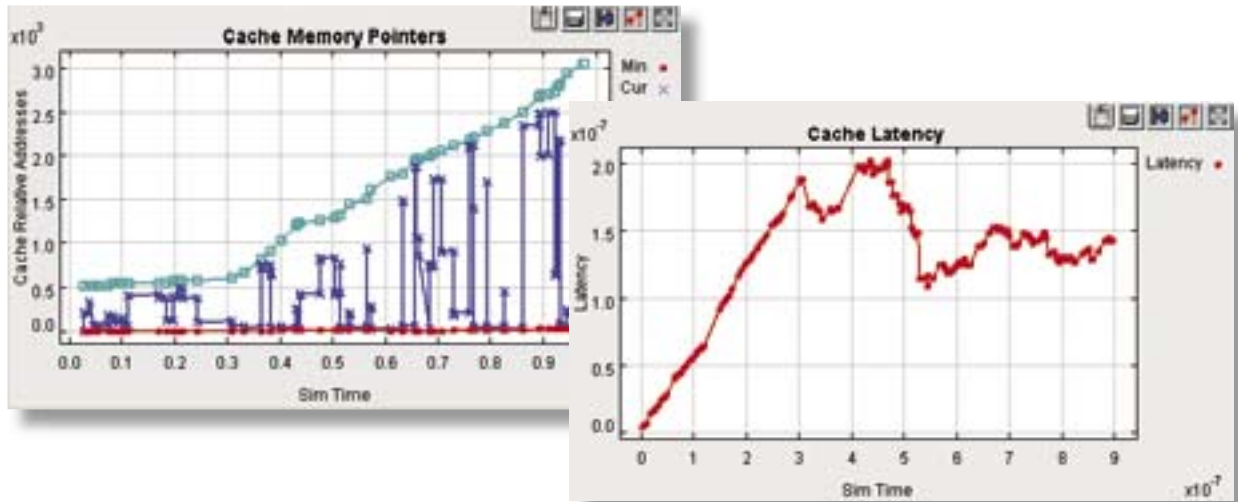
- Discrete Event: Architecture and performance modeling
- Synchronous Data Flow: Baseband, hardware and embedded software
- Finite State Machine: Network protocols
- Continuous Time: Analog and control systems

## Analysis and Debugging Features

- Dynamic probes at ports, blocks and simulator for validation of system correctness, flow review and syntactical debugging
- Interactive viewers in the form of XY, histogram, scatter, timeline, waveform and text
- Specialized viewers for images, audio, signals and video

## Documentation and Publishing

- Publish models and associated analysis as a Java Applet
- Create dynamic specifications and marketing material with executable models



Simulation Results to Optimize System

## Digital and SmartBlocks™ Library Features

- Complete parameterized library for performance analysis and system architecture exploration
- Extend existing blocks through built-in features
- Digital library contains basic blocks for functional and performance details of hardware / software
- SmartBlocks provide architecture components to define custom processors, memory, cache, controllers, bus, pipeline stages, DMA, RTOS, instruction sets and algorithm behavior generation

## Technology-Specific Library

- Sources, sinks, DSP algorithms and analog functions for mixed signal design
- Application-specific library for communications, imaging and audio
- Large functional library of protocols, networking and routing operations

## Demonstration Systems

- Industry's largest set of demonstration systems that cover all variations of system-design including performance, algorithm, architecture and environmental
- Designs of hardware systems, software scheduling, signal and imaging processing, mixed-signal, control systems and protocols

## Interfaces and Extensions

- Tcl foundation for model creation, simulation control and analysis
- Model library extension using Java/C/C++
- Functional interface to third-party simulators, Excel and files
- Support hardware interface to networked devices and serial IO

## Top-Level listing of the VisualSim™ Library



SmartBlocks™	Digital	Networking
Hardware Software Networking Traffic Resources	Traffic Generators Transaction Manipulators Switches, Memories Queues, Resources Flow Management	Nodes Link Masters Protocol Layers Routing Setup PHY Interface

All libraries are parameterized, extendable and come standard in VisualSim Architect

Analog	DSP	Image Processing	Interfaces
Event Generators Waveforms Integrators Differentiators Laplace System	Sources Audio Communication Statistical Filtering Spectrum Analyzers	Transforms Manipulation Processing Functions Video Interfaces Readers and Writers Audio, Video and Images	C/C++/Java Networked Hardware Serial Interface Excel and Files Trace File C-Based Simulators

Debuggers	Model Library	Simulators	Probes & Plotters
Breakpoints Stop & Restart Trace Tracking Animation Dynamic Plotters	Hierarchical Block Dynamic Instantiation Unit Conversion Systems Mathematical Operators Visual Prototyping	Discrete Event Finite State Machine Synchronous Data Continuous-Time	Probing Timeline Histograms Scatter Signal & Waveform Statistics Generation

## Products



### VisualSim™ Architect

- Client simulation package for model creation, execution and analysis
- Schematic editor and post processor
- Four high-performance simulators in a single kernel
- Library of digital, analog, DSP, imaging and SmartBlocks™
- Licensed per local concurrent user

### VisualSim™ Explorer

- Web Server software
- Enables remote model execution in Web Browser
- Licensed per server machine

### Compatible Platforms

- Platform-independent
- Requires Java 1.4.1\_01 or higher

**Contact Information:** Mirabilis Design Inc. | Tel: 408-245-8552 | [www.mirabilisdesign.com](http://www.mirabilisdesign.com) | Email: [info@mirabilisdesign.com](mailto:info@mirabilisdesign.com)

**Copyright Notices:** Mirabilis Design, SmartBlocks and VisualSim are trademarks of Mirabilis Design, Inc. in the United States and other countries. All others are properties of their respective companies.